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Towards a next-generation hybrid switch: Challenges and insights on the parallelization of SiC-MOSFET and Si-IGBT

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ABSTRACT The application of hybrid semiconductor switches (HyS) emerges as a solution to the increasing demand for higher switching frequency and power density at a competitive cost. This paper investigates a HyS based on Si-IGBT (silicon-insulated gate bipolar transistor) in parallel with a SiC-MOSFET (silicon carbide-metal oxide semiconductor field effect transistor), highlighting the main characteristics and challenges to obtain a cost-effective device. Simulations in PLECS and LT-Spice reveal significant phenomena that arise during the conduction and switching of HyS devices. Experimental tests conducted on a double pulse test circuit validate the initial analyses and compare HyS switching losses with the standard solution based on IGBT. Finally, some insights on this technology are provided.

KEYWORDS Hybrid Switch; Silicon IGBT; Silicon Carbide MOSFET; Parallelization; Cost-effective Design.

I. INTRODUCTION

Silicon-based devices have already reached a high degree of maturity, which results in components operating close to the material physical limits. In this context, wide bandgap semiconductors (WBS) emerge as a solution to higher conversion efficiency and higher power density demands. SiC-MOSFET (silicon carbide-metal oxide semiconductor field effect transistor) and GaN HEMTs (gallium nitride-high electron mobility transistors) are examples of WBS-based devices.

These devices have demonstrated superior performance compared to silicon-based devices in terms of switching times, power losses, and better heat dissipation, particularly for the SiC-MOSFET [1]. The latter represents a feature of interest since temperature plays a relevant role in the instability phenomena of bipolar silicon devices [2].

Wide-bandgap materials enable the extension of the operating range of unipolar power devices. Discrete SiC-MOSFETs are commonly utilized in markets that demand blocking voltages of 650 V and 1200 V, which is the typical design range for low-voltage variable speed drives (LV VSD), competing directly with Si-IGBTs.

However, since it is a relatively new technology, it has higher prices than its Si-IGBT counterparts, so this has remained the main barrier to its large-scale use [3]. For comparison, global power IGBT sales exceeded global power SiC sales by more than 5 times in 2022 [4]. The prices of Si and SiC power devices in the TO-247 package with a blocking voltage of 1200V are compared in Figures 1 and 2. The price difference between the two types of devices tends to increase significantly as the nominal current increases. Additionally, for higher currents, there is a shortage of SiC devices due to their unattractive cost.

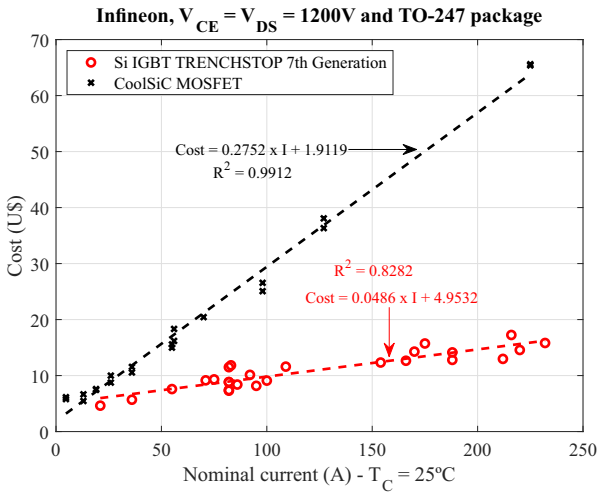

FIGURE 1. Unit cost comparison of Si-IGBT and SiC-MOSFET from Infineon Technologies company. Devices with 1200V blocking voltage and TO-247 package [5]. Data collected in May 2024.

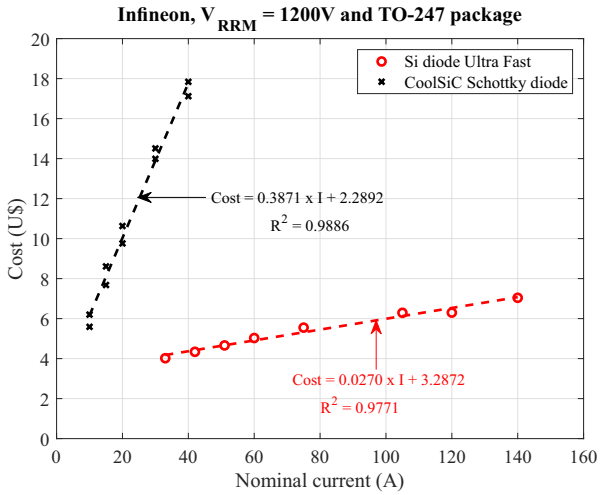

FIGURE 2. Unit cost comparison of Si diodes and SiC Schottky diodes from Infineon Technologies company. Devices with 1200V blocking voltage and TO-247 package [5]. Data collected in May 2024.

One way to exploit the advantage of WBS-based devices and obtain an intermediate cost is by merging different technologies. This association is known as hybrid switch (HyS). An already widely used approach in power converters is the combination of Si-IGBT and SiC-Schottky Barrier Diode (SiC-SBD). Due to the excellent reverse recovery characteristic of the SiC-SBD, this hybrid switch presents lower losses and improves the IGBT device switching response during turn-on [6].

Another investigated approach, the focus of this paper, is the parallel arrangement of a Si-IGBT and a SiC-MOSFET illustrated in Figure 3. This HyS is an alternative to reduce the device cost per ampere because it takes advantage of the superior conduction characteristic of Si-IGBT and the better switching properties of SiC-MOSFET. This approach can reach higher rated power and switching frequency if compared with full Si-IGBT application [3] or the association of Si-IGBT and SiC SBD [7].

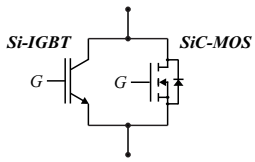

FIGURE 3. Investigated Hybrid Switch - Si/SiC HyS.

The selection of the devices to compose the Si-IGBT/SiC-MOSFET pair must focus on the current distribution. It is desired that the Si-IGBT takes on most of the current during the conduction period and the SiC-MOSFET takes on the most current only during the switching period. In this way, smaller areas of SiC are used, reducing the cost of HyS compared to an application with full SiC MOSFET of the same nominal current as the IGBT. References [8] and [9] investigated methodologies to optimize the nominal current selection of the devices to guarantee the smallest area of SiC and a safe operation of the HyS at the lowest cost.

More recent studies have turned their attention to the development of switching control schemes since it is a crucial factor in device performance. For instance, depending on the switching control schemes, the IGBT can achieve zero voltage switching (ZVS). Figure 4 illustrates the main gate control options proposed in different papers [10], [11], [12], [13]. These options differ in the relative time between the turn-on and turn-off of the IGBT and MOSFET.

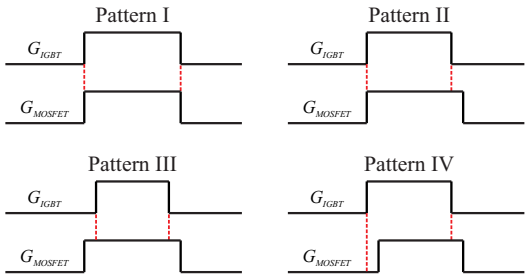

FIGURE 4. Hybrid Switch gate signals patterns investigated in the literature.

It has been observed that for different loading conditions, the most efficient pulse sequence varies [10]. References [10] and [11] compared the different switching patterns shown in Figure 4 considering a VSD application. In terms of efficiency gain, the best turn-on configuration occurs when both devices start to conduct simultaneously (patterns I and II). For the turn-off, when the Si-IGBT is turned off before the SiC-MOSFET (patterns II, III, and IV), better results regarding lower switching losses are obtained. Pattern II has therefore been investigated as the best available pulse sequence in general terms for loss reduction. This scheme also allows the triggering of the pair through a single gate driver, as recently published in [14]. However, it has been observed that for different loading conditions, the most efficient pulse sequence varies [10].

References [15] and [16] propose a methodology for varying switching pattern and frequency as a function of the load current. This proposal presented a reduction of losses when compared to the selection of only one switching method, and improved the reliability by reducing the stress caused by overcurrents in the SiC-MOSFET for operations with higher loads.

Another interesting approach, discussed in references [12], [17], [18], [19], involves adjusting the switching times between the IGBT and SiC MOSFET to achieve thermal balancing between the two devices. This strategy can enhance the reliability of the HyS, potentially allowing for increased operating frequencies or current limits. However, this method presents challenges, including the need to monitor the case temperatures of the devices and to implement a control loop that adjusts the switching times.

Moreover, the development of gate-drivers are object of study in references [13], [14], and [20]. In these cases, the

most sought-after figures of merit are cost and simplicity. One notable proposal is from [14], which uses a single gate driver and a simple auxiliary circuit for the delay generation. However, only the switching pattern II can be implemented.

Despite the many published works, there are still gaps related to the design and evaluation of the hybrid switch in a real application. This work extends the developments of [3] and [21], investigating the behavior of the HyS in PLECS e LTspice simulations. To understand the current sharing between the devices, a generic model was developed to determine the current for the Si-IGBT and SiC-MOSFET at different load current values. This was achieved by utilizing a database containing the conduction resistances and on-state voltage drops of various commercial 1200 V devices.

Furthermore, for the analysis of the switching transients of the HyS, the voltage and current behavior were examined for a hybrid pair consisting of a Si-IGBT and a SiC-MOSFET with nominal currents of 15 A and 13 A, respectively. In this study, the use of an active Miller clamp function and the choice between an IGBT with or without an anti-parallel diode were found to have a significant impact on the operation and viability of a hybrid pair.

Finally, this study is a extended version of [22], where additional analysis are included. Also, this paper provides experimental results on the energy dissipated by HyS devices during tests carried out in a double-pulse test circuit. The results were gathered for different turn-off times between the SiC-MOSFET and the Si-IGBT, and were compared with the losses in a Si-IGBT.

The upcoming sections of this article are outlined as follows. Section II analyzes the current division that occurs in a HyS. The behavior of the transistors during switching is investigated in Section III, while Section IV focuses on the operation of the diodes. Section V presents an experimental analysis of the HyS switching losses, while section VI provides insights into the functional implementation of a hybrid pair. Finally, Section VII contains the conclusions.

II. CONDUCTION PERIOD: CURRENT SHARING

The conductivity modulation guarantees to the Si-IGBT lower conduction losses in nominal current when compared to the SiC-MOSFET [23]. Indeed, most of the current should flow through the IGBT during the conduction period in a cost-effective HyS. During this interval, SiC-MOSFET and Si-IGBT can be approximated by resistors. For the MOSFET, its conduction resistance value ($R_{ds,on}$) is informed in the datasheet and depends on the device nominal current, blocking voltage, gate-source voltage, and temperature. For the IGBT, such information is obtained from the forward voltage drop of the IGBT ($V_{CE,sat}$) and depends on the same parameters as the MOSFET. The non-linear behavior of the IGBT voltage drop means that the device resistance also depends on the current flowing through it.

Figure 5 proposes a current sharing model during the conduction period. It is important to highlight that the IGBT is often modeled during the conduction period as a resistor R_{on} in series with a voltage source $V_{CE,sat}$. This study, alternatively, represents the IGBT as a nonlinear resistance. This approach incorporates the non-linear behavior present at lower currents, and the use of passive modeling leads to a numerically stable model, which is often not achievable when using a voltage source in series with a resistor [3]. The parameters of the current sharing model were obtained through curve fitting of several commercial devices. More details on this model and its validation are presented in Appendix A.

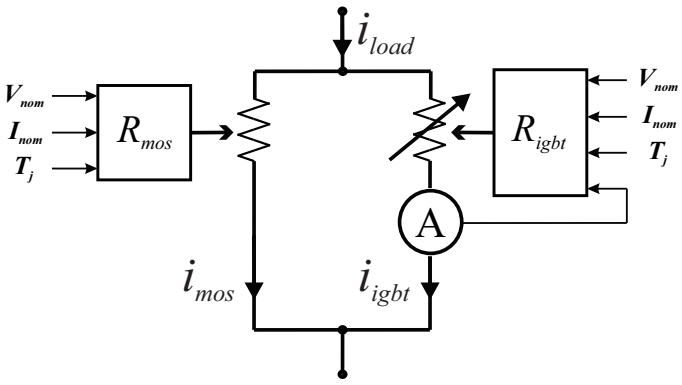

FIGURE 5. Current sharing modeling during the conduction period.

With the resistance models of the SiC-MOSFET and the Si-IGBT, the current division is obtained from simulations of the circuit represented in Figure 5. The software PLECS is used. The results were obtained for different load currents i_{load} and different nominal currents of the devices.

Figure 6 illustrates the current division for different nominal current values of the SiC-MOSFET and different load currents, while keeping the nominal current of the IGBT at 15 A (Figure 6 (a)) and at 25 A (Figure 6 (b)). At the same operating point (equal total and nominal current), it can be noticed that with an increase in the nominal current of the IGBT, there is an increase in the percentage of the total current passing through the device. This is a consequence of the decrease in resistance caused by the higher nominal current. With the silicon device conducting most of the current, a smaller SiC area is required for circuit operation.

For lower load currents, the MOSFET conducts a larger portion of the current, and the higher its nominal current, the larger this portion becomes. This occurs because the IGBT has a high resistance for lower load currents (due to $V_{CE,sat}$), and the higher the nominal current of the MOSFET, the lower its resistance.

It is possible to observe that using a SiC-MOSFET with a lower nominal current than a Si-IGBT is feasible for a Hybrid Switch (HyS), since the Si-IGBT will conduct most of the current for larger load currents. This is important because it helps to reduce the cost of the HyS by minimizing the SiC area. However, it is important to note that the SiC-MOSFET needs to have a minimum nominal current value

to handle most of the current during switching intervals, as will be further discussed in the next subsection.

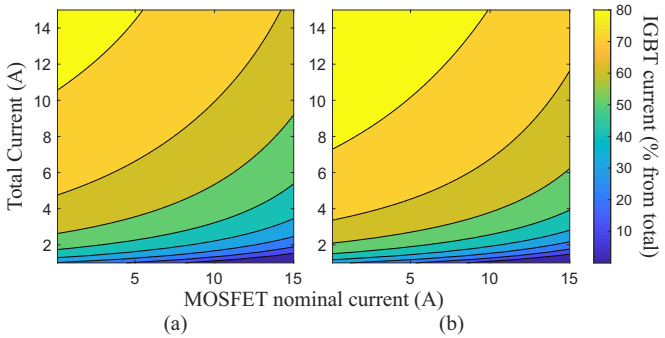

FIGURE 6. Percentage of the total circuit current flowing through the IGBT during the conduction period with a nominal current of (a) 15 A and (b) 25 A. Condition: $T_{vj} = 150$ ℃. Results were obtained using PLECS software.

III. SWITCHING PERIOD

Modeling the HyS switching transient presents challenges. A widely used approach to verify behavior and assess losses is the double-pulse test (DPT). Figure 7 presents a simplified schematic of the DPT circuit with two hybrid pairs. The trigger signals of pairs Q1 and Q2 are complementary. Initially, Q2 goes into conduction while the diode in the Q1 structure is blocked. Then, Q2 turns off, the diode present in the structure Q1 starts conducting.

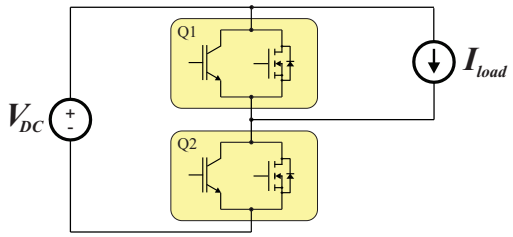

FIGURE 7. Schematic of the DPT with two HyS.

Throughout the DPT simulation in LTspice considering the switching pattern II of Figure 4, some unwanted transient phenomena are observed. The cause of such behavior and possible solutions to be adopted are discussed in this section, since neglecting such phenomena can lead to worse performance of the HyS or even make it unfeasible. The analyses are conducted for a HyS composed of the Si-IGBT (IGW15T120-Infineon) of 15A and the SiC-MOSFET (IMW120R220M1H-Infineon) of 13A.

A. Turn-off

As the SiC-MOSFET turns-off rapidly, it causes a high dv/dt between the IGBT collector and emitter. Due to the miller capacitance, current flows to the IGBT gate and causes a momentary turn-on of the IGBT, as shown in Figure 8 (a). This phenomenon was verified through experiments in [24] and it has the negative effect of increasing the switching losses of the HyS.

This effect has the negative aspect of increasing the switching losses of the HyS. A common practice to solve this problem is to use a clamping drive circuit (active Miller clamp). This circuit can prevent the IGBT gate voltage (V_{GE}) from increasing during the occurrence of dv/dt, preventing its turn-on. For this, when V_{GE} reaches a defined voltage value, the Miller clamp provides a low impedance current path between the gate and the emitter of the IGBT, bringing this voltage close to zero. The HyS turn-off simulation result using the Miller clamp is illustrated in Figure 8 (b). For the evaluated scenario, a 75% peak value reduction is observed in the IGBT current, demonstrating the method effectiveness.

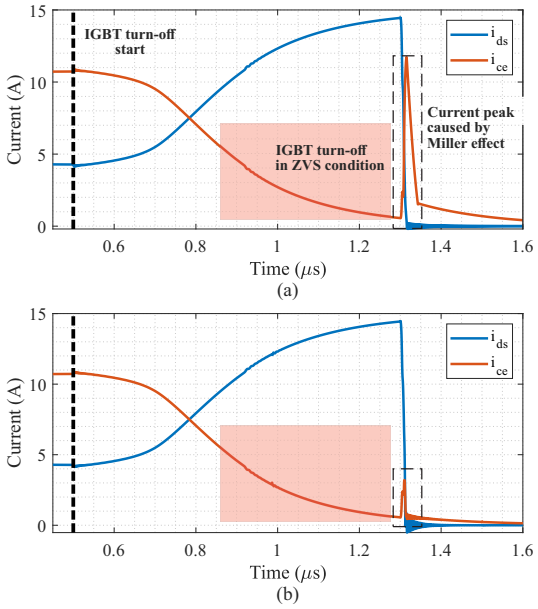

FIGURE 8. Simulation of the HyS turn-off transient composed of a 15 A Si-IGBT and a 13 A SiC-MOSFET. (a) Implementation without the Miller clamp; (b) Implementation with Miller clamp. Conditions: $\mathbf{I_{load} = 15}$ A and $\mathbf{T_{vj} = 150}$ ℃. Results were obtained using LTspice software.

B. Turn-on

The HyS diode choice plays a fundamental role in the viability of the hybrid pair and its performance during turn-on. This is because the reverse recovery current of the diode circulates through the SiC-MOSFET when the hybrid pair turns on. In Figure 9 (a), the simulation of the hybrid switch composed of a Si-IGBT with a silicon freewheeling diode (FWD) shows a current peak in the MOSFET that exceeds the applied load current. This occurs because the IGBT diode has relatively high reverse recovery current (I_{rr}).

Since the selection of the SiC-MOSFET for the HyS has as a figure of merit the smallest possible area, the behavior observed in Figure 9 (a) may make the use of a low current SiC-MOSFET unfeasible. The peak values observed were around 2 times the rated current, exceeding the safe operating area (SOA) of the selected SiC-MOSFET, as analyzed in Appendix VII

The solution adopted was the use of a Si-IGBT without the FWD, so that all the load current returns through the body

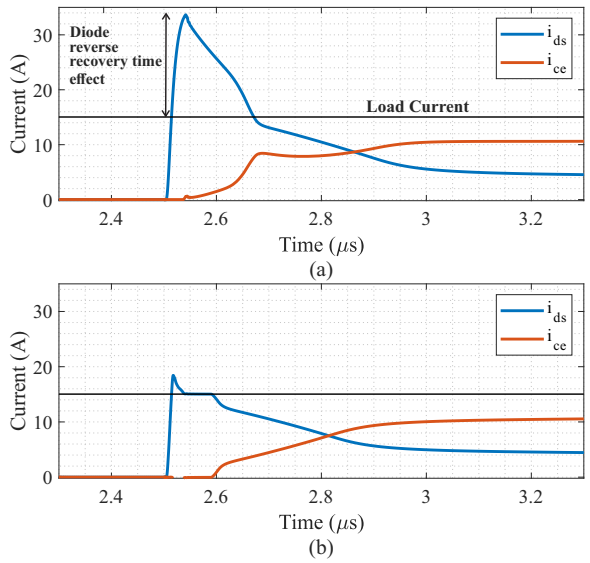

FIGURE 9. Simulation of the HyS turn-on transient composed of a 15 A Si-IGBT and a 13 A SiC-MOSFET. (a) Implementation using IGBT with diode; (b) Implementation employing diodeless IGBT. Conditions: $\mathbf{I_{load} = 15}$ A and $\mathbf{T_{vj} = 150}$ ℃. Results were obtained using LTspice software.

diode of the SiC-MOSFET, which presents a smaller reverse recovery time. Figure 9 (b) shows the turn-on transient for an IGBT without a diode. As observed, this approach reduces the peak current of the SiC-MOSFET to a value close to the rated load current.

C. Switching times

One of the most studied benefits of using the HyS is the reduction in losses compared to Si-IGBTs, particularly during the switching period. To quantify the energy dissipated during turn-on and turn-off events, the voltage drop and current through the devices must be integrated over the switching period, as described by the following equations:

$$E_{on,igbt} = \int_{t_1}^{t_2} v_{CE}.i_{CE}.dt, \tag{1}$$

$$E_{on,mosfet} = \int_{t_1}^{t_2} v_{DS}.i_{DS}.dt, \tag{2}$$

$$E_{off,igbt} = \int_{t_3}^{t_4} v_{CE}.i_{CE}.dt, \tag{3}$$

$$E_{off,mosfet} = \int_{t_3}^{t_4} v_{DS}.i_{DS}.dt. \tag{4}$$

Since the HyS combines two different devices and datasheets do not specify integration periods for HyS, this paper proposes the following integration periods based on common datasheet values [25]:

Turn-on:

- t_1: IGBT gate voltage (v_{GE}) reaches 10% of its steady-state value.
- t_2: IGBT gate voltage (v_{GE}) reaches 80% of its steady-state value.

Turn-off:

- t_3: IGBT gate voltage (v_{GE}) reduces to 90% of its steady-state value.
- t_4: IGBT collector current (i_{CE}) reaches 1% of its steady-state value.

Figure 10 illustrates an example of identifying these switching times. The proposed integration period closely matches the definitions in the Infineon Technologies Si-IGBT datasheet [25], except for t_2. The datasheet suggests stopping the turn-on integration when the collector-emitter voltage (v_{CE}) reaches 3% of its steady-state value. This point is denoted as t_2' in Figure 10. However, with HyS, due to the rapid turn-on of the SiC-MOSFET, this condition is met quickly, often before the IGBT current stabilizes. Thus, this paper proposes a new condition to fully capture the transient behavior of the components, when the currents in the HyS devices are nearly stable. We should highlight that approach lead to higher switching losses when compared with the common definition. However, this is important to guarantee a fair comparison of the HyS with other approaches.

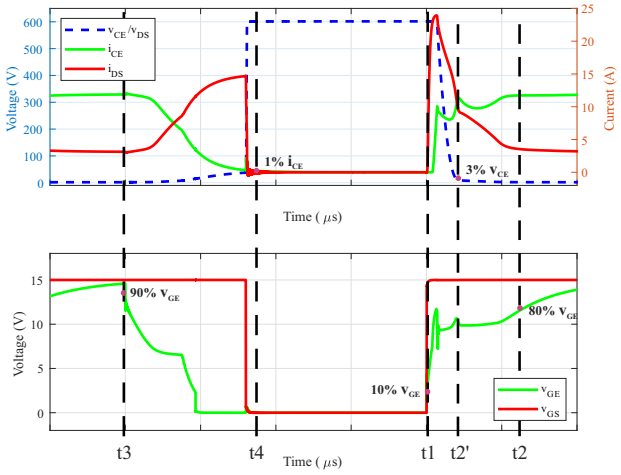

FIGURE 10. Example of integration period determination to calculate the energies for Si-IGBT and SiC-MOSFET in a HyS.

IV. DIODE BEHAVIOR ON CONDUCTION AND SWITCHING TIMES

As seen in the previous section, the adoption of an IGBT with or without the FWD affects the peak current on the SiC-MOSFET during turn-on. However, to assess the power losses in the DPT shown in Figure 7, it is also important to analyze the behavior of the diodes.

Figure 11 (a) shows the gate pulses for the transistor pairs Q1 (Top HyS) and Q2 (Bottom HyS). For turn-on, the pulse represents the gate signals sent to both MOSFET and IGBT, i.e., G_{IGBT} and G_{MOSFET} in Fig. 4. For turn-off, this pulse represents G_{MOSFET}, since the HyS is commanded following the pattern II of Fig. 4. As observed, a dead-time of 200 ns is assumed in this simulation.

In the interval where the bottom HyS turns off, the load current should pass through the diodes of top HyS. The

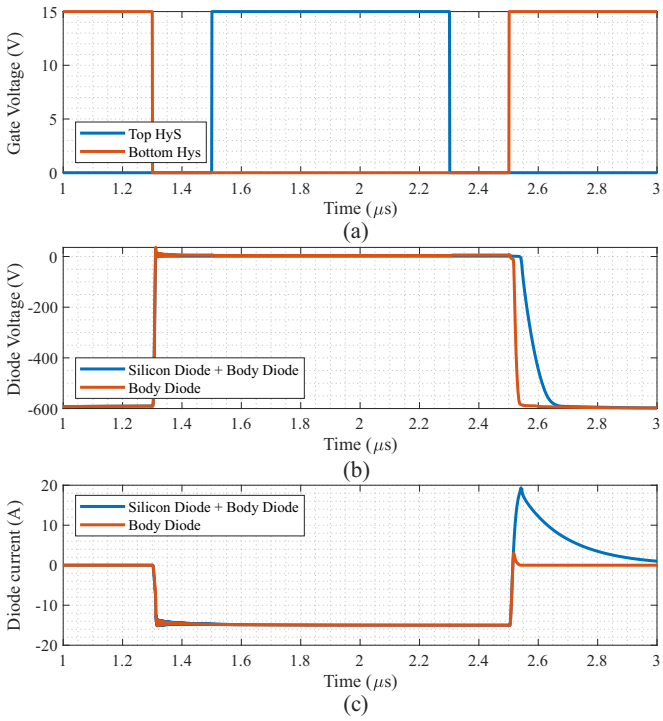

FIGURE 11. Diode's behavior: (a)gate voltage of the power transistors. (b) Diodes voltage drop. (c) Diodes current flow. Conditions: $I_{load} = 15$ A and $T_{vj} = 150$ °C. Results were obtained using LTspice software.

voltage and current across pair Q1 are shown in Figure 11 (b) and (c), respectively. The results are shown for two scenarios:

1) HyS using an IGBT without diode. In this case, the body diode of the SiC MOSFET is the FWD;
2) HyS using an IGBT with diode, where the FWD is an association between the silicon diode and MOSFET body diode.

The voltage and current values are negative because they were measured from the cathode to the anode of the diodes (V_{KA} e I_{KA}). As observed in Figures 11 and 12, during conduction, the voltage amplitude across the diodes decreases, and the current increases. During the turn-on of Q2, the voltage across the diodes for the IGBT with the FWD increases more slowly due to the longer reverse recovery time of the silicon diode. Furthermore, as previously mentioned, this diode generates a higher reverse current, resulting in larger current spikes to the SiC-MOSFET in the bottom HyS.

Due to the switching characteristics of the silicon diode in the IGBT, the use of an IGBT without a FWD becomes more suitable for implementing a HyS. However, the voltage drop across the SiC-MOSFET body diode is more significant than that of the silicon diode in the IGBT with a higher nominal current, as shown in Figure 12. This is expected since the MOSFET body diode is a PIN diode. Due to the lower mobility of holes in SiC, bipolar devices based on this material, such as PIN diodes, tend to have higher on-state voltage drop.

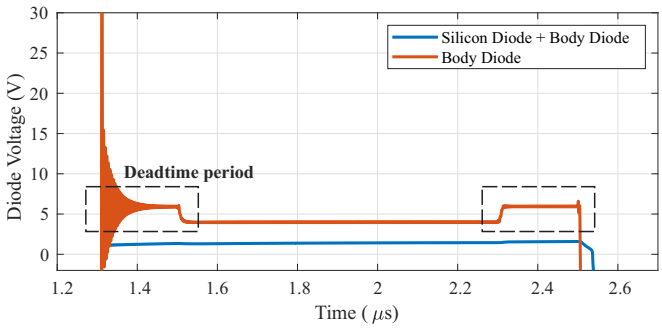

FIGURE 12. Zoomed view of Fig. 11 b. highlighting the deadtime period and diode voltage drop across the hybrid pair for the IGBT with and without FWD.

As observed, for the HyS with the IGBT without FWD, there is a larger transient during the conduction of the SiC-MOSFET body diode. The direct voltage drop across this body diode is also higher compared to the silicon diode. However, when the SiC-MOSFET in the top HyS turns-on, the voltage drop decreases, due to the parallelization of the body diode and SiC-MOSFET channel. Therefore, it becomes interesting to reduce the dead time during device switching to minimize power losses across the SiC diode.

V. EXPERIMENTAL EVALUATION

A. Experimental setup

To investigate the HyS switching behaviour, a DPT circuit topology was built and the assembly is shown in Figure 13. The command of each transistor is executed individually, allowing each device to switch at different times. Therefore, two gate drivers capable of activating two transistors each were used. Table 1 displays the components used in the assembly.

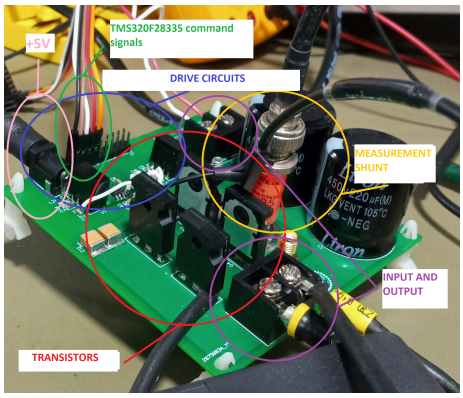

FIGURE 13. Double-pulse test setup built.

Due to limited device availability in the laboratory, a 600V IGBT was used in conjunction with a 1200V SiC MOSFET. In addition, the SiC-MOSFET was selected to ensure that the load current stays within the specified maximum limits during device switching, thus preventing failure. The High and Low Side Gate Drivers can drive IGBTs and MOSFETs in circuits up to 600 V. A 710 μH inductance was used as the

load, and two 220 μF capacitors were connected in parallel to stabilize the DC bus voltage applied to the DPT.

TABLE 1. Transistors and gate drivers for the DPT.

Component	Part Number
SiC-MOSFET 19 A and 1,2kV	IMW120R140M1H
Si-IGBT 60 A and 600V	STGW30NC60KD
Gate Drivers	IR2101STRPBF

The currents passing through the transistors of the Q2 pair, as shown in Figure 7, along with the voltages v_{ce} (v_{ds}) and v_{ge} (v_{gs}) were monitored. The devices were controlled by a LAUNCHXL-F28379D development kit with a TMS320F28379 Digital Signal Controller (DSC). The voltages and currents where measured for the bottom switch (Q2 in Figure 7).

The DPT circuit was tested at three different DC bus voltage levels: 200 V, 250 V, and 300 V. Each voltage level was tested with three different current load values: 10 A, 20 A, and 30 A. The tests also considered the following configurations:

1) Pure IGBT device;
2) HyS with a 0.5μs delay for turning off the SiC-MOSFET relative to the Si-IGBT;
3) HyS with a 1μs delay for turning off the SiC-MOSFET relative to the Si-IGBT.

Current measurement was performed using a PEM AC Current Probe, and the results were visualized and recorded with a Keysight DSOX2014A oscilloscope The integration period for HyS was determined based on the values presented in Section III, while for the single Si-IGBT, the datasheet suggestion was used.

B. Experimental results

To verify the behavior of the devices during switching for each configuration mentioned above, the following waveforms represent the voltages v_{ce}, v_{ge}, and i_{ce} current of the Si-IGBT, as well as the voltages v_{ds}, v_{gs}, and i_{ds} current of the SiC-MOSFET. The results were obtained for a DC-link voltage of 300 V and a load current of 30 A. The areas between the dashed vertical lines defines the integration limits for switching loss computation.

The results shown in Figures 14 and 15 present the waveforms measured for the circuit with the pure IGBT device during turn-off and turn-on, respectively.

Futhermore, during turn-off, the IGBT current decreases more slowly toward the end of the switching period (tail current). This is a negative characteristic of bipolar devices caused by the recombination time of excess charges in the drift region. During IGBT turn-on, the device voltage also reduces more slowly when it reaches low values. This effect is due to the increase in the intrinsic capacitance of the device between the gate and drain terminals ($C_{g,d}$) at low voltages and an accumulation of electrical charges in its drift region during conduction (conductivity modulation).

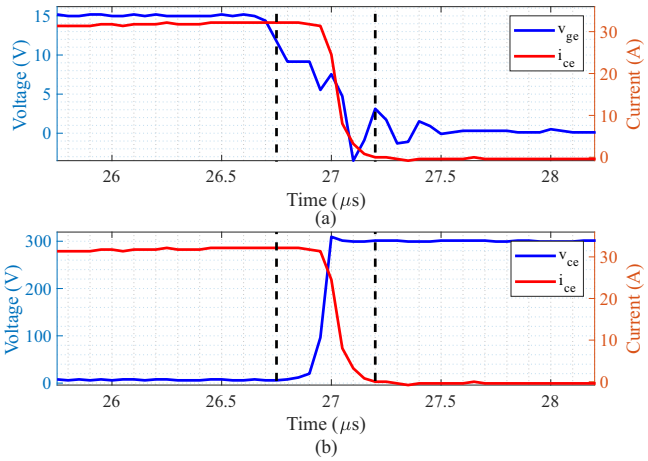

FIGURE 14. Experimental turn-off transient for IGBT: (a) v_{ce} and i_{ce} and (b) v_{ge} and i_{ce}. Conditions: $I_{load} = 30$ A and $V_{DC} = 300$ V.

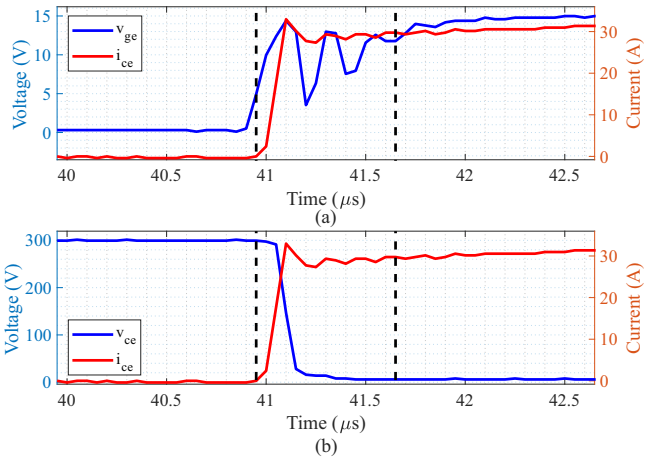

FIGURE 15. Experimental turn-on transient for IGBT: (a) v_{ce} and i_{ce} and (b) v_{ge} and i_{ce}. Conditions: $I_{load} = 30$ A and $V_{DC} = 300$ V.

The IGBT takes approximately 0.5 μs after the turn-off command for its current flow to cease. As shown in Figure 14, around 27 μs, the current i_{ce} and voltage v_{ce} are simultaneously close to their maximum values, implying significant losses during the switching process. For the turn-on event, the IGBT takes approximately 0.2 μs for the nominal circuit current to flow through the device.

Figure 16 shows the waveforms for the HyS tests with a delay of 0.5 μs between IGBT and MOSFET turn-off commands. As can be seen, when deactivating the hybrid switch, the Si-IGBT reaches ZVS, since the voltage over its gate terminal is previously reduced, reducing IGBT losses.

Therefore, the SiC-MOSFET assumes 30 A of load current for 0.5μs. This information is relevant, as the chosen SiC-MOSFET, despite having a lower nominal current, must have a pulsed current limit higher than the maximum load current, to guarantee the reliability of the component. This is one of

the criteria that defines a minimum required silicon carbide area in the HyS.

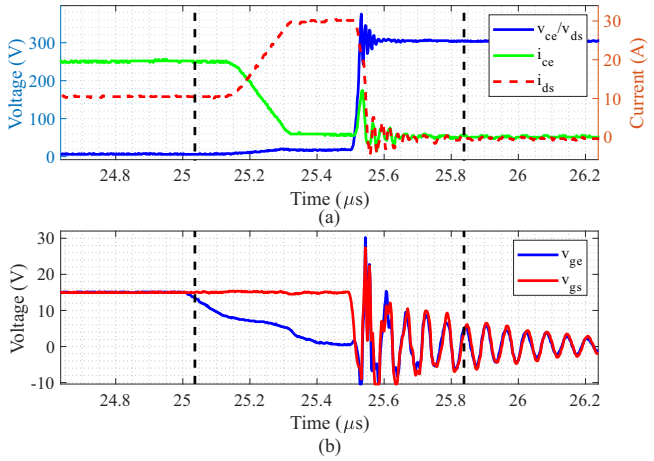

FIGURE 16. Experimental turn-off transient for HyS with a 0.5 μs turn-off delay: (a) voltage drop and current sharing, and (b) gate voltages. Conditions: $I_{load} = 30$ A and $V_{DC} = 300$ V.

Still observing the HyS transient during turn-off, it's noted that the SiC-MOSFET switching is much faster than that of the Si-IGBT, which reduces pair losses. However, it can be observed in Figure 16 that there was an increase in the Ice current and an underdamped oscillation in the gate voltages of the devices in this interval. This occurs because when the SiC-MOSFET turns off, the energy present in the parasitic inductances of the circuit, such as in the printed circuit board traces and component terminals, enters into resonance with the Miller capacitances of the semiconductors. Since the adopted gate driver does not have the Miller Clamp function, discussed in Section III, the voltages at the gate terminals may oscillate during turn-off.

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From Figure 17, it can be seen that it is not necessary to delay conduction of the SiC-MOSFET about the Si-IGBT, since the first switches much faster than the second, reducing the pair losses. Therefore, for a few moments, the SiC-MOSFET must once again assume the entire load current. However, as the voltage v_{ge} of the Si-IGBT tends to increase, the device enters saturation and takes on most of the load current.

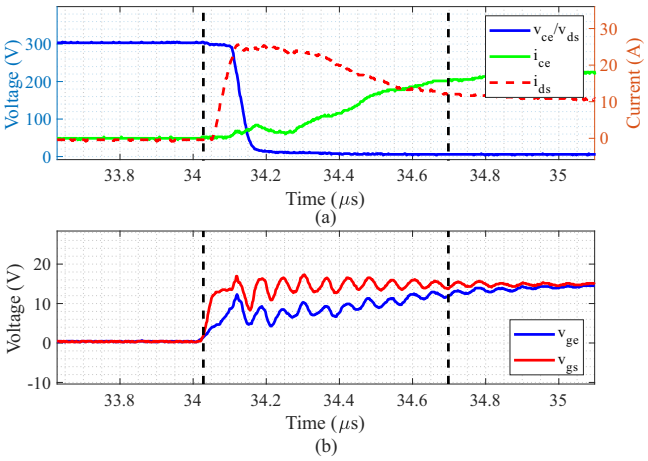

FIGURE 17. Experimental turn-on transient for HyS with a 0.5 μs turn-off delay: (a) voltage drop and current sharing and (b) gate voltages. Conditions: $I_{load} = 30$ A and $V_{DC} = 300$ V.

During the turn-off of the hybrid switch (HyS) with a 1 μs delay for the SiC-MOSFET, the results showed in Figure 18 reveals that there is a peak in i_{ce} current when the SiC-MOSFET turns-off, since the Si-IGBT has been blocked for a longer period. Even during a short interval, the Si-IGBT partially reactivates, suggesting that a gate-driver with Miller clamp is still necessary to minimize pair losses, yet with longer SiC-MOSFET delay intervals. The HyS turn-on process with a 1 μs delay is similar to those with a 0.5 μs delay in Figure 17, as both devices switch at the same time.

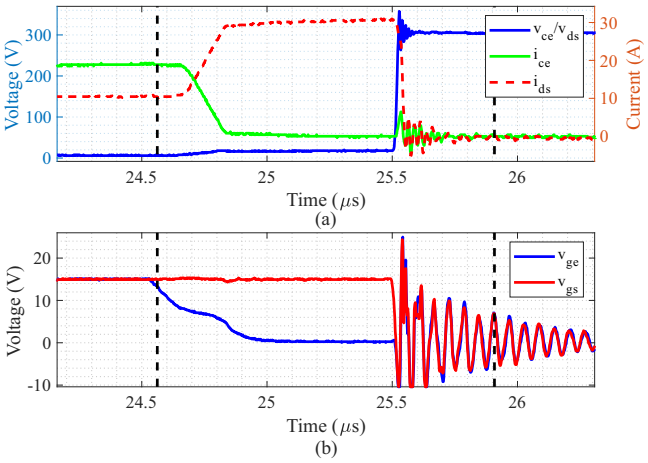

FIGURE 18. Experimental turn-off transient for HyS with a 1 μs turn-off delay: (a) voltage drop and current sharing and (b) gate voltages. Conditions: $I_{load} = 30$ A and $V_{DC} = 300$ V.

Figure 19 shows the switching losses for all tests performed on the DPT with each of the configurations. It is possible to observe that an increase in voltage level and total circuit current results in increased losses for all switch configurations, as expected. The hybrid pair also showed a reduction in switching losses compared to the standalone silicon IGBT, particularly at higher voltage and current levels. It is also noted that the HyS with a 0.5 μs turn-

off delay had better efficiency compared to the same with a 1 μs turn-off delay, since the SiC-MOSFET spent a shorter period conducting the entire load current. For the condition of 30 A and 300 V, the IGBT exhibited losses close to 1500 μJ, while the hybrid pair showed losses of 1150 μJ (1 μs delay) and 940 μJ (0.5 μs delay) under the same conditions, representing a reduction of 22.9% and 37.0% in losses, respectively. Tables 2 presents the percentage loss reduction for both HyS configuration compared to the pure Si-IGBT.

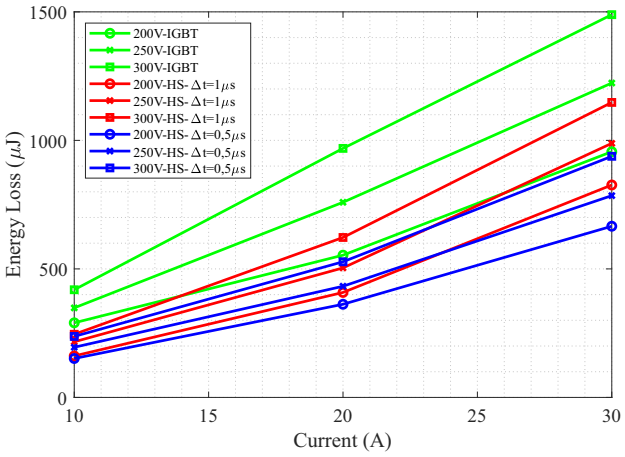

FIGURE 19. Comparison of losses among circuits featuring IGBTs, HyS with 0.5 μs delay, and HyS with 1 μs delay. Results are provided for three levels of DC voltage and three circuit current values.

TABLE 2. Percentage loss reduction: Si-IGBT x HyS for the two delays employed.

	0.5 μs delay			1 μs delay		
	200 V	**250 V**	**300 V**	**200 V**	**250 V**	**300 V**
10 A	47.8	44.0	43.3	44.4	37.9	41.4
20 A	34.5	43.0	45.5	26.2	33.6	35.8
30 A	30.3	35.8	37.0	13.6	19.2	22.9

VI. INSIGHTS

The results and analyses highlight the challenges of obtaining a cost-effective hybrid switch. At this point, some insights can be drawn.

Regarding the gate driver, several pulse patterns can be employed, with pattern II in Figure 4 commonly providing the best efficiency for HyS. The use of a single gate-driver circuit could be interesting for cost reduction, however, the use of two gate drivers makes it possible to operate different HyS efficiently, since it is feasible to change the delay time between device switches. Futhermore, Miller Clamp is especially important to avoid the accidental IGBT turn-on during HyS turn-off.

Also, the diode technology plays an important role in the HyS performance. For example, the SiC body-diode presents better performance during switching. However, in the conduction period, this diode performs worse than its silicon counterparts. A possible investigation is the inclusion of a SiC Schottky diode in the HyS. In this case, the switching and conduction performances could be balanced. However, the inclusion of this diode increases the HyS cost.

From the cost point of view, the use of a minimum SiC area is beneficial. The provided results indicate that the minimum SiC area is strongly dependent on the turn-on and turn-off transients. Ideally, the MOSFET should be capable of handling the whole load current while the IGBT performs soft switching. However, the results also show that the MOSFET should not be chosen only based on its nominal current, but also based on its peak current capability.

To analyze the costs related to the assembly used in the experimental evaluation, the prices of the components listed in Table 1 were collected, in addition to a SiC-MOSFET with a nominal current that supports the maximum value of the evaluated circuit: C3M0075120D with 32 A. This survey allows the comparison of costs involving the switch and gate driver assembly for the configurations with pure IGBT, HyS, and pure SiC-MOSFET under the experimental conditions. The cost values, expressed as a percentage of the HyS cost, for quotations from two different electronic component suppliers, are presented in Table 3.

TABLE 3. Assembly cost comparison [5], [26].

Topology	**Devices + Gate drivers**	**Cost (%) - Mouser**	**Cost (%) - Digikey**
HyS	**2 - IR2101STRPBF** **1 - STGW30NC60KD** **1 - IMW120R140M1H**	100	100
Full Silicon	**1 - IR2101STRPBF** **1 - STGW30NC60KD**	44.15	49.83
Full SiC	**1 - IR2101STRPBF** **1 - C3M0075120D**	131.10	117.81

The results presented in Table 3 reveal that, compared to the pure Si-IGBT, the HyS assembly resulted in a price increase due to the inclusion of an additional gate driver and a SiC-MOSFET with a nominal current lower than the total circuit current value. In comparison to the full SiC approach, the HyS showed an average cost reduction of 24.46%.

It is important to note that the comparison considers the use of two packages for the HyS assembly, since discrete devices were assumed, as well as two gate drivers. This leads to the conclusion that the development of a HyS with a single encapsulation and only one gate driver would result in even more competitive solution. It is also observed that, as shown in Figure 1, the cost curve of the SiC-MOSFET has a higher slope, indicating that its price increases significantly for higher nominal currents. Thus, the HyS can become an economically viable alternative for these conditions.

Ultimately, summarizing the various aspects covered in the this paper, selecting a viable HyS for an application involves the following steps:

1) Devices must have the same blocking voltage, and its value must be consistent with the converter topology.

It is important to take into account the presence of parasitic inductances.

2) The IGBT must have a nominal current compatible with the application current, as it will conduct most of the circuit's current during the conduction period.
3) If the application does not require a bidirectional current capability, an IGBT without anti-parallel diode should be selected. This choice contributes to reduce the HyS cost.
4) For the SiC MOSFET, the peak drain current rating must be higher than the application current, as this device will conduct most of the current during switching.
    a) When selecting the SiC MOSFET, keep in mind that parasitic capacitances and inductances can increase the peak current experienced by the device during turn-on.
    b) If the HyS is bidirectional, take the reverse recovery time of the diode into consideration when choosing the SiC MOSFET.
5) Adopt switching pattern II (Figure 4), as it reduces IGBT switching losses and subsequently the losses in the HyS.
6) Employ gate drivers with a active Miller clamp feature to minimize IGBT reactivation during the SiC MOSFET's turn-off. Two approaches can be taken for gate drivers:
    a) Use a single gate driver for both semiconductors, which aims to reduce costs.
    b) Use a separate gate driver for each device. This allows for the adjustment of switching intervals between the semiconductors, promoting better thermal balance and increasing the reliability of the HyS.
7) Determine the switching times of the devices that will yield the best efficiency or thermal balance for the semiconductors under nominal operating conditions.
8) Establish a thermal design for the hybrid switch to test at a specified switching frequency for power converter operation at nominal power or under a defined drive pattern.
9) During testing on prototypes of the power converter, make one of the following decisions:
    a) If some semiconductors experience thermal stress that exceeds their limits, select a semiconductor with a higher nominal current and repeat the previous steps or redesign the thermal configuration.
    b) If the semiconductors in the hybrid switch operate within their specifications, repeat the previous steps using devices with a lower nominal current to optimize the cost of the HyS.
10) Finally, evaluate the overall cost of the hybrid switch to determine whether it is lower than that of a SiC MOSFET with a nominal current equal to that of the IGBT to justify its adoption.

VII. CONCLUSION

This paper investigates the behavior of the Si-IGBT/SiC-MOSFET hybrid pair during conduction and switching periods. During transients, phenomena resulting from the interaction of the hybrid switch devices were observed, which can lead to worse performance or even make its application unfeasible.

For a more reliable hybrid switch implementation, gate drivers with Miller clamp prevented the Si-IGBT from being turned on during the HyS turn-off, while the adoption of diode-free Si-IGBT made it possible to reduce the reverse recovery effect in the turn-on of the HyS, decreasing the peak current to values within the safe operating region of the MOSFET. The results obtained in a DPT circuit demonstrate the greater efficiency of a HyS compared to a pure Si-IGBT device, in addition to demonstrating that the variation of the SiC-MOSFET turn-off delay is relevant to maximize the switch's efficiency.

To deepen the development of HyS, future efforts should focus on modeling techniques that enable the selection of the SiC-MOSFET with the lowest nominal current for a specific Si-IGBT and circuit current. Additionally, it would be crucial to implement and analyze the limits of a power converter using HyS as a significant step toward making the technology a commercially viable option.

APPENDIX A: CURRENT SHARING MODELING DURING THE HyS CONDUCTION PERIOD

This appendix presents the current division model used to evaluate the conduction losses of the HyS. Instead of employing certain part numbers, this work looks for typical values of the devices conduction resistances, allowing to generalize of the results and contributing to future works aiming the optimization of the SiC-MOSFET area.

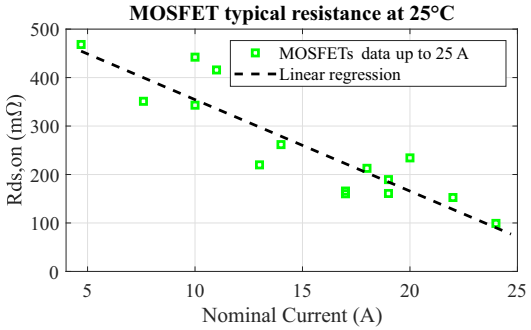

FIGURE 20. R_{ds} **typical data as a function of** 1200 **V MOSFETs' rated currents up to** 25 **A. Affine function with determination coefficient (R²) of** 0.9438**.**

For the MOSFET, the resistance $R_{ds,on}$ is obtained directly from the datasheet and its value is dependent on device parameters. Data collection is performed for MOSFETs from different manufacturers and rated currents, for the

same blocking voltage and TO-247 encapsulation. It allows, through linear regression models, to obtain the typical resistance value of a MOSFET.

Figure 20 shows the collected data mass and the linear regression that allows defining the approximate resistance value of a commercial MOSFET in mΩ, depending on its nominal current as:

$$R_{ds,on} = -26.31 \cdot I_n + 762. \tag{5}$$

The correction of the MOSFET resistance value as a function of the device operating temperature is considered through a correction factor (FC_{mos}), obtained from the datasheet. Figure 21 illustrates the data collected. The correction factor is estimated as:

$$FC_{mos} = 0.00003 \cdot T_{vj}^2 + 0.0002 \cdot T_{vj} + 0.9911. \tag{6}$$

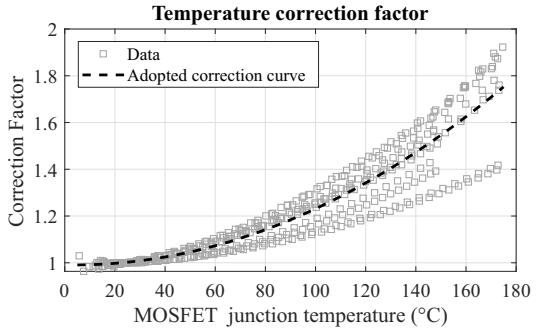

FIGURE 21. SiC-MOSFET conduction resistance correction factor as a function of junction temperature. Adopted curve whose determination coefficient (R^2) was 0.8617**.**

For the IGBT, the conduction resistance value $R_{CE,on}$ is not found in the datasheet but can be obtained through the direct voltage drop graph $V_{CE,sat}$ for different values of instantaneous currents I_{CE} and activation voltages V_{GE}. These IGBT data are obtained for different rated currents and the same blocking voltage.

To obtain the typical IGBT resistance value, the methodology proposed in [27] is used. This methodology consists of normalizing the instantaneous current values by the nominal current of the device, to obtain the typical value of voltage drop V_{CE} for a given normalized current value. Different curves can be obtained for different rated currents, operating temperatures, and applied gate voltages. Thus, IGBT resistance can be estimated by:

$$R_{on} = \frac{V_{CE,sat}\left(\frac{I_{n,igbt}}{I_{CE}}, T, V_n, V_{GE}\right)}{I_{CE}} \tag{7}$$

The collected data includes TrenchStop and FieldStop technology IGBTs manufactured by Infineon Technologies with integrated anti-parallel diode and nominal current up to 40 A and TO-247 encapsulation. As the silicon IGBT is a more technologically mature device, data were collected for only one manufacturer, and significant differences between them are not expected. The same does not occur for the silicon carbide MOSFET, in which its relatively new technology proposes that different manufacturers may have different designs for the device, and therefore, in this case, more data were collected.

Figure 22 presents data collection of voltage drop $V_{CE,sat}$ for different instantaneous currents in pu with voltage V_{GE} =15 V.

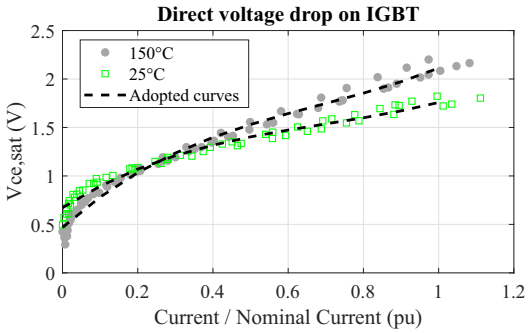

FIGURE 22. Voltage drop across silicon IGBTs. Behavior modeled by a third-degree equation, obtaining a determination coefficient (R^2) of 0.9771 **for 25 ℃ and** 0.9865 **for 150 ℃.**

The curves adjusted in the data of Figure 22 have the following expressions:

$$V_{CE,sat(25C)} = 1.27 \cdot I_{pu}^3 - 2.66 \cdot I_{pu}^2 + 2.47 \cdot I_{pu} + 0.67. \tag{8}$$

$$V_{CE,sat(150C)} = 1.73 \cdot {I_{pu}}^3 - 3.56 \cdot I_{pu}^2 + 3.47 \cdot I_{pu} + 0.47. \tag{9}$$

Different from the SiC-MOSFET, temperature correction is not a simple multiplier factor. To compute the voltage drop for other temperatures, linear interpolation and extrapolation from equations 8 and 9 are adopted.

For the model validation, the pairs presented in Table 4 were simulated in *software* LTspice through its available spice models. The current division result was compared with the simulation using the typical values model. The results presented in Figure 23 prove the adherence of the proposed model.

APPENDIX B: PULSED DRAIN CURRENTS FOR 1200V SiC-MOSFET

The maximum values of current $I_{D,pulse}$ that the MOSFETs support in the transient period were also evaluated. Such information is useful for verifying the supportability of the silicon carbide devices in the hybrid pair during switching periods, since they tend to assume, in theory, the entire circuit current for a short period. Figure 24 presents these values in terms of multiples of the nominal current I_n.

On average, 1200 V silicon carbide MOSFETs support about 2.2 times their rated current value as pulse current,

TABLE 4. Investigates hybrid pairs.

Pair	Device	*Part Number*	In (A)	Supplier
1st	Si-IGBT	IKW15T120	15	*Infineon*
1st	SiC-MOSFET	IMW120R350M1H	4,7	*Infineon*
2nd	Si-IGBT	IGW15T120	15	*Infineon*
2nd	SiC-MOSFET	IMW120R220M1H	13	*Infineon*

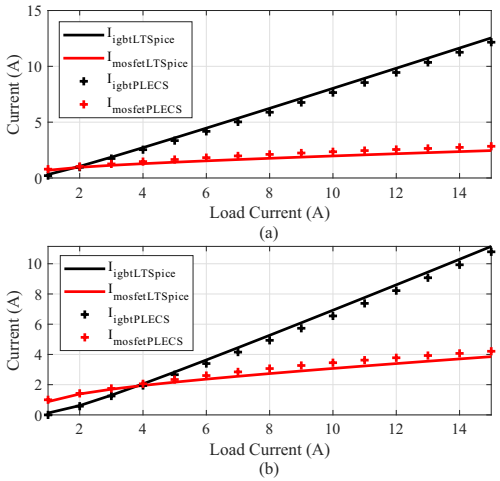

FIGURE 23. Current division in spice models and models obtained for the pair comparison: (a) MOSFET 4.7 A and IGBT 15 A and (b) MOSFET 13 A and IGBT 15 A.

with values ranging from 1.5 and 2.8 times I_n. A device with $I_{D,pulse}$ equal to 2.2 times I_n allows us to roughly conclude that, in order not to exceed the operating limits of the SiC-MOSFET, this device must have at least, rated current equal to 45% of the predicted value for total HyS current. At this point, it is worth mentioning that:

- This estimate does not include the effect of diode reverse recovery, which increases the MOSFET current peak;
- The use of this estimation can be conservative since the current pulse holds for a few microseconds and SiC industry is still improving the surge capability of the MOSFETs.

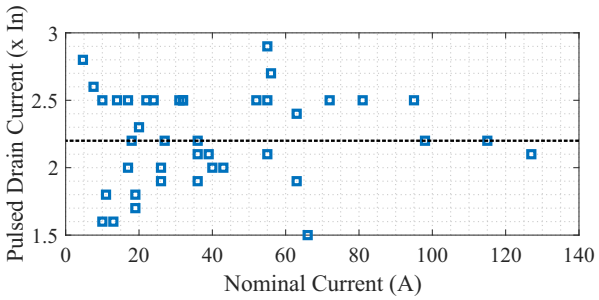

FIGURE 24. Pulsed current data for 1200 V MOSFETs with average value highlighted.

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AUTHOR'S CONTRIBUTIONS

P. H. G. VILELA: Formal Analysis, Investigation, Methodology, Software, Validation, Writing – Original Draft. **E. F. COTA**: Data Curation, Formal Analysis, Methodology, Software, Visualization, Writing – Original Draft, Writing – Review & Editing. **H. A. PEREIRA**: Conceptualization, Funding Acquisition, Resources, Supervision, Validation, Writing – Review & Editing. **T. P. CORRÊA**: Data Curation, Funding Acquisition, Investigation, Methodology, Software, Supervision, Writing – Review & Editing. **A. F. CUPERTINO**: Conceptualization, Project Administration, Resources, Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

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