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48 V to 1 V DC-DC Converter Based on Cascade/Ladder Connected Switched Capacitor Cells

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ABSTRACT This paper proposes a cascade/ladder switched capacitor converter integrated with an interleaved synchronous buck converter to provide a 48 V to 1 V conversion for data center applications. The switched capacitor stage decreases the input voltage from 48 V to 3 V (a reduction of 16 times), with low voltage stress on the input switches and intermediate voltage levels that can be used as voltage sources. The interleaved buck stage provides voltage and current control and is connected in cascade with the switched capacitor stage to reduce the voltage from 3 V to 1 V (a reduction of 3 times). Furthermore, a switching frequency optimization is proposed for the switched-capacitor converter to maximize efficiency. The proposed solution was experimentally validated in a two-stage 30 W prototype: the first stage is the proposed cascade/ladder switched capacitor topology (48 V to 3 V) with unregulated conversion, which provides a maximum efficiency of 91,6%, and the second stage is the buck converters (3 V to 1 V) with regulated conversion.

KEYWORDS Non-Isolated DC-DC Converters, Step-down converter, Switched-capacitor cell.

I. INTRODUÇÃO

In recent years, there has been an increase in the use of high-gain DC-DC step-up and step-down converters. These converters are essential for applications such as data centers [1]-[2], renewable energy sources [3], electrical vehicles [4], and storage systems [5]. Achieving high efficiency in these converters poses a challenge due to the high input voltage and output current in step-down converters and the high input current and output voltage in step-up converters [6].

Data center systems often require conversion ratios as high as 400 V to 0.8 V [2], [7], making it difficult to achieve good efficiency. To enhance efficiency, recent solutions propose multiple conversion stages, with one stage converting from 400 V to 48 V, and another stage converting from 48 V to 3.3 V – 0.8 V. Solutions for the first case typically involve isolated converters such as the dual active bridge (DAB) or resonant LLC converters [8]. For the second stage (48 V to 3.3 V~0.8 V), named Point of Load (POL) converters or Voltage Regulator Modules (VRM), different solutions are found in the literature, including LLC [9 – 10], half-bridge [10 – 11], buck converter variations [10], and converters with gain cells like the switched capacitor (SC) converters [10, 12-15]. The power levels range from units to hundreds of watts [10]. One of the biggest challenges is the higher output current values, which lead to low efficiencies and the use of converters or devices in parallel.

Solutions using transformers or inductors often suffer from low efficiency due to core losses, leakage inductance, and larger physical size [13]. On the other hand, switched capacitor solutions offer better efficiency when compared to transformer/inductor-based solutions, but they present challenges in voltage control [16]-[17]. Furthermore, switched capacitor cells are versatile and can be connected in a ladder, cascaded configuration, or a combination of both, to increase gain [18].

This paper proposes a two-stage solution for converting 48 V to 1 V for data center applications. The first stage consists of a mixed switched capacitor converter (MSSC) operating in an open-loop configuration, connected in cascade with the second stage, which is an interleaved synchronous buck converter (ISBC) [19]-[21] operating in a closed-loop configuration.

The first stage is responsible for the majority of the output voltage reduction (48 V to 3 V) and is the main contribution of this paper. It provides a high step-down gain and a low voltage value for a second stage to operate with an adequate duty cycle. The MSCC structure was proposed in [18] but was not validated experimentally. This study aims to verify experimentally and proposes a frequency optimization approach to maximize the efficiency of MSCC converter. The second stage (buck) is well-known in the literature, and further decreases the voltage (3 V to 1 V) and controls the output voltage. This control is particularly challenging in solutions based on switched capacitors. Additionally, the interleaving technique [20]-[23] allows the current division among components, increasing the efficiency of converters with high currents and low voltages. These converters

exhibit reduced input current and output voltage ripple, significantly reducing the size of the input and output filter capacitors [22].

This paper's main contribution lies in the introduction, analysis, and verification of the MSCC, briefly proposed in [18]. The study approaches a detailed analysis of the proposed mixed-switched capacitor converter (MSCC), the cascaded connection between an MSCC topology and a three-phase interleaved synchronous buck converter to reach a gain from 48 to 1V, an optimization method to determine the switching frequency that maximizes the efficiency of converters, a closed-loop operation to provide a 1 V regulated output voltage, design and build of prototypes, and experimental validation.

In addition to this introduction section, Section II presents the derivation of the proposed converter, Section III presents the static analysis and optimization of the MSSC to increase efficiency, and Section IV discusses the ISBC topology. The experimental results are presented in Section V, and finally, Section VI summarizes the conclusions.

II. PROPOSED CONVERTER DERIVATION

The proposed converter consists of a mixed (cascade and ladder) switched capacitor converter (MSCC) and a three-phase interleaved synchronous buck converter (ISBC), connected in a cascaded configuration, as shown in Fig. 1.

The MSCC is derived from a step-down version of the switched capacitor cell [24], as presented in Fig. 2. When all the switches are appropriately controlled, the converter operates bidirectionally.

A comparison is presented in [18] among the ladder, cascade, and mixed connections for high step-down applications. With the same number of switches, the mixed connection exhibits a higher voltage gain than the ladder connection while subjecting the switches to less voltage stress than the cascade connection. However, the MSCC was not validated experimentally, and its performance was unavailable.

The comparison demonstrates that, for the same number of switches, the cascade connection provides higher voltage gain and requires fewer capacitors than the ladder connection. However, it incurs more voltage stress on the components. The mixed connection offers the same voltage gain as the cascade connection but with reduced voltage stress and higher efficiency. Therefore, it is a suitable choice for high-gain applications, and this is the connection proposed in this paper. It is important to highlight that each stage of the switched capacitor cell operates independently and can have different components and switching frequencies.

The ISBC topology is derived from the traditional buck converter. This topology has been proposed in other papers [19]-[23] with the objective of increasing efficiency. The interleaving technique [20] employed in these converters allows the current division among the components, resulting in improved efficiency for converters with high currents and low voltages.

Furthermore, these converters effectively cancel input current and output voltage ripples, significantly reducing the size of the input and output filter capacitor [22]. In this paper, the ISBC is responsible for decreasing and controlling the output voltage with high efficiency.

III. MIXED SWITCHED CAPACITOR CONVERTER

A. *STATIC GAIN*

Considering the continuous conduction mode (CCM) and the complementary nature of the command pulse v_{g2} to v_{g1} (see Fig. 1), the three ladder-connected cells at the input provide a ¼ voltage gain while distributing the voltage stress among the components. The remaining stages are cascade-connected, resulting in an exponential increase in gain with a relation 2^N. Thus, the generalized gain of MSCC converter (G_{MSCC}) is given by (1), where N is the number of cascades connected stages.

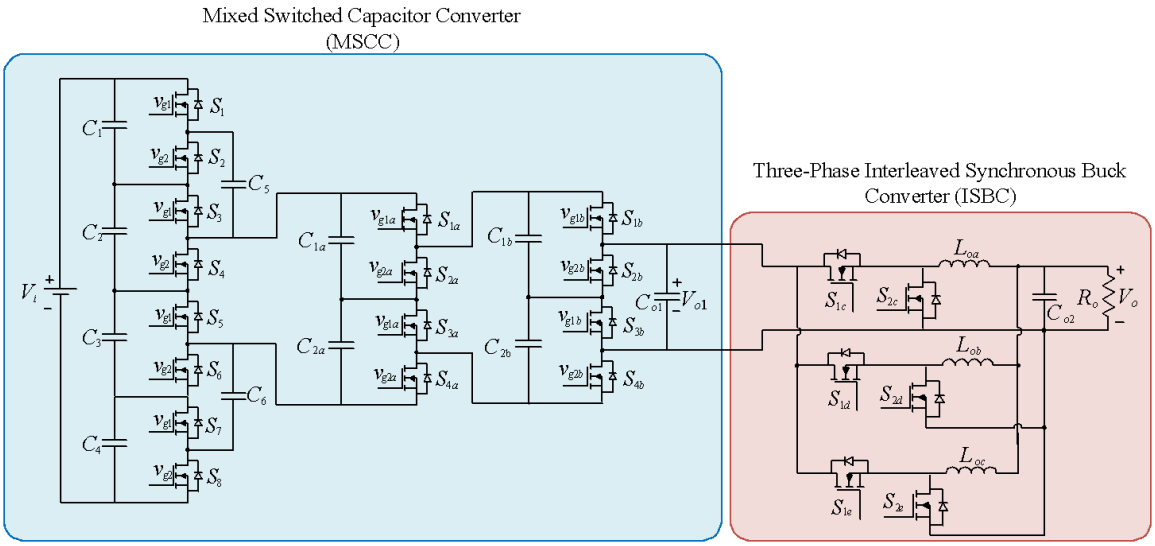

FIGURE 1. Proposed converter: cascaded connection between a mixed switched capacitor and a three-phase interleaved synchronous buck converter.

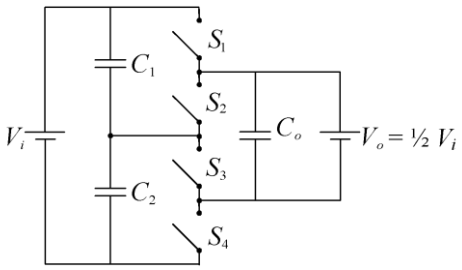

FIGURE 2. The step-down version of the ladder-switched capacitor cell [20].

$$G_{MSCC} = \frac{V_{o1}}{V_i} = \frac{1}{4}\frac{1}{2^N} \quad (1)$$

The proposal topology has $N = 2$, thus the static gain is given by (2).

$$G_{MSCC} = \frac{V_{o1}}{V_i} = \frac{1}{4}\frac{1}{2^2} = \frac{1}{16} \quad (2)$$

More cascaded cells can be added in the topology and the resulting converter is exposed in Fig. 3.

B. *SWITCHED CAPACITOR DESIGN*

There are various approaches to designing switched capacitor converters, and the one utilized in this paper is presented in [25]. It is based on analyzing current capacitor peaks during charge and discharge cycles in steady-state, which can assume three different operation modes.

The first mode is the complete charge mode (CC), where the capacitor discharges completely within one operational stage, causing the current to reach zero, as illustrated in Fig. 4 (a).

The second mode is the partial charge mode (PC), where the capacitor only partially discharges within one operational stage, as shown in Fig. 4 (b). In this mode, the current varies but does not reach zero.

Lastly, the third mode is the no-charge mode (NC), where the charge in the capacitor remains virtually unchanged, resulting in a constant current within one operational stage, as depicted in Fig. 4 (c).

The CC mode leads to high peak currents and conduction losses, while the NC mode requires high capacitances and frequencies, making it expensive and leading to high switching losses. Therefore, the converter is typically designed to operate in the PC mode.

To design the converter, the analysis considers a 0.5 duty cycle, all capacitors with the same capacitance, and all switches with the same resistance. Opting for the same switches and capacitors simplifies the design process, as it ensures a consistent time constant across the entire circuit.

The time constant (τ) of the circuit is given by (3):

$$\tau = CR_s \quad (3)$$

where C is the capacitance, and R_s is the equivalent series resistance, which can be calculated by (4).

$$R_s(f_s\tau) = \frac{2R_{on}}{f_s\tau}\frac{1 - e^{-\frac{1}{f_s\tau}}}{1 + e^{-\frac{1}{f_s\tau}} - \left(e^{-\frac{D}{f_s\tau}} + e^{-\frac{D}{f_s\tau}}\right)} \quad (4)$$

where R_{on} is the switch resistance, D is the duty cycle, and f_s is the switching frequency.

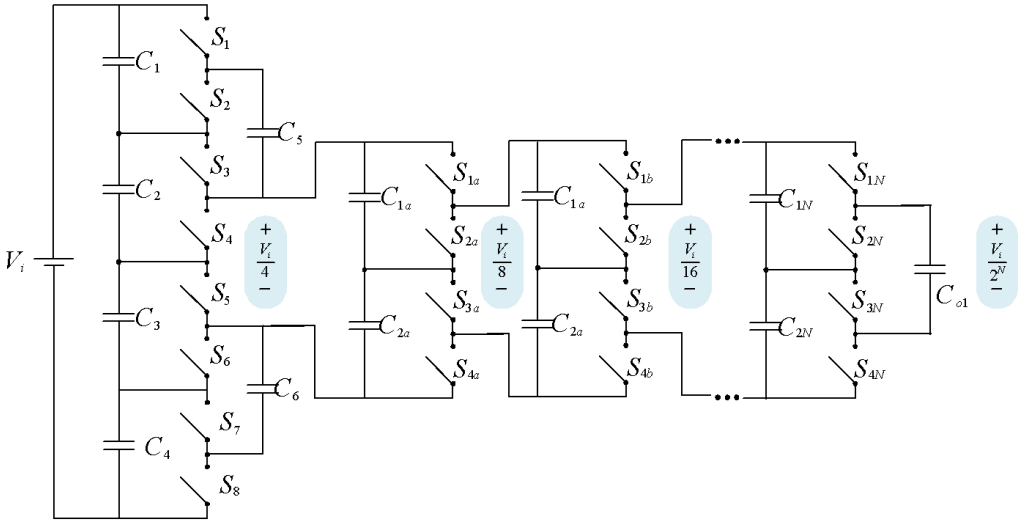

FIGURE 3. Generalized MSCC.

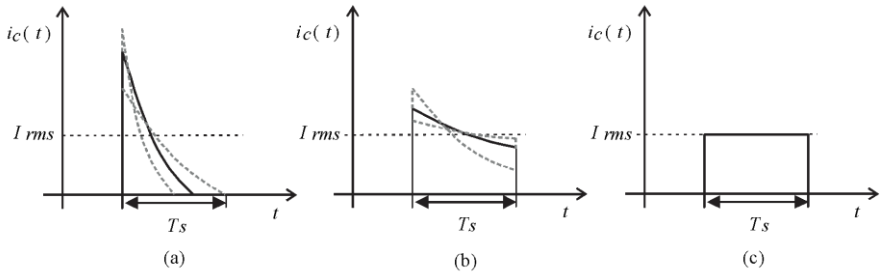

FIGURE 4. Switched capacitor modes: (a) complete charge, (b) partial charge, and (c) no charge.

Normalizing (4) in function of $f_s\tau$ is obtained (5), which is graphically presented in Fig. 5.

$$\underline{R_s(f_s\tau)} = \frac{R_s(f_s\tau)}{2R_{on}} \tag{5}$$

Upon observing Figure 5, it can be noted that the CC mode occurs until $f_s\tau = 0.1$, with high resistance in this situation. Between $f_s\tau = 0.1$ and $f_s\tau = 0.5$ lies the PC mode, while for $f_s\tau > 0.5$, the NC mode is prevalent. This relationship can be utilized to design the switched capacitor converter to operate in the PC mode, as follows (6).

$$C \geq \frac{2R_{on}f_s}{f_s\tau} \tag{6}$$

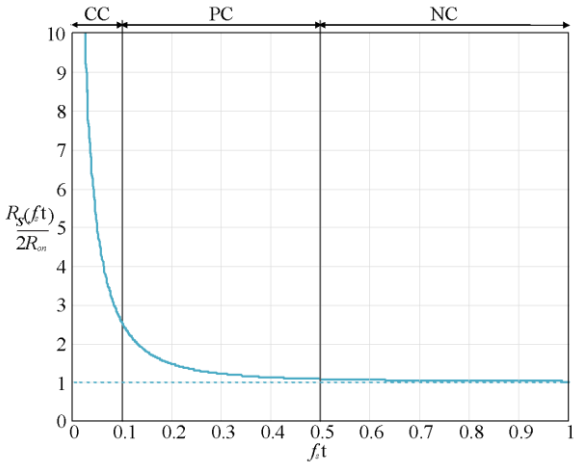

FIGURE 5. Normalized R_s in function of f_s ⎸.

C. *VOLTAGE AND CURRENT STRESSES*

The voltage and current stresses on the switches of the MSCC are shown in Table 1, where I_o is the output current, and P_o is the output power.

TABLE 1. Voltage and Current Stresses on the MSCC Switches.

Switch	Voltage	Average Current	RMS Current
$S_{1,2,3,6,7,8}$	$\frac{V_i}{4}$	$\frac{P_o}{V_i}$	$\frac{2P_o}{\sqrt{2}V_i}$
$S_{4,5}$	$\frac{V_i}{4}$	$\frac{3P_o}{V_i}$	$\frac{6P_o}{\sqrt{2}V_i}$
$S_{1a,2a,3a,4a}$	$\frac{V_i}{8}$	$\frac{I_o}{2^N}$	$\frac{I_o}{2^{(N-1)}\sqrt{2}}$
$S_{1b,2b,3b,4b}$	$\frac{V_i}{16}$	$\frac{I_o}{2^{(N-1)}}$	$\frac{I_o}{2^{(N-2)}\sqrt{2}}$
$S_{1N,2N,3N,4N}$	$\frac{V_i}{2(N+2)}$	$\frac{I_o}{2}$	$\frac{I_o}{\sqrt{2}}$

D. *EFFICIENCY ANALYSIS AND FREQUENCY OPTIMIZATION*

The conduction losses of the switches are given by (7).

$$P_{cd} = R_{on}I_{rms}^2 \tag{7}$$

where R_{on} is the conduction resistance, and I_{rms} is the RMS current of the switch.

The switching losses are given by (8), whereas V_s is the off-state voltage, I_s is the on-state current, t_r is the rise time, and t_f is the fall time.

$$P_{sw} = V_s I_s f_s \left(\frac{t_r + t_f}{2}\right) \tag{8}$$

The losses caused by the intrinsic capacitance charge and discharge are described in (9).

$$P_{sw} = f_s C_{oss} V_s^2 \tag{9}$$

where C_{oss} is the switch output intrinsic capacitance.

It should be noted that the operating frequency significantly impacts the converter losses, as it determines the mode of operation for the switched capacitor and influences the behavior of the current in the cell. Therefore, this paper proposes a frequency optimization approach to maximize efficiency.

To achieve this, it is necessary to express the losses as functions of the switching frequency. The conduction losses in each switch, concerning the frequency, are described by (10), where the normalized series resistance is used as a multiplying factor. Consequently, the total losses as a function of the frequency can be defined in (11), while the efficiency as a function of the frequency is expressed in (12).

Using (12) and the values provided in Table 3, a graph can be plotted to identify the frequency at which maximum efficiency is achieved. In this case, the optimum frequency lies between 70 and 130 kHz, as illustrated in Fig. 6.

$$P_{cd}(f_s) = \underline{R_s(f_s\tau)}R_{on}I_{rms}^2 \tag{10}$$

$$P_{tot}(f_s) = P_{cd}(f_s) + P_{sw}(f_s) + P_{cap}(f_s) \tag{11}$$

$$n(f_s) = \frac{P_o}{P_o + P_{tot}(f_s)} \tag{12}$$

IV. INTERLEAVEAD SYNCHRONOUS BUCK CONVERTER

A. *STATIC GAIN*

Each phase of the interleaved buck converter operates independently, maintaining a 120º phase difference between the gate signals. This configuration demonstrates analogous behavior to a conventional buck converter, and its static gain can be expressed as shown in (13).

$$G_{ISBC} = \frac{V_o}{V_{o1}} = D \tag{13}$$

B. *PASSIVE COMPONENTS DESIGN*

The inductance can be obtained by (14).

$$L_{oa,b,c} = L = \frac{V_{o1}D(1-D)}{\frac{\Delta_{IL\%}I_o}{3}f_s} \tag{14}$$

where V_{o1} is the output voltage of MSCC, $\Delta_{IL\%}$ is a percentage of the output current ripple of ISBC.

The output capacitor in the ISBC is reduced compared to that of a traditional buck converter due to the cancellation of the current ripple achieved through the interleaving technique. It can be designed by (15).

$$C_{o2} = \frac{V_{o1}}{96Lf_s^2\Delta_{Vco\%}V_o} \tag{15}$$

whereas $\Delta_{Vco\%}$ is a percentage of the output voltage ripple of ISBC.

The factors of 3 in (14) and 96 in (15) stem from the ripple cancellation attributes enabled by the three-phase interleaving. This approach minimizes the dimensions of inductors and capacitors when contrasted with those in a conventional buck converter. Furthermore, it reduces the conduction losses resulting from current distribution, with

the trade-off of an increased component count.

C. *VOLTAGE AND CURRENT STRESSES*

The voltage and current stresses of the ISBC switches are approached in Table 2, where I_L is the inductor current.

TABLE 2. Voltage and Current Stresses on the ISBC Switches.

Parameter	$S_{1a,b,c}$	$S_{2a,b,c}$
Peak voltage	V_{o1}	V_{o1}
Average voltage	$V_{o1}(1-D)$	$V_{o1}D$
Average current	I_LD	$I_L(1-D)$
RMS current	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$

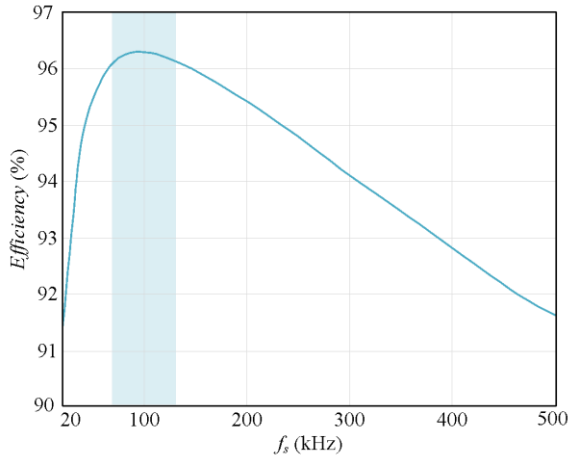

FIGURE 6. Efficiency in function of the switching frequency for 30 W.

D. *CONTROL SCHEME*

The control strategy employed in the converter is based on the classical two-loop averaged control approach used in buck converters. This involves a fast inner loop that regulates the current flowing through the inductors and a slower outer loop that controls the output voltage. Each converter phase has its own current loop and duty cycle, with a 120° phase shift between them.

The output of the voltage controller generates the current reference in correlation with the output current. Notably, the current for each interleaved buck converter constitutes one-third of the load current. Consequently, to accurately generate the current reference, a 1/3 gain is employed at the voltage controller output. A proportional-integral (PI) controller achieves voltage and current regulation. The control diagram is depicted in Fig. 7, and the transfer functions are provided as follows (16)-(19).

$$PI_v(s) = K_{PIv}\frac{s+\omega_{zv}}{s} \tag{16}$$

$$PI_i(s) = K_{PIi}\frac{s+\omega_{zi}}{s} \tag{17}$$

$$G_i(s) = \frac{I_{L(s)}}{D(s)} = \frac{V_{o1}}{sL+R_L} \tag{18}$$

$$G_v(s) = \frac{V_{o(s)}}{I_o(s)} = \frac{1}{sC+\frac{1}{R_o}} \tag{19}$$

The controllers were discretized using the Tustin method, given by (20), where T_s is the sampling period.

$$s = \frac{2(z-1)}{T_s(z+1)} \tag{20}$$

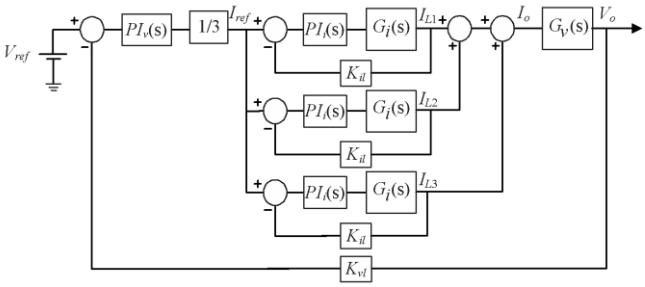

FIGURE 7. Three-phase interleaved synchronous buck converter control scheme.

V. EXPERIMENTAL RESULTS

Two prototypes were developed to validate the proposed topology: one prototype for MSCC providing a 48 V to 3 V conversion, which validated the topology and frequency optimization; a second prototype for the BKSI, to obtain the 3 V to 1 V conversion and the voltage control. The schematics of prototypes are exhibited in Fig. 8, the prototype of the MSCC is shown in Fig. 9 (a), and the prototype of the ISBC in Fig. 9 (b). The vertical boards in the prototypes are the isolated gate drivers. Based on the available devices, the power level utilized in the tests is 30 W to validate the converter theory (1V @ 30A in output voltage and output current). However, it can operate at higher power levels using other devices.

The primary emphasis was on validating the MSCC topology and the frequency optimization. Moreover, an additional objective encompassed achieving a regulated output voltage for the 48 V to 1 V conversion.

The design specifications and components used in the MSCC prototype are detailed in Table 3, and the specifications and components of the BKSI prototype in Table 4. A switching frequency of 80 kHz was employed, being within the frequency range determined by the frequency optimization analysis. Silicon switches with low series resistance (maximum 1.6 mΩ) were chosen, attributable to the substantial current and conduction losses inherent to this specific application.

TABLE 3. Design specifications and prototype components of MSCC.

Parameter	Value
Input voltage (V_i)	48 V
Output voltage (V_{o1})	3 V
Gain (G_{MSCC})	1/16
Output power (P_o)	30 W
Switching frequency (f_s)	80 kHz
$f_s\tau$	0.3
Switches (S_x)	BSC016N06NST 60 V / 234 A
Capacitors (C_x)	KG57NX7S1C107M500JH 100 µF / 16 V (six in parallel)

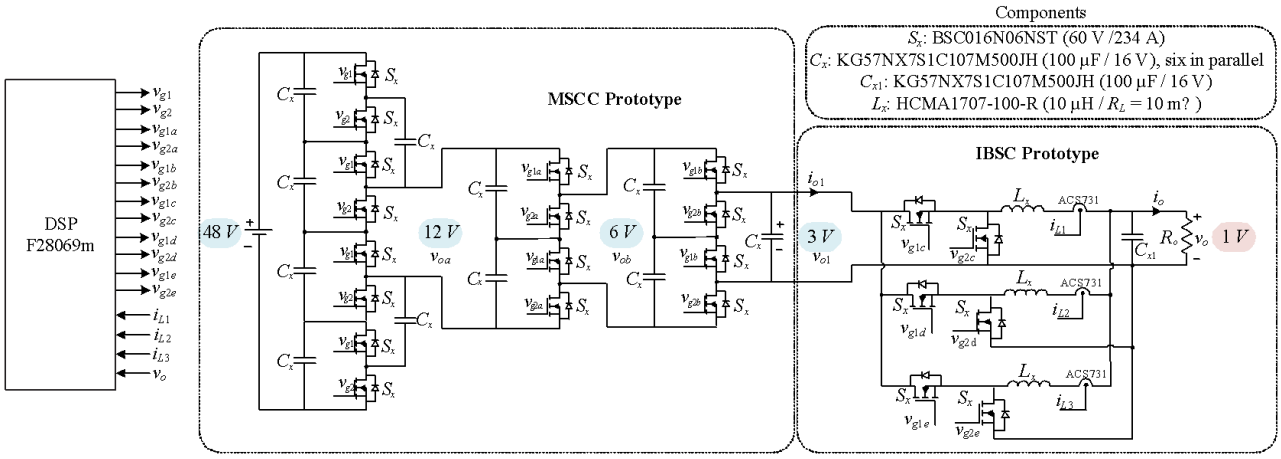

FIGURE 8. Schematics of the prototypes.

The experimental results were obtained by connecting the MSCC and ISBC prototypes in a cascaded configuration, enabling the conversion from 48 V to 1 V.

Figure 10 (a) illustrates the voltage levels across the switches of the MSCC. The ladder stage (v_{S1}) experiences the highest voltage stress at 12 V, which reduces by half in each cascade stage, resulting in 6 V in the cascade stage 1 (v_{S1a}) and 3 V in the cascade stage 2 (v_{S1b}). The phase difference between each stage voltage is also evident due to the 90º phase shift.

Figure 10 (b) displays the output voltages of the ladder stage (v_{oa}), cascade 1 stage (v_{ob}), cascade 2 stage (v_{o1}), and the output current (i_{o1}). These measurements were taken with a 48 V input voltage and a 30 W output power in the MSCC. The output voltage of the ladder stage is one-quarter of the input voltage (12 V), while the output voltage of each cascade stage is half the value of the previous stage (6 V and 3 V).

TABLE 4. Design specifications and prototype components of IBSC.

Parameter	Value
Input voltage (V_{o1})	3 V
Output voltage (V_o)	1 V
Gain (G_{MSCC})	1/3
Output power (P_o)	30 W
Switching frequency (f_s)	80 kHz
Inductor current ripple ($\Delta_{IL\%}$)	10%
Output voltage ripple ($\Delta_{Vco\%}$)	1%
Current loop phase margin	75°
Current loop crossover frequency	1 kHz
Current PI zero frequency (ω_{zi})	2.8 krad/s
Gain PI current (K_{Pli})	0.02
Voltage loop phase margin	90°
Voltage loop crossover frequency	50 Hz
Voltage PI zero frequency (ω_{zv})	1.8 krad/s
Gain PI voltaget (K_{Plv})	5.2
Switches (S_x)	BSC016N06NST 60 V / 234 A
Capacitor (C_{xa})	KG57NX7S1C107M500JH 100 µF / 16 V
Inductors (L_x)	HCMA1707-100-R 10 µH / R_L = 10 mΩ
Digital signal processor (DSP)	F28069m
Current sensors	ACS731

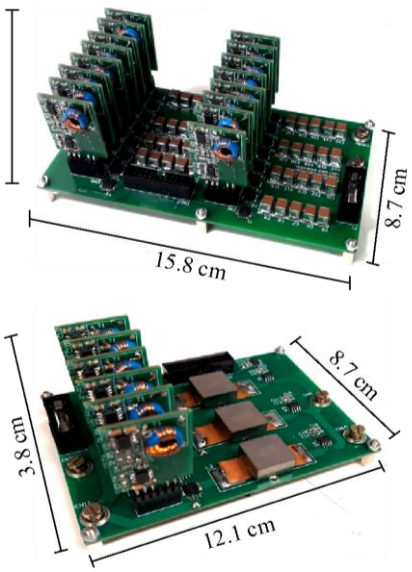

FIGURE 9. Developed prototypes: (a) MSCC and (b) ISBC.

Figure 11 (a) and (b) present the experimental results of the input voltage (V_i), MSCC output voltage (v_{o1}), ISBC output voltage (v_o), and ISBC output current (v_o) at half power (15 W) and rated power (30 W), respectively. It is observed that the voltage v_{o1} changes from 2.82 V to 2.58 V due to the lack of regulation in the MSCC stage. However, the ISBC maintains an output voltage of around 1 V with proper control.

The current control in the ISBC serves two functions: limiting the current in short-circuit situations and maintaining the current balance in the inductors. To validate the latter, experimental results were obtained with the converter in open-loop (Fig. 12 (a)) and closed-loop (Fig. 12 (b)) operations.

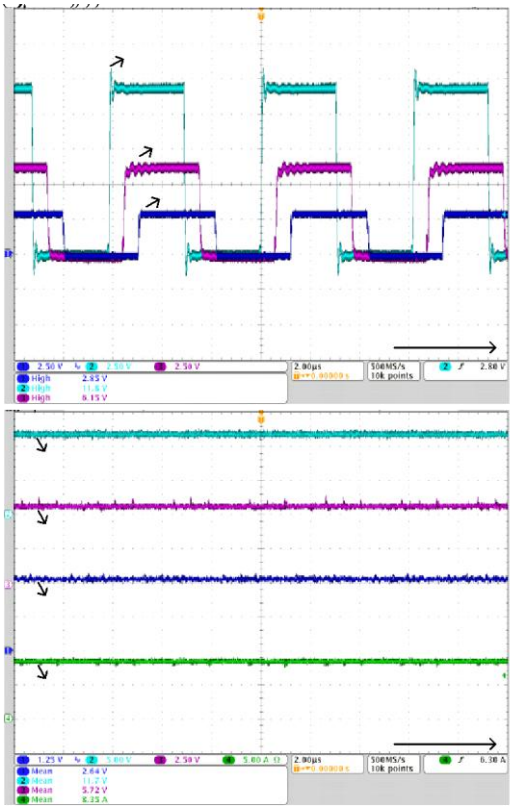

FIGURE 10. Experimental results of MCSS: (a) voltage in the switches of the ladder (v_{S1}), the cascade 1 (v_{S1a}) and the cascade 2 (v_{S1b}) stages; (b) voltage in the output of the ladder (v_{oa}), the cascade 1 (v_{ob}) and the cascade 2 (v_{o1}) stages and the output current (i_{o1}).

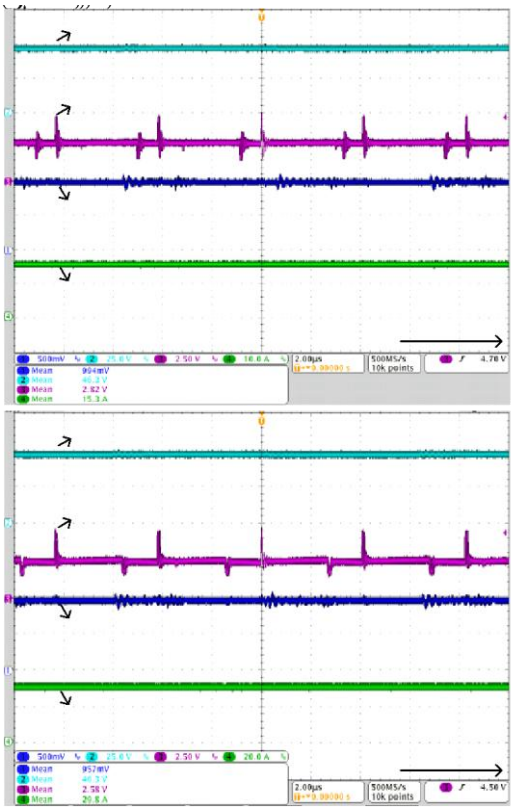

FIGURE 11. Experimental results of entire topology (MSCC + ISBC) – Input voltage (V_i), MSCC output voltage (v_{o1}), ISBC output voltage (v_o), and ISBC output current (i_o): (a) half power and (b) rated power.

In the open-loop scenario, the currents in the inductors are unbalanced. However, in the closed-loop case, the current control ensures that the three inductor currents remain balanced.

Figure 13 (a) shows the input voltage (V_i), MSCC output voltage (v_{o1}), ISBC output voltage (v_o), and ISBC output current (i_o) under a 66% positive load step. In contrast, Figure 13 (b) presents the measurements under a negative load step. In both cases, the output voltage follows the 1 V reference after a transient period.

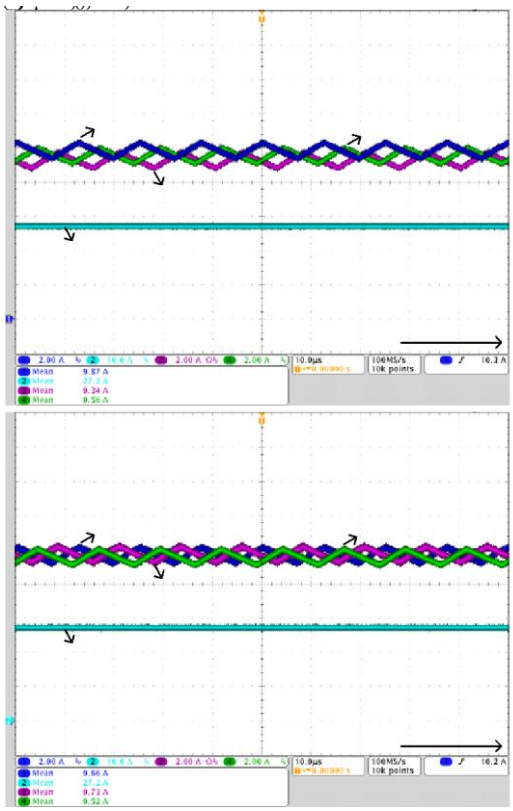

FIGURE 12. Experimental results – ISBC inductor currents (i_{L1}, i_{L2}, and i_{L3}) and output current (i_o) in: (a) open-loop and (b) closed-loop operation.

A. *EFFICIENCY ANALYSIS OF THE MSCC*

To validate the proposed frequency optimization outlined in this paper, the MSCC converter underwent testing using the Yokogawa WT500 power analyzer at two distinct switching frequencies. One switching frequency was chosen from the frequency range acquired through analysis (80 kHz), while the other was deliberately set beyond this range (160 kHz), as illustrated in Fig. 14 (a). The efficiency peak for the MSCC stage was notably observed at 91.6% when operating at 80 kHz. Conversely, the efficiency peak at a switching frequency of 160 kHz was recorded as 87.22%, aligning with the anticipated outcomes from the frequency analysis.

Theoretical analysis was performed to evaluate loss distribution in the point delineated in Fig. 14 (a), and the results are depicted in Fig. 14 (b). The capacitor losses are primarily due to conduction losses caused by the equivalent series resistance (ESR). These losses are analyzed using parallel capacitors based on the RMS current obtained from simulations.

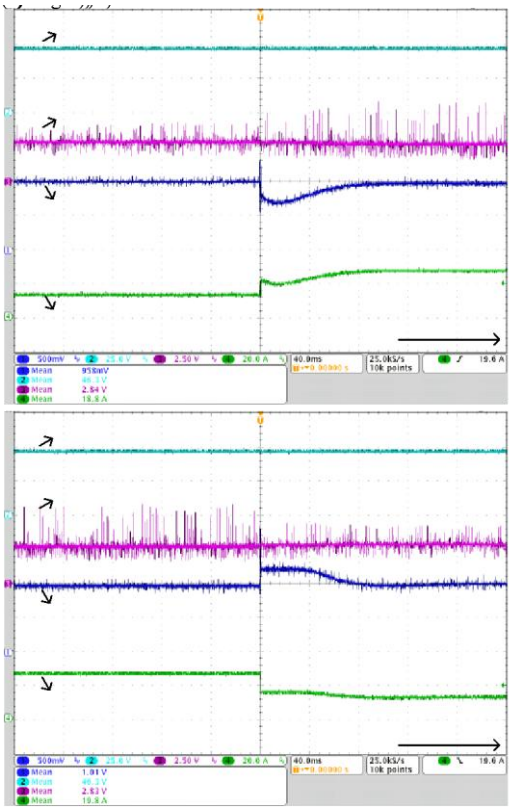

FIGURE 13. Experimental results – Input voltage (V_i), MSCC output voltage (v_{o1}), ISBC output voltage (v_o), and ISBC output current (i_o): (a) 66% positive load step and (b) 66% negative load step.

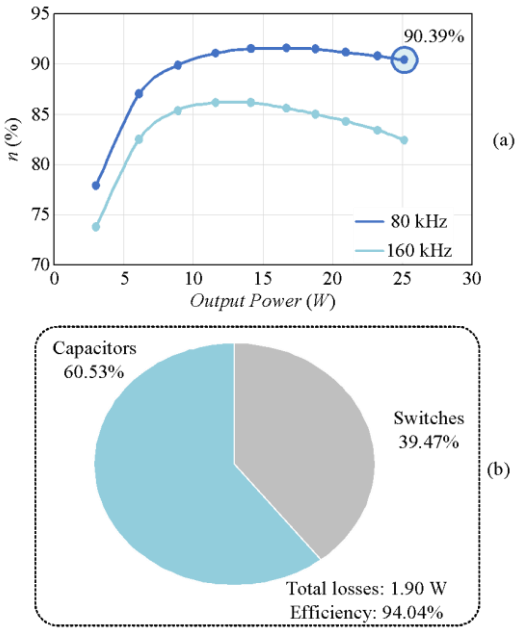

FIGURE 14. (a) The curve of the experimental efficiency of MSCC and (b) theoretical distribution of losses of MSCC.

The expected theoretical efficiency at rated power was 94.04% (as seen in Fig. 14 (b)), and the experimental efficiency obtained was 90.39% (as seen in Fig. 14 (a)). The leading cause of variance between theoretical and experimental efficiencies is the resistance stemming from the PCB trace, which holds significant values in applications characterized by low voltage and high current. This prototype serves as evidence showcasing the potential of this converter to achieve higher efficiency through an optimized prototype. It also shows how important it is to reach an optimized layout for this step-down converter.

B. *COMPARISON WITH OTHER SOLUTIONS*

A comparison of the proposed converter with other structures proposed in the literature is presented in Table 5, in which all of them underwent tests with a conversion from 48 V to 1 V. In the table, T represents the number of transformers, L the number of inductors, C the number of capacitors, S the number of controlled switches, V_c the maximum voltage stress on the capacitors, V_s the maximum voltage stress on the switches, G the gain ratio, P the maximum output power, and η the maximum efficiency. A first highlight is that none of these converters use diodes, which shows that these components perform worse than controlled switches for these applications.

In [26], a two-stage non-isolated solution is proposed. The first stage uses a hybrid SCC for the conversion from 48 V to 24 V, and the second stage uses a four-level buck converter with a series capacitor and coupled inductors for the conversion from 24 V to 1 V. In [27], a structure named Dual-Phase Multi-Inductor Hybrid Converter is proposed. This converter was tested for converting up to 48 V to 1 V and a rated power of 100 W. In [28], a three-level isolated half-bridge converter with synchronous current doubled at the output is proposed. The structure was tested for the conversion from 48 V to 1 V with a maximum power of 60 W. In [29], a forward converter with active clamping is presented. It was tested with input voltages of 48 V and 12 V, and output voltage between 0.7 V and 1.1 V.

A comparison with on-chip solutions was also made. In [14], a two-stage converter using a three-level buck with a hybrid Dickson switched capacitor converter is proposed, achieving a 48 V to 1 V conversion with a maximum output power of 12 W. In [30], a dual-phase buck converter is proposed to achieve a single-stage conversion from 48 V to 1 V with a maximum power of 1.5 W. In [31], a 12-level series capacitor converter is proposed, achieving a 48 V to 1 V conversion with a maximum output power of 8 W.

Compared to the structures in [26-29] in Table 5, the proposed converter presented the highest number of capacitors and switches, was tested at a lower power, and had slightly lower efficiency than the others. However, it has the lowest voltage stress on the components regarding HB-FC-CD. Since efficiency is the most crucial figure of merit, the theoretical distribution of losses of MSCC is shown in Fig. 14 (b), and it presents a maximum efficiency of 94.2%, higher than the other converters in the table. Thus, with a new design minimizing losses in the tracks and with experimental efficiency approaching the theoretical one, the proposed converter has the potential to reach a higher efficiency value and be more competitive in this merit as well.

Compared to the converters' on-chip solutions [14, 30-31], the proposed solution presents the highest conversion ratio and output power. However, it uses the highest component count. It should be highlighted that the proposed converter was not built on-chip, but it is suitable for it due to the low voltage stress on the components. It presents lower values than proposed solutions [14] and [31].

The theoretical efficiency curve as a function of output power is depicted in Fig. 15. The curve was plotted up to the maximum experimental output power, which is 60 W, for comparison with the converters proposed by [28] and [29]. The proposed converter achieves a maximum theoretical efficiency of 94.18%, surpassing the other converters, and maintains an efficiency above 75.5% across the entire power range. The experimental results did not reach the theoretical efficiency due to issues with the PCB design, which increased the trace resistance. This application has a high output current value, challenging active high-efficiency values due to the conduction losses in PCB and components.

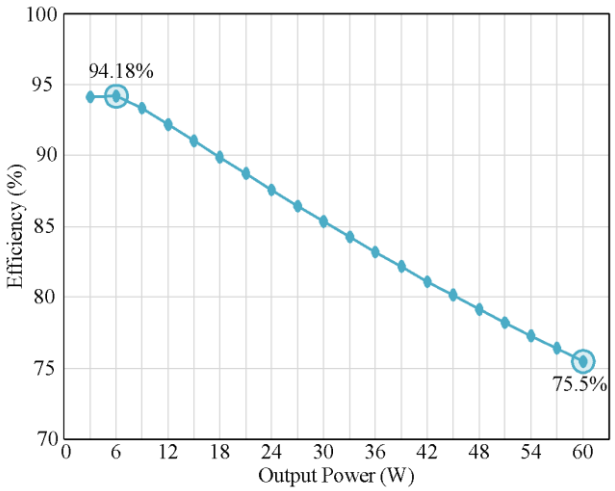

FIGURE 15. Efficiency curve concerning the output power of the proposed converter.

TABLE 5. Comparison with other converters.

Topology	*T*	*L*	*C*	*S*	*Vc*	*Vs*	*G*	*P*	*n*
Proposed	0	3	12	22	*Vi*/4	*Vi*/4	*D*/16	30 W	87.22 %
HSCC [26]	0	10	9	16	*Vi*/2	*Vi*/2	*D*/8	150 W	90.6 %
DP-MIH [27]	0	4	4	8	3*Vi*/4	3*Vi*/4	*D*/*N*	100 W	90.9 %
HB-FC-CD [28]	0	2	4	6	*Vi*/2	*Vi*/4	*D*/4*n*	60 W	92.8 %
ACFC [29]	1	1	3	4	*Vi*	*Vi*(1+1/n)	*D*/*n*	60 W	89.9 %
HDSCC [14]	0	3	6	11	*Vi*/2	*Vi*/2	*D*/10	12 W	90.4 %
DFBC [30]	0	2	1	4	*Vi*/2	*Vi*/2	*D*/4	1.5 W	85.4 %
SCBC [31]	0	2	11	13	*Vi*(12-*i*)/12	*Vi*/12	*D*/12	8 W	90.2 %

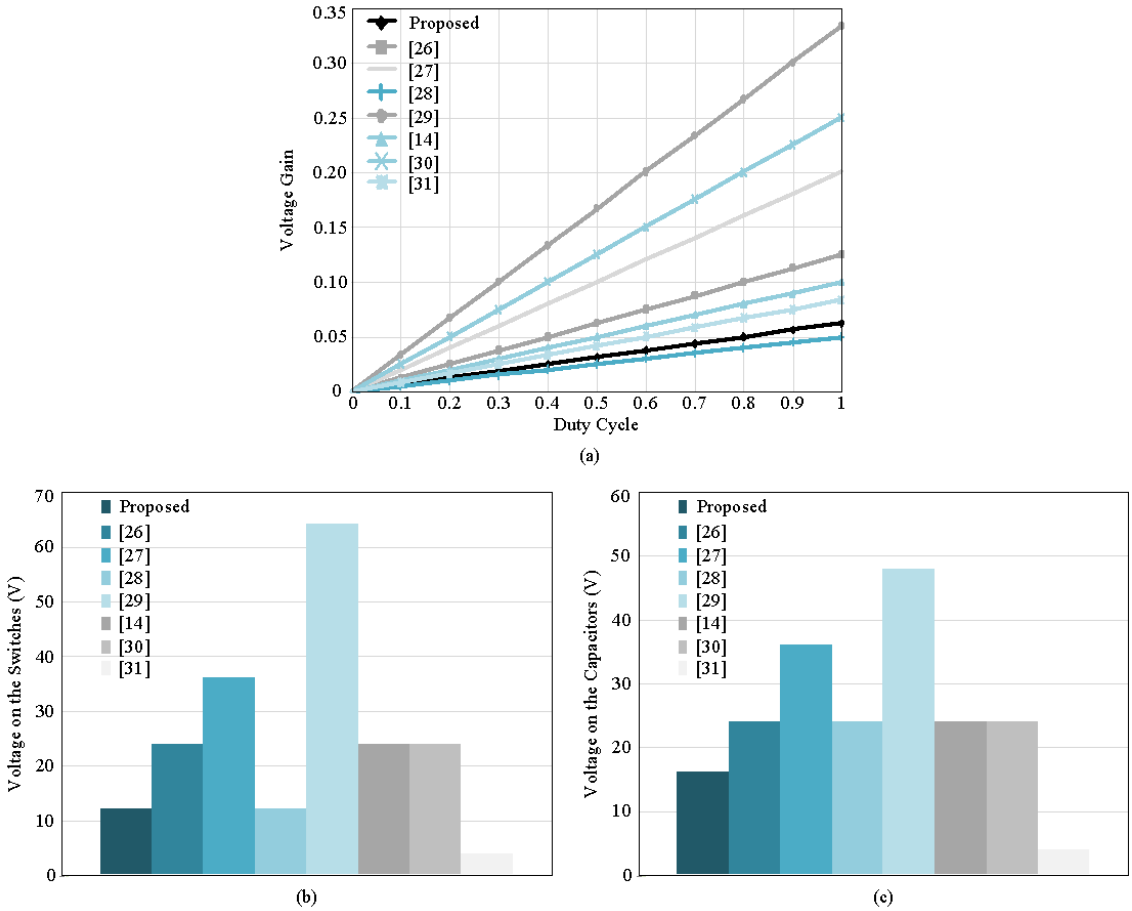

FIGURE 16. Comparison with other converters: (a) voltage gain in relation to the duty cycle, (b) voltage on the switches and (c) voltage on the capacitors.

To emphasize the comparison between the converters, Fig. 16 (a) depicts the graph of voltage gain as a function of the duty cycle for the converters listed in Table 5. Additionally, Fig. 16 (b) shows the voltage on the switches, and Fig. 16 (c)

illustrates the voltage on the capacitors. The proposed converter exhibits the second-lowest voltage gain, just behind the converter proposed by [28] (this solution utilizes a transformer). It also has the second-lowest voltage on the switches and capacitors, only surpassed by the converter proposed by [30] (tested at a lower output power than the proposed converter).

VI. CONCLUSIONS

This paper approached a new configuration of a switched capacitor cell, which integrates a cascade and ladder structure (named as mixed switched capacitor converter – MSCC). The structure provided a higher gain than the ladder SC cell using a smaller number of components and was verified to be adequate for high step-down DC-DC converters.

This study approached the MSCC connected with an interleaved synchronous buck converter to obtain a 48 V to 1 V conversion, specifically targeting applications in data centers. The first stage utilizes the MSCC to convert 48 V to 3 V, while the second stage employs the interleaved synchronous buck converter (ISBC) to convert 3 V to 1 V further.

The paper developed the mathematical analysis and design methodology for MSCC, including an optimization technique to determine the optimal switching frequency for enhanced efficiency in switched capacitor converters.

Two prototypes with an output power of 30 W were constructed to verify the proposed solution, one for MSCC and another for the ISBC stage. Both are connected in a cascaded configuration to provide 48V to 1V. The MSCC prototype achieved a voltage gain of 1/16, effectively converting the input voltage from 48 V to 3 V, while also generating intermediate voltage levels of 12 V and 6 V that can be utilized as additional voltage sources. Operating at the optimized frequency, the peak efficiency achieved was 91.16% for the MSCC stage, which provides 48V to 3V. This proposed configuration can be applied in intermediate stages for high-gain DC-DC converters operating in open-loop. The ISBC prototype successfully converted 3 V to 1 V, maintaining balanced currents in the inductors and regulated output voltage during load variations.

In conclusion, the proposed study offers a solution based on the SC for the conversion from 48 V to 1 V in data center applications. Topology and experimental approach were the main contributions of the paper.

AUTHOR'S CONTRIBUTIONS

N. C. D. PONT: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Writing – Original Draft, Writing – Review & Editing. **J. M. ANDRADE**: Supervision, Writing – Original Draft, Writing – Review & Editing. **C.BHARATIRAJA**: Conceptualization, Investigation. **B. LEHMAN**: Conceptualization, Investigation. **T. B. LAZZARIN**: Conceptualization, Investigation, Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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