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Proposal of Fully Integrated LED Driver with Enhanced Power Density for Street-lighting Applications

Igor B. Barboza[1,2,*], **Guirguis Z. Abdelmessih**[2], **Renan R. Duarte**[1], **Maikel F. Menke**[1], **Marco A. D. Costa**[1]

[1]Federal University of Santa Maria (UFSM), GEDRE - Intelligence in Lighting, Santa Maria, Brazil.
[2]University of Burgos (UBU), Electromechanics Department, Burgos, Spain.

e-mail: igor.b.barboza@gedre.ufsm.br*; gzakiguirguis@ubu.es; renan.duarte@gedre.ufsm.br; maikel.menke@ufsm.br; marcodc@gedre.ufsm.br.
*Corresponding author

ABSTRACT This paper proposes a new fully integrated Boost and Buck converter. The topology results from integrating the Boost as the power factor correction (PFC) stage and the Buck as power control (PC) stage. Besides this, the paper presents a methodology for designing the PFC stage inductor based on the inductance ratio between the PFC and PC stage inductances. In this work, the methodology analysis is carried out to enhance the converter power density using magnetics integration. Magnetic circuits and finite elements simulations compare the standalone and the integrated magnetics designs. Finally, the methodology is validated for the proposed fully integrated topology by implementing an 180 W LED driver prototype, which works properly for the grid voltage range (180-250 V_{rms}) and ensures full DCM operation between 10 and 100% of the LED load power. The experimental results show that the proposed topology fulfills the recommendation IEEE 1789-2015 and the standard IEC 61000-3-2 (Class C) in the grid range. The peak efficiency is 93.5% at 180 V_{rms}. The integrated magnetic enables a volume reduction of 20% compared to the standalone magnetics. The converter component count is significantly reduced compared to LED drivers found in the literature for street-lighting applications.

KEYWORDS Integrated magnetics, light-emitting diodes, LED drivers, magnetic core.

I. INTRODUCTION

LEDs (Light-emitting diodes) are nowadays recognized as the most appropriate artificial light source for most applications, mainly due to their robustness, high CRI (Color Rendering Index), high luminous efficacy, long lifetime, and no emission of UV rays [1], [2], [3].

In street-lighting applications, LEDs need a power supply to adapt the AC mains to the DC LED load, provide high PF (Power Factor) and low THD (Total Harmonic Distortion), and produce adequate current and voltage levels for the LED operation. For these reasons, the two-stage configuration LED drivers are recommended, the first is the PFC stage, which is in charge of the energy quality (high PF and low THD) in addition to keeping the average DC bus voltage at a regulated value, while the PC stage is responsible for the control of the LED load current. In this structure, the PFC and PC converters are independently controlled and often selected for high-power LED drivers [4][5]. Due to this fact, the independent switches and control systems of this configuration favor the proper operation on a broader AC grid voltage range and greater LED dimming interval.

A typical two-stage structure for street-lighting applications employs the Boost converter as the PFC stage (in CrCM) and Buck as the PC stage (in CCM). However, the selection of a two-stage configuration increases the total system component count.

Another solution is the utilization of single-stage converters formed by boost-buck-based converters, which is interesting in small power LED drivers ($<$ 100 W). The SEPIC converter is commonly selected in small power applications within this family of topologies. Some advantages of the SEPIC converter are its simplicity and low component number. However, as previously mentioned, due to the power level of this LED load, above 100 W, a single-stage configuration is not recommended, especially for the limited degree of freedom and the switch thermal management [6].

Aiming to reduce the LED drivers' component count, volume, size, and weight, hence decreasing the production costs, many integrated converter topologies have recently been proposed for different applications, including LED drivers [7], [8], [9], [10], [11], [12], [13], [17], [14], [15].

However, there are several issues regarding the integrated converter topologies for LED street-lighting applications found in literature, mainly with respect to the high number of capacitors and magnetic components, which represent the most significant part of the prototype total volume [9], [10], [12], [16].

Besides converters' integration, another technique to drastically reduce the volume of the prototype is magnetics in-

tegration, which makes it possible to integrate two magnetic components in the same core.

Many works in literature have already addressed the issue of volume reduction in converters by proposing magnetics integration techniques [17].

In [13], the first integrated magnetic was employed in an integrated converter. It was used in an LED driver, employing the Buck as the PFC stage and the Boost as the PC stage, both in DCM, to feed a 26.5 W LED load. This was also the first full integration (converters and magnetics integration) in an LED driver.

The magnetic integration technique is characterized by the absence of a gap in the center arm, hence the inductances are determined by the gaps in their respective individual outer arms. An additional advantage of this structure is the subtraction of the fluxes (generated by the MMF in the outer arms) in the center arm of the magnetic, which decreases the total core losses.

A relevant study of magnetics integration in LED drivers is presented in [9], in which a full integration is also proposed. The magnetics integration technique presented in [9] is employed individually in the magnetics of the PFC and PC stages; hence, this work has two integrated magnetics. The PFC stage integrated magnetic is formed by the transformer and the inductor of the modified Buck-Boost type converter, while the resonant tank inductor and the transformer of the LLC resonant converter make the integrated magnetic of the PC stage.

The configuration and methodology proposed by [13] leads to the power density increase in LED drivers. The power density presented in [13] is higher than the prototypes implemented in [9], besides the lowest component count presented by [13]. Furthermore, this technique is the simplest of the three references, which increases the reproduction reliability.

Dissimilar to these previous works, this paper proposes a new fully integrated LED driver topology, named FIBoBuC, using the Boost and Buck converters as PFC and PC stages, respectively. This converter integration was not previously presented in the literature. Besides that, the additional novelty of the current work is the magnetics integration in this topology. This converter significantly reduces the LED driver's volume and luminaire production costs. An additional advantage that the proposed converter presents is the design simplicity and lower switch count.

This work's motivation is to reduce the volume and costs of an 180 W commercial two-stage LED driver, formed by a Boost PFC stage in BCM and a Buck PC stage in CCM [18]. This product has standalone magnetics in each converter. The current paper is focused on the FIBoBuC, however, the basics information of the previously mentioned converter are illustrated in [19] and [20].

An additional contribution of this paper is the proposal of a new design methodology for the PFC inductor based on the integrated converter inductance ratio. This methodology allows the design of this element to be done using just the input grid voltage, the bus voltage and the nominal output voltage. The experimental results validate the proposed methodology.

The paper is organized as follows: Section II presents the analysis of the proposed integrated converter, including its operation principle, equivalent modes, main waveforms and mathematical relations. Section III describes the design methodology of the proposed FIBoBuC, highlighting the PFC inductor design based on the inductances´ ratio. Section IV details the design of the integrated magnetic, the theoretical and simulation procedures, and the validation using finite elements method (FEM). The standalone magnetics that will be compared to the integrated one are analyzed theoretically, as well as by FEM simulations. Section V validates the proposed FIBoBuC and the new design methodology by implementation and experimental results, in addition to comparing the current study with the main literature works, which present integrated converters for LED drivers in the same power range. Finally, the conclusions of this work are exposed in Section VI.

II. ANALYSIS OF THE PROPOSED BOOST PFC AND BUCK PC INTEGRATED CONVERTER

The proposed topology is based on integrating a DCM Boost converter as the PFC stage and a DCM Buck converter as the PC stage, following the methodology presented in [21]. The PFC stage must operate in DCM to avoid the necessity of a PFC control strategy. Furthermore, the full DCM operation is the most apropriate to ensure LED LFR (Low-Frequency Ripple) reduction, as verified by [22].

Besides this, the magnetics integration does not interfere with the converters' integration. Fig. 1 presents the schematic of the proposed converter, in which V_{rect} is the rectified voltage, after the diodes full-bridge rectifier. Fig. 2 illustrates the four operation modes of the proposed topology.

During Mode I, shown in Fig. 2(a), the switch S conducts, as well as the diodes $D2$ and $D3$. During this interval, the Boost inductor L_{Bo} and the Buck inductor L_{Bu} are charging, the bus capacitor C_b is discharging.

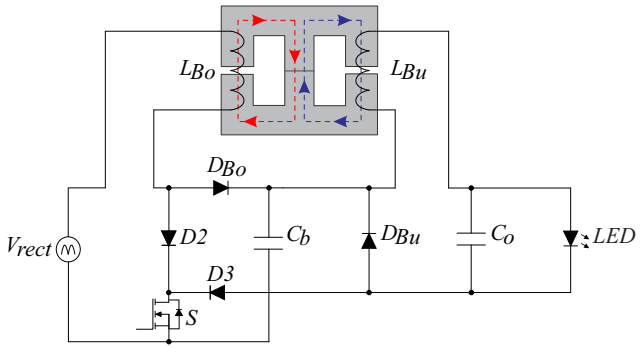


FIGURE 1. Schematic of the proposed FIBoBuC.

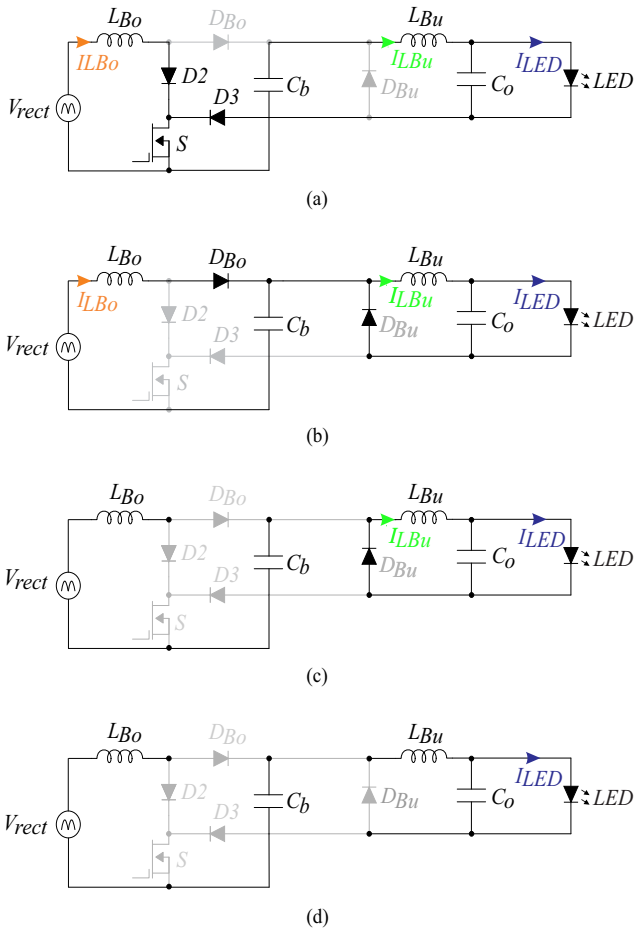


FIGURE 2. Equivalent operation modes of the FIBoBuC. (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV.

Mode II begins when S is turned off and both $D2$ and $D3$ are blocked, while the diodes D_{Bo} and D_{Bu} start conducting, as presented in Fig. 2(b). In this mode L_{Bo} and L_{Bu} discharge, C_b is charged with the energy stored in L_{Bo} and C_o is charged with the energy stored in L_{Bu}, from the first mode.

Mode III starts when one of the inductors is completely discharged, which varies according to the design specifications. D_{Bo} and D_{Bu} stop conducting when L_{Bo} and L_{Bu} are completely discharged, respectively. When D_{Bo} is blocked, C_b is fully charged and floating and, when D_{Bu} is blocked, it means that C_o is fully charged. Mode III, represented in Fig. 2(c), shows the condition in which L_{Bo} is fully discharged before L_{Bu}, because it corresponds to the experimental validation of the given work.

Mode IV initiates when L_{Bo} and L_{Bu} are totally discharged and, during this mode, none of the diodes nor S conduct, and the output capacitor C_o supplies the load.

Fig. 3 illustrates the main current waveforms of the FIBoBuC at a high-frequency switching period T_s.

The mathematical analysis of the integrated topology enables a proper design for full DCM operation. This study considers an ideal converter and an ideal input sinusoidal grid voltage $v_g(t)$ given by (1), where $V_{g.pk}$ is the grid peak voltage and ω_L is the angular grid frequency, in rad/s.

The peak currents of the Boost and Buck converters are expressed by (2) and (3), respectively, where D is the duty cycle, f_s is the switching frequency, V_o is the average output voltage and V_b is the average bus voltage. It is important to emphasize that D is the same for both converters, since they share the same switch.

$$v_g(t) = V_{g.pk} \cdot \sin(w_L \cdot t) \tag{1}$$

$$I_{Bo.pk} = \frac{D \cdot V_{g.pk}}{L_{Bo} \cdot f_s} \tag{2}$$

$$I_{Bu.pk} = \frac{(V_b - V_o) \cdot D}{L_{Bu} \cdot f_s} \tag{3}$$

The ratio between $V_{g.pk}$ and V_b is expressed by the index α, in (4), and the average grid current $i_g(t)$ per switching period is calculated by (5) [23]. The input power $p_g(t)$ is obtained by (6).

$$\alpha = \frac{V_{g.pk}}{V_b} \tag{4}$$

$$i_g(t) = \frac{D^2}{2 \cdot f_s \cdot L_{Bo}} \cdot \left(\frac{v_g(t)}{1 - \alpha \cdot \sin(w_L \cdot t)} \right) \tag{5}$$

$$p_g(t) = v_g(t) \cdot i_g(t) \tag{6}$$

By calculating the coefficient $Y(\alpha)$ through (7), it is possible to determine the Boost converter voltage ratio by (8) [24].

$$Y_f(\alpha) = -2 - \frac{\pi}{\alpha} + \frac{2}{\alpha \cdot \sqrt{1 - \alpha^2}} \cdot \left(\frac{\pi}{2} + \sin^{-1}(\alpha) \right) \tag{7}$$

$$\frac{V_b}{V_{g.pk}} = \frac{Y(\alpha)}{\pi} \cdot \frac{L_{Bu}}{L_{Bo}} \tag{8}$$

The voltage gain of the Buck converter in DCM operation is expressed by (9) [25]. The ratio between (9) and (8) results in the integrated converter voltage gain, expressed by (10), in which I_{LED} is the average LED current.

$$\frac{V_o}{V_b} = \frac{D^2}{\left(D^2 + \frac{2 \cdot I_{LED} \cdot L_{Bu} \cdot f_s}{V_b} \right)} \tag{9}$$

$$\frac{V_o}{V_{g.pk}} = \frac{D^2 \cdot Y(\alpha)}{\pi \cdot f_s} \cdot \frac{L_{Bu}}{L_{Bo}} \cdot \frac{V_b}{(1 + 2 \cdot I_{LED} \cdot L_{Bu})} \tag{10}$$

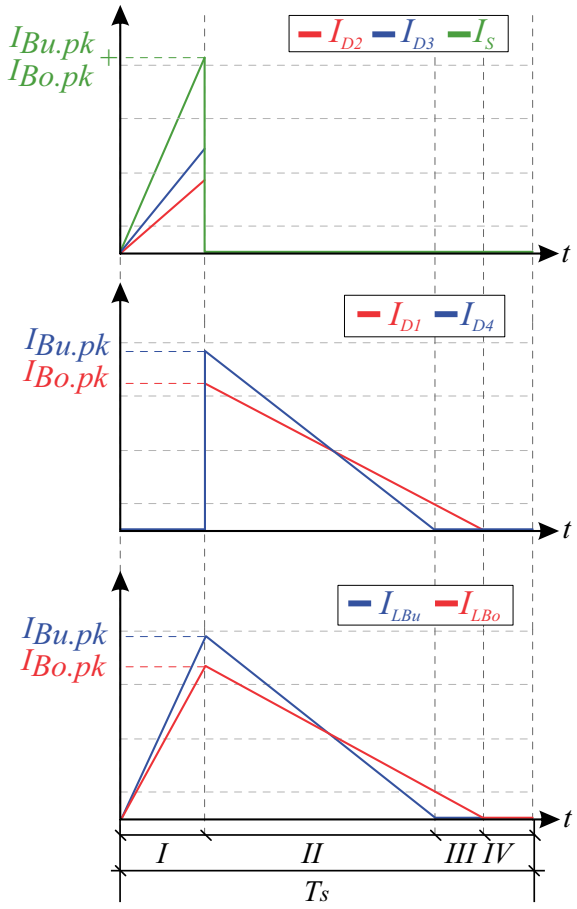


FIGURE 3. Main current waveforms of the FIBoBuC in full DCM operation, within a switching period.

III. DESIGN METHODOLOGY OF THE INTEGRATED CONVERTER

The design methodology proposed in this work is based on the inductances ratio L_{ratio}, which only uses the design specifications of peak grid voltage $V_{g.pk}$, bus voltage V_b, and output voltage V_o to design the PFC stage inductor, once the PC stage inductor is already known. The design of the PC stage inductor follows the methodology proposed by [14].

Concerning the FIBoBuC, it is required to determine the critical duty cycles $d_{Bo.crit}$ and $d_{Bu.crit}$ to establish the boundaries for full DCM operation of both converters, the PFC and PC stages [25]. Once the design specifications are known, it is possible to calculate $d_{Bo.crit}$ and $d_{Bu.crit}$ numerically. Then, the duty cycle must be kept always below the smallest value between these two boundaries to ensure full DCM operation of the integrated topology.

Since DCM is ensured by fixing the duty cycle D of the integrated switch in a value within the boundaries of the PFC and PC converters for DCM, the operation of the two integrated converters emulates a resistive load at the input. Furthermore, the analysis of the two converters can be decoupled, hence each one of them are analyzed individually [14].

The next step is to find the PC stage equivalent resistance R_{PC}. For a Buck converter, R_{PC} is given by (11). In addition, R_{PC} is also equivalent to (12), in which P_b is the average power delivered from the input to the bus. Considering an ideal converter, P_b corresponds to the average value of (6), and also to the LED nominal power. The inductance of the PC stage L_{Bu} is then isolated by manipulating (11) and (12). Once the factor Y_f in (13) [14] is replaced inside the resultant expression, the design equation for L_{Bu} is obtained by (14).

$$R_{PC} = \frac{2 \cdot L_{Bu} \cdot f_s}{D^2} \tag{11}$$

$$R_{PC} = \frac{{V_b}^2}{P_b} \tag{12}$$

$$Y_f = \frac{V_b}{V_b - V_o} \tag{13}$$

$$L_{Bu} = \frac{1}{Y_f} \cdot \frac{V_b^2 \cdot D^2}{2 \cdot P_b \cdot f_s} \tag{14}$$

The factor X_f shown in (15) is defined to design the inductor of the PFC stage [14].

$$X_f = \frac{2}{\alpha^2} \cdot \left[\frac{-2 \cdot \alpha}{\pi} - 1 + \frac{1}{\sqrt{1-\alpha^2}} \cdot \left(1 + \frac{2 \cdot \sin^{-1}(\alpha)}{\pi} \right) \right] \tag{15}$$

In the following, the proposed design methodology itself is presented. This is developed by manipulating (10), replacing (7) in the resultant expression, then isolating the relationship between inductances L_{Bo} and L_{Bu} in (7) and, finally, identifying the coefficients (13) and (15) into (7).

After this analysis, the inductances ratio L_{ratio} expressed by (16) is obtained, hence allowing to design the PFC stage inductor only in terms of the voltages $V_{g.pk}$, V_b and V_o.

$$L_{ratio} = \frac{L_{Bo}}{L_{Bu}} = \frac{1}{2} \cdot \alpha \cdot X_f \cdot Y_f \tag{16}$$

An advantage of this methodology is the possibility to analyze V_b in terms of $V_{g.pk}$ for any value of L_{ratio}, which enables the selection of the V_b to enhance the converter efficiency and/or reduce the volume of C_b, according to the desired design criteria of the application.

The graph of Fig. 4 provides several curves of L_{ratio}, thus enabling the selection of V_b for a given $V_{g.pk}$ and a fixed V_o, which is selected according to the load characteristic.

In this topology, to ensure the operation of the PFC stage, which is a Boost converter, V_b must always be higher than $V_{g.pk}$.

The capacitors C_b and C_o are designed to accomplish the IEEE 1789-2015 recommendation, which defines a maximum percentage of current ripple $\Delta I_{LED}\%$ as 19.2% at nominal power for a grid frequency of 60 Hz [26].

Initially, it is required to calculate the low-frequency ripple transfer ratio $LFRTR$ of a PC stage Buck converter [15]. After that, the percentage bus voltage ripple $\Delta V_b\%$ is obtained by the ratio between $\Delta I_{LED}\%$ and LFRTR, which is calculated in the previous step. Finally, the bus capacitance C_b can be determined by (17) [14], where f_L is the grid frequency.

The value of C_o is designed as a conventional output capacitor of a DCM Buck converter, expressed by (18), in which ΔV_o is the output voltage ripple [22].

It is important to analyze the influence of the grid frequency f_L in the FIBoBuC design. This parameter has no impact in the design of the PFC and PC stage inductors. However, f_L is inversely proportional to the bus capacitance, hence the decrease of this value from 60 to 50Hz, slightly increases the volume of the C_b, according to (17), considering the other same design specifications.

The low-frequency LED current ripple will also change in this case, from 120 to 100Hz. Regarding the limit duty cycles to ensure the full DCM operation, f_L does not change the PC stage duty cycle, but it affects the maximum duty cycle of the PFC stage. In the PFC stage using the Boost in DCM, if the f_L is lower, then the the limit for the DCM operation is higher [23], which enables to use a slightly smaller switching frequency f_s, which can also reduce switching losses.

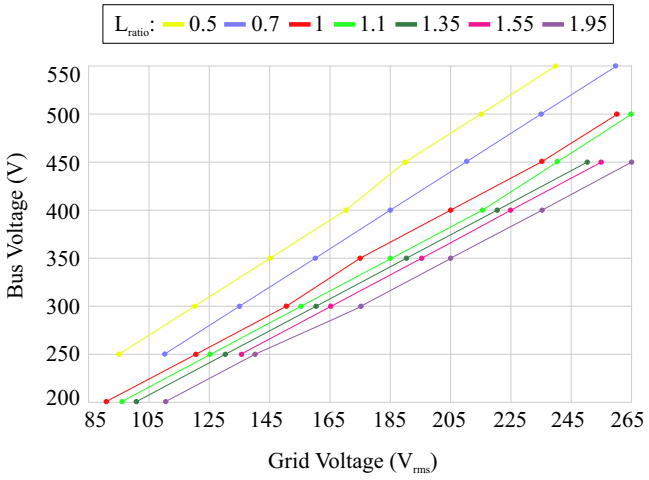


FIGURE 4. Inductances ratio analysis by varying V_b at distinct values of $V_{g.pk}$, with V_o fixed for the selected LED load at nominal power, at 104.4V.

$$C_b = \frac{P_b}{4 \cdot f_L \cdot V_b^2 \cdot \Delta V_b\%} \cdot \left[2 \cdot \alpha + \int_{\alpha}^{\pi-\alpha} \left| \frac{1 - \cos(2 \cdot \theta) - 2 \cdot sin(\alpha) \cdot \sin(\theta)}{1 - \frac{2 \cdot \alpha}{\pi} - \frac{\sin(2 \cdot \alpha)}{\pi}} \right| d\theta \right] \tag{17}$$

$$C_o = \frac{V_b \cdot L_{Bu}}{2 \cdot V_o \cdot \Delta V_o \cdot (V_b - V_o)} \cdot \left[\frac{(V_b - V_o) \cdot D}{f_s \cdot L_{Bu}} - I_{LED} \right]^2 \tag{18}$$

IV. ANALYSIS AND DESIGN OF THE STANDALONE AND INTEGRATED MAGNETICS

The inductances L_{Bo} and L_{Bu} are defined according to the methodology exposed in Section III, using equations (11)-(16).

Regarding the physical design of the inductors, the number of turns N is given by (19), in which L is the winding inductance, $I_{L.max}$ is the peak inductor current, B_{max} is the peak flux density and A_{cs} is the cross-sectional area of the core arm in which the winding is positioned.

$$N = \frac{L \cdot I_{L.max}}{B_{max} \cdot A_{cs}} \tag{19}$$

The magnetics integration is proposed to improve the integrated converter power density, simultaneously decreasing core losses compared to two standalone magnetics, which are designed using the same electrical and magnetic specifications.

The main principle of this magnetics integration technique is the subtraction between the magnetic fluxes at the center arm of the core since they flow in opposite directions, thus reducing the core losses. The gaps must be placed only in the outer arms in order to force their reluctance to be much higher than the center arm reluctance, which has no gap.

The decoupling between the windings' magnetic fields ensures that the integrated magnetic operation will not interfere with the converter's electrical behavior.

The integrated magnetic design follows the steps described in [13], including the design equations, thus only its essential points will be mentioned in this paper.

The core PQ 35/20 [27] is selected for the design of the integrated magnetic. To compare this integrated magnetic with standalone magnetics, two PQ 26/20 cores are chosen to theoretically design the Boost and Buck converters' standalone inductors [28].

This model was selected for each standalone magnetic because it is the PQ core size - hence the same format as the core selected for the integrated magnetic - which presents the central arm cross-sectional area A_{cent} with the closest value to the outer arms cross-sectional area A_{cs} of the core selected for the integrated magnetic, the PQ 35/20.

As mentioned above, to provide a fair comparison between the standalone and integrated magnetics, they are designed

TABLE 1. Design Specifications of the Magnetics

Parameter Symbol	Boost Inductor	Buck Inductor
Inductance L	368µH	273µH
Peak current $I_{L.max}$	3.45A	4.60A
Peak flux density B_{max}	0.35T	0.45T
PQ 35/20 outer arms A_{cs}	108.55 mm^2	
PQ 26/20 center arm A_{cs}	119 mm^2	

using identical electrical and magnetic specifications, which are shown in Table 1, as well as the same ferrite material, the 3C95 MgZn [29].

The simulations of the equivalent magnetic circuits of the standalone and integrated magnetics are developed according to the data available in the datasheets of the PQ cores and the 3C95 MgZn ferrite material [27], [28], [29].

The equivalent circuits representation and the simulation modeling are based on the procedures found in [13] and [20].

Based on the results of these simulations, the core losses are estimated to prove that the total core losses of the integrated magnetic are smaller than the sum of the total core losses of the standalone magnetics.

This estimation considers the volumetric losses presented in the ferrite material datasheet [29], according to the B_{max} at the fundamental switching frequency, in addition to the second and third harmonics. The geometry volume of each core part is taken into account, aiming to increase the precision of the losses' prediction, as can be detailed analyzed in Fig. 5.

The theoretical analysis of the standalone and integrated magnetics total core losses is compared with FEM simulations, which can be observed in Fig. 6.

The total theoretical core loss results calculated using the methodology of Fig. 5 are very close to the total core losses obtained by the FEM simulations in each magnetic in the standalone and integrated cases. These total losses are around 0.6 W, considering the average power losses within a low-frequency period of 120 Hz.

Furthermore, the flux density distribution between the center and the outer arms presented in Fig. 6 is in accordance with the values of Fig. 5.

Fig. 6 enables the verification of the fluxes subtraction at the center arm, resulting in B_{max} and core losses close to zero in many points of the waveforms.

Hence FEM simulations confirm the core losses theoretical analysis. These results show that the core losses are slightly lower using the integrated magnetic instead of separate inductors in identical design specifications.

However, the main advantage of the magnetics integration is the significant volume reduction enabled, because the PQ cores 26/20 and 35/20, selected for the standalone and integrated inductors, respectively, present total volumes of 9994 mm^3 and 12521 mm^3.

As there are two standalone magnetics and just one integrated magnetic, there is a core volume reduction above 20% using the magnetics integration.

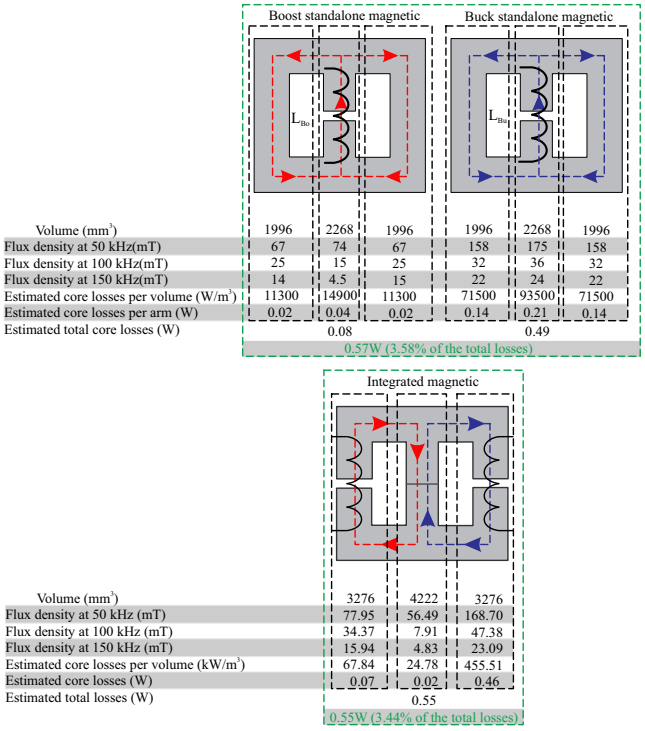


FIGURE 5. Theoretical core losses in the integrated magnetic of the FIBoBuC at the input voltage of 220 V_{rms} and nominal power.

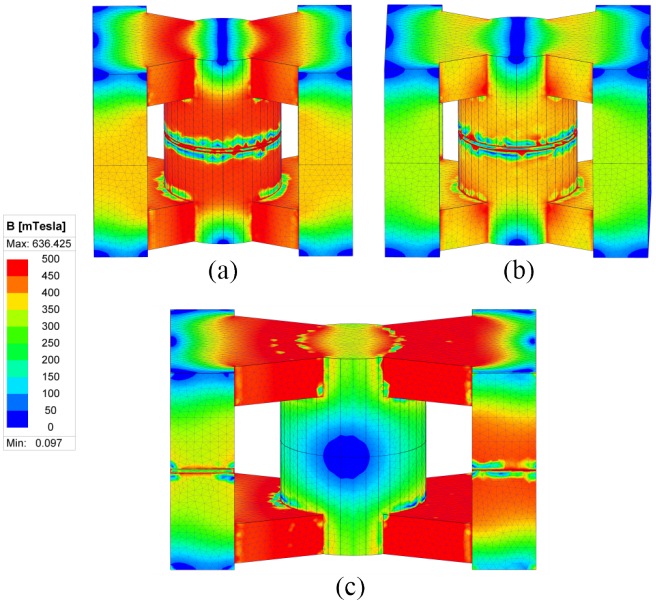


FIGURE 6. FEM simulation results of the magnetic flux densities at 220 V_{rms} and nominal power, using the software Ansys Maxwell. (a) standalone Boost magnetic; (b) standalone Buck magnetic; and (c) integrated magnetic.

V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The proposed FIBoBuC is implemented based on the methodology presented in Section III and on the integrated magnetic design described in Section IV.

Table 2 presents the prototype design specifications. By using (16) at the selected V_b, the inductances ratio L_{ratio} corresponds to 1.35. According to (14), L_{Bu} is 273 μH, and L_{Bo} results in 368 μH.

Table 3 presents the list of the main components of the FIBoBuC prototype. The 3D illustration of the magnetics construction is shown in Fig. 7, all in the same scale, to show how they are manufactured.

The photograph of the prototype is shown in Fig. 8. Its total volume is 432.28 cm^3. Since the nominal power is 180 W, the power density is 0.42 W/cm^3. Although heatsinks are not shown in this photograph, they are attached in the MOSFET switch and diodes D_{Bo} and D_Bu to dissipate the heat and ensure safe long-term operation.

After the integrated magnetic manufacturing, it is found that it corresponds to 44.7% of the FIBoBuC prototype volume. It is important to highlight that the PCB layout was not designed concerning volume, so the prototype power density can still be enhanced.

The power analyzer Yokogawa WT1800 is used to measure the efficiency results.

The grid voltage, grid current, bus voltage and LEDs current waveforms of the FIBoBuC at 220 V_{rms} and nominal operation are presented in Fig. 9. As can be noticed, the input waveforms behavior is nearly sinusoidal, typical of a DCM operation of the Boost converter, with the PF and THD corresponding to 0.95 and 26.38%, respectively.

As shown in Fig. 9, at 220 V_{rms} the measured $\Delta V_b\%$ is around 8.18%. The previous calculated $\Delta V_b\%$ was 10.53%, according to the C_b design presented in Section III, hence in accordance with the predicted design value.

The average bus voltage V_b is 396 V. The LED load is working at the desired operating point since I_{LED} and V_{LED} correspond to 1.56 A and 104.26 V, respectively.

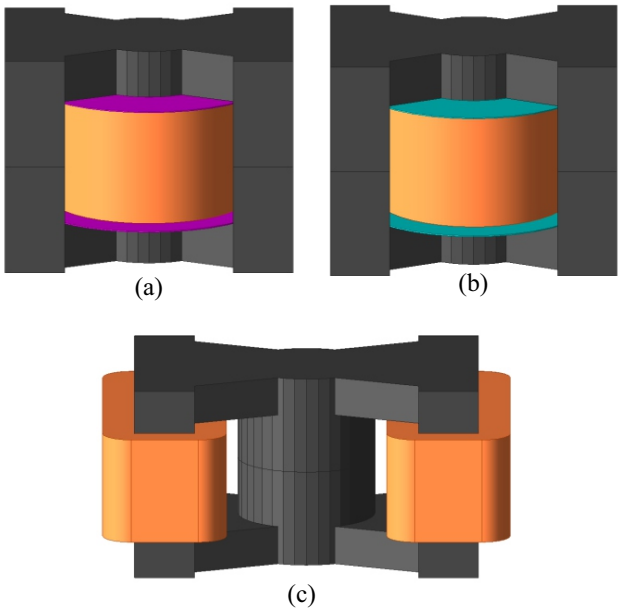


FIGURE 7. 3D illustration of the magnetics physical construction: (a) standalone Boost magnetic - PQ 26/20 core; (b) standalone Buck magnetic - PQ 26/20 core; (c) the integrated magnetic - PQ 35/20 core.

TABLE 3. List of Components of the Prototype

Parameter	Model / Value
Full bridge rectifier	GBU406
Integrated magnetic core	PQ 35/20
Boost inductor	L_{Bo} = 368 µH N_{Bo} = 34 turns, g = 0.40 mm 20 x Litz wire AWG 34
Buck inductor	L_{Bu} = 273 µH N_{Bo} = 28 turns, g = 0.37 mm 20 x Litz wire AWG 34
Bus capacitor	47 µF / 450 V
Output capacitor	15 µF / 200 V
Switch	NTP190N65S3HF - 650 V / 20 A
Diodes	BYC10DX-600 - 600 V / 10 A

TABLE 2. Design Specifications of the LED Drivers

Parameter	Symbol	Value
Grid RMS Voltage	$V_{g.RMS}$	180∼250 V
Grid frequency	f_L	60 Hz
Average input power	P_{in}	180 W
Nominal LED current	I_{LED}	1.55 A
Percentage LED current ripple	$\Delta I_{LED}\%$	19.2 %
LED threshold voltage	$V_{th.LED}$	82 V
LED operating resistance	R_{LED}	13 Ω
Nominal LED voltage	V_{LED}	104.4 V
Nominal bus voltage	V_b	400 V
Percentage bus voltage ripple	$\Delta V_b\%$	10.53 %
Switching frequency	f_s	50 kHz

The low-frequency LED current ripple (120 Hz) is around 250 mA (peak-to-peak), which represents a percentage value of 17.8% at full power, thus fulfilling the requirements of the IEEE 1789-2015, which establishes a maximum of 19.2% and once more corroborates the validation of the design of C_b.

Fig. 10 presents the Si MOSFET switch drain-to-source voltage and current at low and high-frequency, also at 220 V_{rms}. As can be observed, the switching frequency is 50 kHz, the maximum drain-to-source voltage V_{DS} is 570 V and the peak drain-to-source current I_{DS} is 8.64 A.

It must highlighted that the FIBoBuC is a hard switching topology. The V_{DS} voltage spikes on the switch are attributed

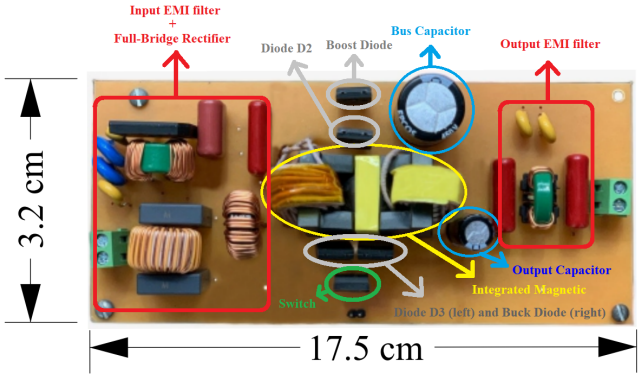


FIGURE 8. Prototype of the FIBoBuC.

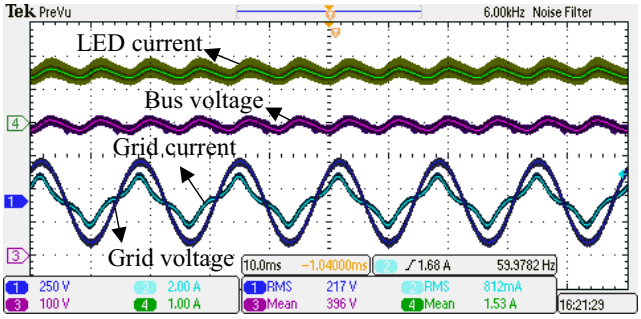
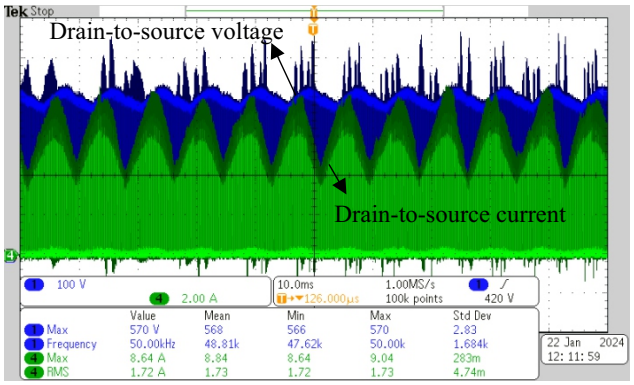
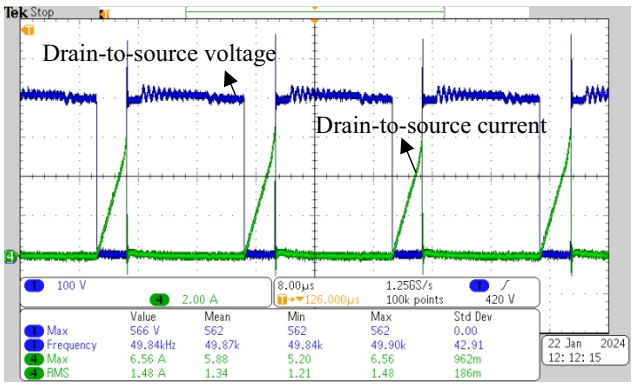


FIGURE 9. Grid voltage (CH1 – 250V/div.), grid current (CH2 – 2A/div.), bus voltage (CH3 – 100V/div.) and LED load current (CH4 – 1A/div.) of the FIBoBuC at 220 V_{rms} and nominal power.



(a)



(b)

FIGURE 10. SiC MOSFET V_{DS} (CH1 – 100V/div.) and I_{DS} (CH2 – 2A/div.) at 220 V_{rms} and nominal power. (a) low-frequency; (b) high-frequency.

to the parasitic inductances in the PCB layout, which can be easily enhanced.

Fig. 11 shows the inductors' currents, which confirm the full DCM operation at 220 V_{rms} and 180 W, as expected.

The LED dimming is achieved by changing the duty cycle D of the controlled switch S. The FIBoBuC presents full DCM operation from 10% to 100% of the LED load power at 180, 220 and 250 V_{rms}, which confirms the desired characteristic of the proposed topology.

It must be noted that, in order to guarantee DCM operation in both converters of the integrated topology, the duty cycle of the shared switch must always be below the minimum duty cycle between the two converters for a given operation. In this case, between 180 Vrms and 250 Vrms, considering the nominal power, the shared switch duty cycle remains between 15% and 27%.

The efficiencies of the proposed FIBoBuC under LED dimming are presented in Fig. 12.

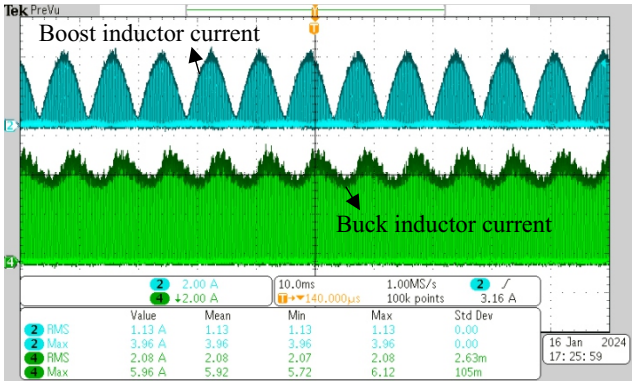
The power range is varied from 10 to 100% of the nominal load in all the operating points. At 180 V_{rms}, the FIBoBuC efficiency remains above 92.7% and the peak efficiency is 93.6%. At 220 V_{rms}, it remains above 91% and the peak efficiency is 92.2%. At 250 V_{rms}, it remains above 90.5% and the peak efficiency is 92.1%.

The efficiencies of the FIBoBuC at different grid voltages are very competitive compared to the results of the LED driver with a two-stage commercial LED driver [18], being higher in mostly operating points. This two-stage configuration with magnetics integration was investigated in the case studies [20] and [30]. In these two works, there are discussions regarding the developed research and other industrial applications and solutions. Both references compared their developed solutions with the . This product is detailed . The results vary between 88.5% and 93.1% throughout the LED load dimming range.

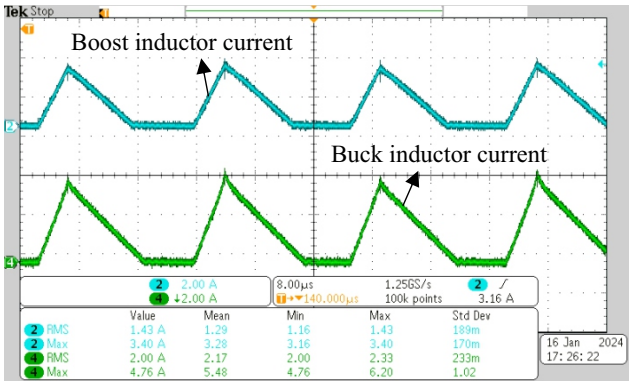
The power factor PF increases as the power is increased at the three input voltage conditions, as presented also in Fig. 12. As can be seen, under light load conditions, the efficiency remains high and very close to their respective peak values at different grid input voltages.

The Fig. 13 analyzes the proposed converter's grid current harmonic content at 220 V_{rms} and the nominal power. It confirms that, even though the FIBoBuC presents a large

THD at this condition, it is still within the IEC 61000-3-2 (Class C) standard limits. It can be noticed that the third harmonic content is high, as expected for the PFC Boost converter working in DCM [31].



(a)



(b)

FIGURE 11. Boost inductor current (CH2 – 2A/div.) and buck inductor current (CH4 – 2A/div.) at 220 V_{rms} and nominal power. (a) low-frequency and (b) high-frequency.

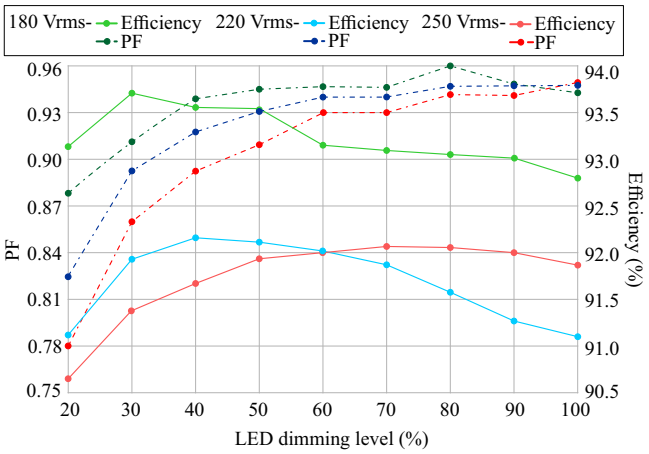


FIGURE 12. Efficiency and PF under LED dimming of the the FIBoBuC at 180, 220 and 250 V_{rms}.

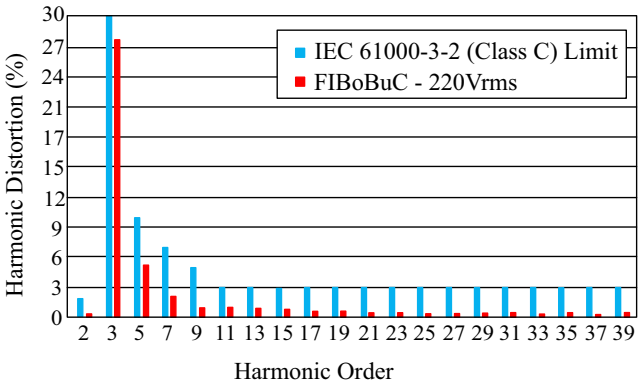


FIGURE 13. Comparison of the FIBoBuC grid current with the IEC 61000-3-2 (Class C) standard limits at 220 V_{rms}.

The comparison between the proposed FIBoBuC and literature works is presented in Table 4. It limits the comparison to LED drivers using integrated converters for for street-lighting applications with nominal power equal to or higher than 150 W.

The efficiencies of the proposed FIBoBuC, [9], [10] and [11] at different grid input voltages and LED dimming levels are available in Table 5, from 25% to 100% of the nominal LED load power.

In this comparison, besides the FIBoBuC, the evaluated topologies are the integrated buck-boost (PFC) with LLC resonant (PC) converter [9], the integrated class-E (PFC) with LLC resonant (PC) converter [10] and the integrated bridgeless boost (PFC) with isolated current-driven half-bridge (PC) converter [11].

As can seen in Table 5, high efficiencies are achieved by [9], between 50 and 100% of the load at the grid voltages of 220 and 265Vrms. However, it presents the

TABLE 4. Comparison Between the Proposed Integrated Converter and Related Literature Works

References	[9]	[10]	[11]	FIBoBuC
Number of Switches	2	2	2	1
Number of Inductors	2	1	1	2
Number of Transformers	2	2	2	0
Number of Cores	2	3	3	1
Number of Converter Diodes	3	3	4	4
Number of Capacitors	7	4	6	2
Total component count	25	15	18	10
Nominal Power (W)	200	150	150	180
RMS input Voltage (V)	185∼265	180∼250	99∼132	180∼250
Grid frequency (Hz)	50	50	60	60
Nominal Bus Voltage (V)	280	340	370	400
Output Voltage (V)	200	32	75	105
Magnetics Total Volume (cm^3)	34.17	90.82	16.09	9.99
Power Density (W/cm^3)	0.35	0.20	0.27	0.42

TABLE 5. Efficiency Comparison at Different LED Dimming Levels

LED Dimming Level (%)	[9]			[10]			[11]			FIBoBuC		
	185V	220V	265V	180V	220V	250V	99V	120V	132V	180V	220V	240V
25	85.80	90.10	90.80	-	-	-	95.30	95.40	95.50	93.60	91.50	90.70
50	88.20	92.00	93.10	-	92.80	-	95.78	95.88	96.02	93.50	92.10	91.90
75	91.50	93.80	94.30	-	92.30	-	95.85	95.97	96.17	93.27	91.75	92.06
100	89.50	93.40	94.00	80.50	91.40	92.30	95.30	95.80	96.00	92.69	91.15	91.84

largest component count. In [10], the efficiencies available are below the efficiencies of the FIBoBuC, [9] and [11] at almost all the operating points. The topology of [11] shows the highest efficiencies over the LED dimming range, but only at lower grid voltages (99-132 V_{rms}). In [11], the increase of the grid voltage also increases the bus voltage, as well as the switching losses. As consequence, the efficiency will decrease at higher grid voltages.

The proposed FIBoBuC presents the lowest component count and just one active switch, which requires only one driving circuit, thus reducing complexity. Besides this, the power density of the proposed FIBoBuC is 17% higher than in [9], 52% higher than in [10] and 36% higher than in [11]. In this work, the high power density is strongly related with the magnetics volume reduction, which is enabled by the magnetics integration.

VI. CONCLUSION

This work proposed a novel fully integrated converter focused on an LED driver application.

A new design methodology is proposed based only on the inductance ratio between the PFC and PC inductors, using only the peak grid voltage, the average bus voltage, and the average output voltage as input parameters.

An integrated magnetic is presented to reduce the power magnetics volume, which decreases the core losses, minimizes the component count, and enables the reduction of the magnetic core volume by more than 20% in comparison to two standalone magnetics under the same design specifications. FEM simulations validate the theoretical analysis of the core losses.

The magnetic volume reduction of 20% allowed by implementing the integrated magnetic instead of the designed standalone magnetics also represents an overall power density increase of 3.6 W/cm^3, if the separated inductors were implemented in the prototype with the same dimensions.

Considering that the magnetics of the power converters are a considerable portion of the volume and cost of LED drivers, this is an important landmark of the proposed work in street-lighting LED applications, hence enabling to drastically reduce the production costs of the entire LED luminaire by increasing the power density.

A prototype of the FIBoBuC to supply an 180 W LED load with an output voltage of 104V is built and tested at the input voltages from 180 to 250 V_{rms}.

The experimental results validate the proposed design methodology. The proposed converter also complies with the limits of the IEC 61000-3-2 (Class C) standard, despite the low PF and high THD. This is a characteristic of the Boost PFC converter in DCM operation.

Hence, the Boost converter is not indicated in integrated LED drivers for which the universal voltage range is a requirement, because it requires the bus voltage to always be above the peak value of the input voltage, which is a limitation.

Nevertheless, as shown by the experimental results and compared with other literature, this integrated topology presents good performance for a fixed grid input voltage within the range tested in this work (180-250 V_{rms}).

The efficiencies are above 92.5%, 91% and 90.5% at 180, 220 and 250 V_{rms}, respectively, from 20 to 100% of the LED load power. The maximum efficiency of the FIBoBuC is 93.6%, achieved at 180 V_{rms}. The peak efficiencies obtained at 220 and 250 V_{rms} are, respectively, 92.2% and 92.1%.

The FIBoBuC efficiency can be increased mainly by decreasing the two major verified losses: the MOSFET switching losses and the diodes D_{Bo} and D_{Bu} conduction losses. The switching losses can be decreased by using a semiconductor device with lower total output capacitance C_{oss} and, secondly, design the gate driver according to the selected MOSFET. Other alternative for it is the replacement of the MOSFET for a wide bandgap (WBG) device, such as SiC or GaN, which also leads to a better thermal management of the switch. Regarding the diodes conduction losses, they can be reduced by selecting devices with lower threshold voltages.

For this study, the efficiency measurements ensure accuracy and repeatability, including the converter thermal stabilization in each operating point.

The thermal behavior of the proposed integrated magnetics is not analyzed in this paper, but the experimental results at nominal power showed that the core and windings temperatures are as expected, far from exceeding the maximum values.

Another topic to be further investigated is the EMI performance of the FIBoBuC.

The FIBoBuC was tested in open-loop operation, because the focus was the verification of its operation and accordance with the theoretical design. Hence, a proposal for an additional proposal for future works is the implementation of a control circuit and the research on the input-to-output dynamic response of this topology.

The FIBoBuC can be scaled up to higher power applications once thermal management aspects are adequately analyzed, as well as careful PCB layout.

The total cost of the converter is not analyzed in this paper, because it includes distinct aspects and details that must be individually investigated, such as the manufacturing complexity, costs of materials and savings in long-term operation.

Finally, the comparison between the proposed FIBoBuC and the most outstanding literature on integrated converters for high-power LED drivers ($>$ 150 W) was performed.

The proposed topology presents the best cost-benefit relation between these solutions since it has the lowest number of components, just one switch and one magnetic core. Besides this, as there is only one switch, it requires only one driving circuit and a simple control system.

Furthermore, the integrated magnetic of the FIBoBuC represents the smallest proportion between the magnetic volume and the total prototype volume between all the compared literature works.

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AUTHOR'S CONTRIBUTIONS

I.B.BARBOZA: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Project Administration, Software, Validation, Visualization, Writing – Review & Editing. **G.Z.ABDELMESSIH:** Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Supervision, Visualization, Writing – Review & Editing. **R.R.DUARTE:** Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Visualization, Writing – Review & Editing. **M.F.MENKE:** Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Visualization, Writing – Review & Editing. **M.A.D.COSTA:** Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Supervision, Visualization, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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BIOGRAPHIES

Igor Bertoncello Barboza was born in Santa Maria – RS, in 1997. He received his Bachelor's and Master's degrees in Electrical Engineering from the Federal University of Santa Maria (UFSM) in 2020 and 2022, respectively. Since mid-2015, he has been a member of the GEDRE research group, focused on Intelligence in Lighting. He is currently pursuing a dual degree Ph.D. (cotutelle) in Electrical Engineering by the UFSM and the University of Burgos (UBU), in Spain. His research interests include electronic systems for lighting, LED driver circuits, converters with GaN transistors, and photovoltaic solar energy systems. He is a member of IEEE and chaired the UFSM IEEE Student Branch between 2023 and 2024.

Guirguis Zaki Abdelmessih received his B.Sc. degree in Electrical Engineering from the University of Ain Shams, Egypt, in 2013. He received his M.Sc. degree in "Electrical Energy Conversion and Power Systems" and his Ph.D. degree (with honors) on "analysis and development of improved converters for LED drivers with special focus on efficiency and dimming" from the University of Oviedo, Gijón, Spain, in 2015 and 2020, respectively. Since 2021, he is working as a Permanent Professor at the electromechanical department of the University of Burgos, Spain. Dr. Guirguis is the co-author of more than 28 journal and conference publications, including 12 publications in highly referenced journals. His research interests include light-emitting diodes, LED drivers, dc/dc converters, ac/dc converters, PFC stages, dimming systems, renewable energy, and power systems. He currently serves as Associate Editor of the IEEE Transactions on Industry Applications and IEEE Industry Applications Magazine.

Renan Rodrigo Duarte received the B.S., M.Sc., and Ph.D. degrees in Electrical Engineering from the Federal University of Santa Maria (2015, 2017, and 2022, respectively). He completed a curricular internship at Fraunhofer IZM in Berlin, Germany, in the RF SmaRenan Rodrigo Duarte received the B.S., M.Sc., and Ph.D. degrees in Electrical Engineering from the Federal University of Santa Maria (2015, 2017, and 2022, respectively). He completed a curricular internship at Fraunhofer IZM in Berlin, Germany, in the RF Smart Sensor Systems department (2014-2015) and worked as a senior designer at Zagonel S.A., focusing on hardware and embedded firmware design and development (2020-2023). Since 2023, he has been a professor at the Federal University of Santa Maria (UFSM). His main research areas include artificial lighting systems, high-efficiency converters, and GaN semiconductors.rt Sensor Systems department (2014-2015) and worked as a senior designer at Zagonel S.A., focusing on hardware and embedded firmware design and development (2020-2023). Since 2023, he has been a professor at the Federal University of Santa Maria (UFSM). His main research areas include artificial lighting systems, high-efficiency converters, and GaN semiconductors.

Maikel Fernando Menke received the B.S., M.Sc., and Ph.D. degrees in Electrical Engineering from the Federal University of Santa Maria, Santa Maria, Brazil, in 2015, 2016, and 2021, respectively. From 2019 to 2022, he was a Professor with the Federal Institute of Santa Catarina. Since 2022, he has been a Professor with the Federal University of Santa Maria. His research interests include lighting applications, DC-DC converters, power factor correction, and the analysis, design, modeling, and control of resonant power converters. Dr. Menke is a Member of the Brazilian Power Electronics Society (SOBRAEP) and IEEE.

Marco Antônio Dalla Costa received his B.S. and M.Sc. degrees in Electrical Engineering from the Federal University of Santa Maria, Brazil, in 2002 and 2004, respectively. He earned his Ph.D. degree (with honors) in Electrical Engineering from the University of Oviedo, Spain, in 2008. Since 2009, he has been serving as a Professor at the Federal University of Santa Maria, Brazil. Dr. Dalla Costa has co-authored over 240 journal and conference papers. His research interests include power electronics applied to lighting systems, LED drivers, LED modeling, horticultural lighting, and visible light communication systems. Since 2018, he has been serving as an Associate Editor for the IEEE Transactions on Industrial Electronics and the IEEE Journal of Emerging and Selected Topics in Power Electronics. Additionally, he chaired the IEEE Industry Applications Society's ILDC (2019–2020) and MSDAD (2020–2021).