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Leakage Current Mitigation in On-Grid Photovoltaic Systems Using a Flexible Multi-Level Inverter Topology

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ABSTRACT Leakage current is an issue that often causes problems in transformerless grid-connected PV inverters, such as electromagnetic interference, which is conducted or radiated and derates the quality of power injected into the grid. It can also lead to electrical safety problems, impair the performance of other equipment nearby, and thus make the generation system unavailable. Therefore, mitigation procedures for the leakage current in transformerless grid-connected PV inverters are essential to ensure system efficiency and safety. In this sense, a new single-phase grid-connected transformerless inverter topology was proposed using modulation switching techniques to keep the leakage current at acceptable standard levels. With the proposed topology, by monitoring the leakage current rms value, the inverter can be driven in a three- or five-level pattern for the main switches, thereby keeping the leakage current at a satisfactory level. The topology was implemented in a versatile hardware-in-loop Typhoon-HIL to emulate a digital twin of the complete system, with the control loops and switching generation embedded in a family Texas Instruments F28335 DSP. The results obtained for total harmonic distortion and energy conversion efficiency were then compared with other consolidated topologies, and the leakage current was proved to be effectively modified when the inverter is switched in three- or five-level modes.

KEYWORDS Leakage current; Common mode voltage; Multi-level PWM; Photovoltaic inverters.

I. INTRODUCTION

In recent years, growing concern about energy demand and the substantial environmental impact caused by using fossil fuels to generate energy has led to the search for renewable energy sources. The alignment of technology and science advancements with sustainable development goals - SDG [1] of the United Nations is a paramount motor to the emerging research in several knowledge areas; cleaning, efficient and effective power conversion is adherent to the goals #7 - Affordable and Clean Energy, #9 - Industry, Innovation and Infrastructure, and #11 - Sustainable Cities and Communities, asides to indirect contributions to other SDG. In this scenario, solar energy stands out due to its clean and abundant nature, which can be competitive and work in conjunction with hydro and thermal sources [1], [2]. Due to these characteristics and the increasing development of energy conversion systems, new solutions are constantly being sought to overcome the challenges associated with photovoltaic energy conversion, such as the variation in solar irradiation and the need for high efficiency.

Various factors, such as the growth in the demand for clean energy, the reduction in the cost of power electronics, and advances in control technologies, drive the evolution of photovoltaic inverter topologies. However, new challenges arise with the increasing injection of solar energy into the electricity grid, such as the need to guarantee the stability and compatibility of the system with other renewable energy sources [3], [4]. In this context, new inverter topologies must offer greater flexibility, modularity, and intelligence, allowing photovoltaic systems to be integrated into increasingly complex and distributed electrical grids [5].

Previous work on photovoltaic inverter topologies presents diverse approaches and levels of detail. Authors such as [6] and [7] offer in-depth analyses of the main topologies, comparing their performance in terms of efficiency, cost, and waveform quality. [8] and [9], [10] explore the latest trends in modular and multilevel topologies, highlighting their advantages for large photovoltaic systems. This variety of perspectives enriches knowledge on the subject and helps develop the most suitable topologies for each application.

The function of the inverter is to convert the direct current generated by photovoltaic modules into an alternating current suitable for use in electrical distribution networks. In this context, transformerless inverters have become increasingly common due to their advantages over systems with transformers. In addition to cost and the physical volume reduction, they allow for improved energy efficiency and better conversion of the direct current generated by

[1]The UN SDGs, https://sdgs.un.org/goals

photovoltaic modules into alternating current for injection into the electrical grid [11].

In this way, a new topology of the inverter connected to the grid without a transformer that presents low leakage current through the modulation switching strategy allows situations where the parasitic capacitance reaches a value such that the leakage current exceeds the normative limits to ensure the continuity of power injection into the grid.

This paper is divided into six sections. The second section briefly explains the transformerless inverter and its characteristics, comparing it with the transformer-based inverter. The third section describes the most common transformerless inverter topologies in the literature, describing their principle of operation. The fourth section proposes a new topology to solve the problems addressed in the previous sections by changing levels based on the value of the relevant leakage current in the system. In section five, a comparison is made between the proposed topology and the topologies in the literature. Finally, the sixth section presents the conclusion of the results obtained in the article.

II. PROBLEMS OF TRANSFOMERLESS PV INVERTERS

Inverters transformer-based (galvanically isolated) have disadvantages over transformerless (non-isolated) inverters. One of the main disadvantages is their weight. The transformers used in these inverters are typically made of ferromagnetic material, such as silicon steel, which makes them heavy [12]. Another important disadvantage of inverters with transformers is related to the volume occupied by these components [13]. Transformers tend to take up a considerable amount of space due to the need for adequate insulation and the arrangement of the coils. It limits design flexibility in applications where space is a valuable resource. Finally, efficiency is another notable disadvantage of inverters with transformers [14]. By nature, transformers introduce losses into the system due to hysteresis effects and eddy currents. Although this, transformerless inverters have some disadvantages, including parasitic capacitance that implies in common mode voltage and leakage current, which will be explained in this section, detailing their characteristics.

A. Parasitic capacitance

The photovoltaic module is structured as: an aluminum frame, special glass, encapsulant, photovoltaic cells, encapsulant, and a *back sheet*. In a normative way, it is required that the metallic structures are grounded [13]. In this way, an equivalent capacitive effect arises in the modules of the photovoltaic system, as shown in Fig. 1, where this equivalent value depends on various factors, including humidity and temperature to which the modules are subjected during their operation [15]. In unsophisticated transformerless topologies, the relationship between the *string* (DC) and grid (grid) potentials oscillate with large amplitude, providing a high common mode voltage, which corroborates the emergence of a leakage current circulating through the system between photovoltaic modules and grid [16].

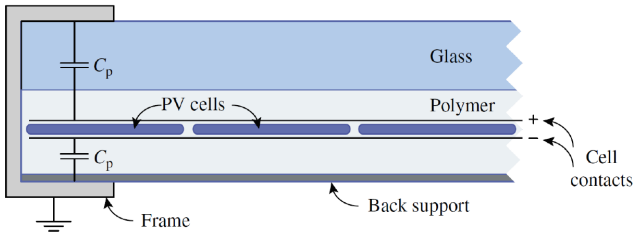

FIGURE 1. Parasitic capacitances in the photovoltaic module adapted from [17].

B. Common mode voltage

The topology of the inverter and the modulation strategy defines the relationship between the potentials of the string (DC) and the grid (AC). The semiconductor switches' switching can transmit the grid's alternating potential to the photovoltaic modules. In topologies without a transformer, the potentials in the strings can reach values with large oscillations. The non-constant common-mode voltage favors the emergence of leakage current circulating through the system, [18]. The common-mode and differential-mode voltages in the inverter in Fig. 2 can be written according to the equations 1 and 2, respectively.

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{2}$$

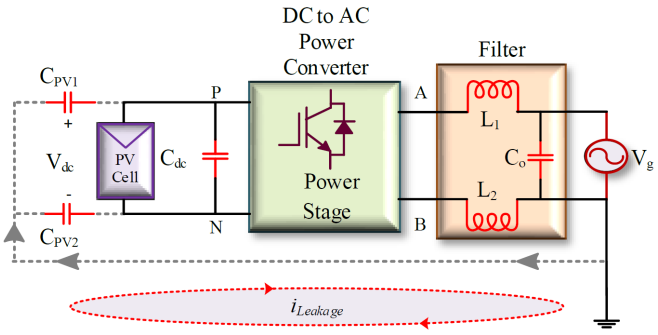

FIGURE 2. Parasitic capacitances and leakage current in the grid-connected photovoltaic system without transformer (adapted from [19], [20]).

C. Leakage current

The state of charge of the parasitic capacitances is altered when there is a variation in the voltage applied to the terminals of the photovoltaic module. Due to the parasitic capacitance and the inverter's common mode voltage, a leakage current arises and flows through the system, as seen in Fig.2. This effect can cause protection from trips,

safety problems, efficiency degradation, additional harmonic distortion, and electromagnetic interference problems. In general, the variation in the amplitude of the voltage applied to the terminals of the photovoltaic module is proportional to the amplitude of the leakage current. In the case of transformerless inverters, this current will circulate throughout the system and be injected into the electricity grid, which causes an increase in harmonic content [21], [22].

D. Leakage current regulations

The leading international standards that define operating limits and leakage current criteria are VDE 0126-1-1 and IEC 62109-2. Differential current is defined as the algebraic sum of the leakage current values, which flows through the parasitic capacitance, and the residual current, which flows through the circuit's conductors, expressed as a practical value. Protection against excessive residual current is one of the safety requirements for transformerless inverters, and its primary purpose is to protect against electric shock [23], [24].

The VDE 0126-1-1 and IEC 62109-2 standards set limits for residual current. If this exceeds 300 mA, the inverter must be disconnected from the mains within 300 ms. In addition, variations in leakage current over a given time must follow the limits described in Tab. 1. Thus, when the leakage current is high, the residual current monitoring is compromised, causing the protections to be triggered in an undesirable way.

TABLE 1. Leakage current variation limits, according to VDE 0126-1-1 [24]

$i_{Leakage}$ (mA)	Time (ms)
30	300
60	150
100	40

The common mode voltage produced by the PV inverter added to the equivalent parasitic capacitance of the modules causes the emergence of a leakage current that circulates between the DC and AC parts of the PV system, as shown in Fig.1 [25]. This leakage current causes degradation of the quality of the power injected into the electrical grid by elevating the harmonic content of the current and EMI (electromagnetic interference). If this current value exceeds the regulatory limits [24], [26], the PV inverter must disconnect from the grid to ensure the safety of equipment and people.

Some adopted ways in the literature to overcome these effects are clamping at the neutral point of the DC bus and decoupling, which can occur either on the AC or DC side, as demonstrated in [27], [28], or directly connecting the ground of the grid to the ground of PV ensemble [29]. This work aims to mitigate the effect of leakage current by implementing the modulation switching strategy. This approach disturbs the parasitic capacitance to keep the leakage current within normative limits. In this way, continuity of power injection into the grid is guaranteed, ensuring proper system operation.

III. FULL BRIDGE-DERIVED TOPOLOGIES

In this section, we introduce the three-level topologies, specifically the *Full-Bridge* and its variations, *HERIC*, and *HB-ZVR*. Additionally, we cover topologies operating with five levels, such as *NPC - five levels*, *T-type - five levels* and *Floating Capacitors*. The operational details of each topology are described, and we delve into specific results concerning common-mode voltage and leakage current. These findings are explored to facilitate subsequent comparisons.

A. Full-Bridge

The *full-bridge* topology is shown in Fig.3. With the unipolar *PWM* modulation scheme, the operation of switches Q1 and Q2 are complementary at low frequency (60 Hz). Switches Q3 and Q4 are operated at high frequency (20 kHz), which allows for reaching an output voltage of three levels (+Vdc, 0, -Vdc), [30].

The three-level output voltage reduces the inverter's output filter without significant losses while maintaining high efficiency. However, despite its high efficiency and simple requirements for the output filter, this topology presents a high leakage current, as the common mode voltage during its operation varies at high frequency. Therefore, using the transformerless *full-bridge* topology for grid-connected photovoltaic applications is unsuitable, [31].

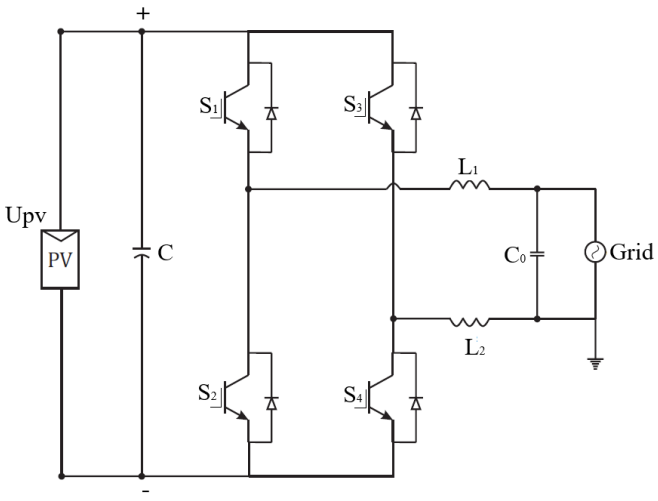

FIGURE 3. Full-Bridge (FB) inverter topology

B. HERIC

The Highly Efficient and Reliable Inverter Concept (*HERIC*) topology, initially proposed in 2003 by *Sunways*, combines the advantages of modulation in three output voltage levels, of unipolar *PWM* with the reduction of common mode voltage and current of escape. This way, the inverter's efficiency is improved considerably without compromising other system parameters, [31], [32].

The zero voltage state is reached using bidirectional switches between the output terminals, *1* and *2* inversely

as shown in Fig. 4, offering a free-flow path to the grid. The AC *bypass* switches prevent the exchange of reactive power between the output filter inductors (L1 and L2) and the DC link capacitor (Cdc), contributing to improved efficiency.

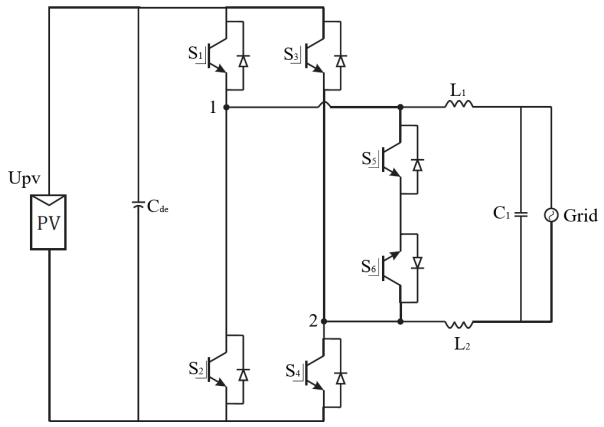

FIGURE 4. HERIC inverter topology.

C. HB ZVR

The H-Bridge Zero-Voltage Switch Controlled Rectifier (*HB-ZVR*) topology was initially presented in [31]. Its main feature is to connect the midpoint of the DC link to the inverter only because the state period uses a diode rectifier bridge and a switch, as shown in Fig.5.

The zero voltage state is achieved by turning S5 on when S1 and S4 are turned off. Switching of S5 will be complementary to S1 and S4, with a small *dead time* to avoid a short circuit in the DC link capacitor (*Cdc*). Switch S5 allows the main current to flow in both directions; in this way, the inverter can supply reactive.

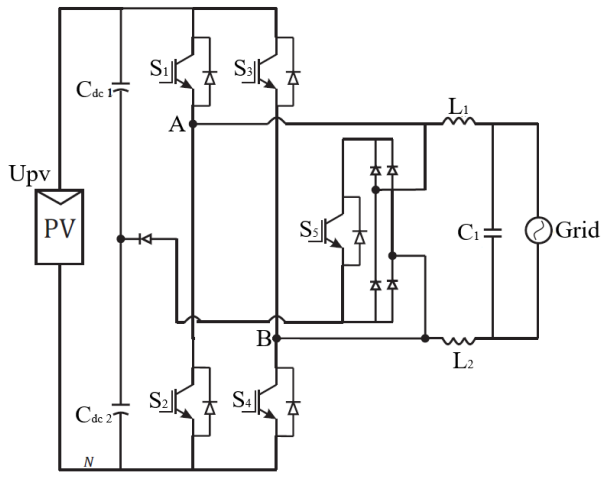

FIGURE 5. HB-ZVR inverter topology adapted from [27].

[31] shows that the topology *HB-ZVR* has a slightly lower efficiency compared to *HERIC* because the 'bidirectional switch' is switched at high frequency, while in the case of the topology *HERIC*, the 'bidirectional switch' is switched to the mains operating frequency. With an efficiency of approximately 94%, it is an alternative solution for transformerless grid-connected single-phase photovoltaic systems.

D. NPC- five levels

The 5-level Neutral Point Clamped Inverter (*NPC*) multilevel inverter configuration, presented in Fig. 6, employs five voltage levels to generate a sinusoidal output. This is achieved through a setup from a parallel arrangement of the traditional 3-level NPC. Its primary advantage is providing an output voltage with significantly reduced harmonic distortion. This is extremely important in applications requiring a high power quality standard, particularly in grid-connected renewable energy systems [33].

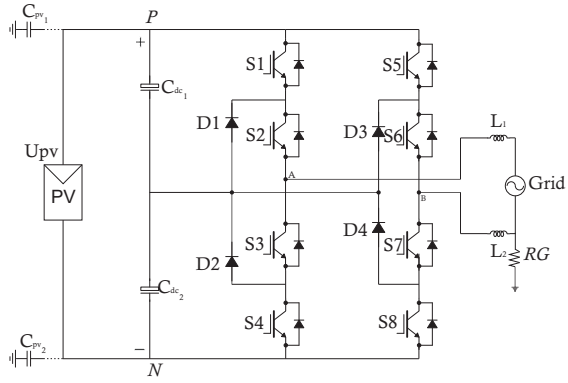

FIGURE 6. NPC five levels inverter topology.

Reducing the breakdown voltage of the semiconductor devices to half of the DC bus voltage decreases switching losses, which are less sensitive to the switching frequency [34].

E. T-type- five levels

The 5-level T-type inverter is a multilevel alternative widely used in single-phase photovoltaic systems. It uses eight switches to generate five levels, like the full-bridge NPC, as shown in Fig 7.

However, the T-type inverter operates with fewer semiconductor devices in the current path than the full-bridge NPC, which results in low conduction losses. On the other hand, only half of the T-type inverter's semiconductors operate at half the DC bus voltage [35].

In addition, it requires at least two switch changes in the transitions between voltage levels. Yet, the T-type inverter is considered a promising option for applications in photovoltaic systems due to its high efficiency, low conduction losses, and lower number of semiconductor devices compared to other multilevel topologies [36]–[38].

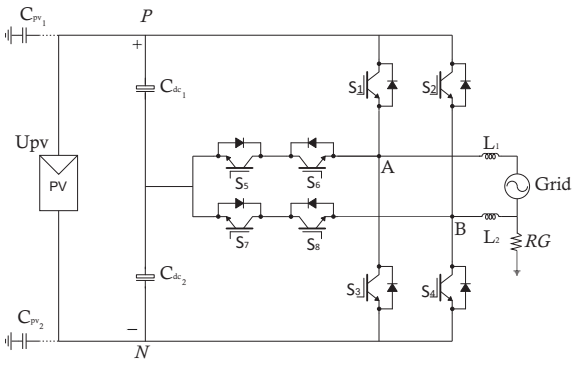

FIGURE 7. T-type five levels inverter topology.

F. Floating Capacitors - five levels

The 5-level floating capacitor *(FC)* inverter is a multilevel option that has been used in photovoltaic systems, consisting of two floating capacitors operating at half the DC bus voltage, generating five voltage levels [39]. As shown in Fig. 8.

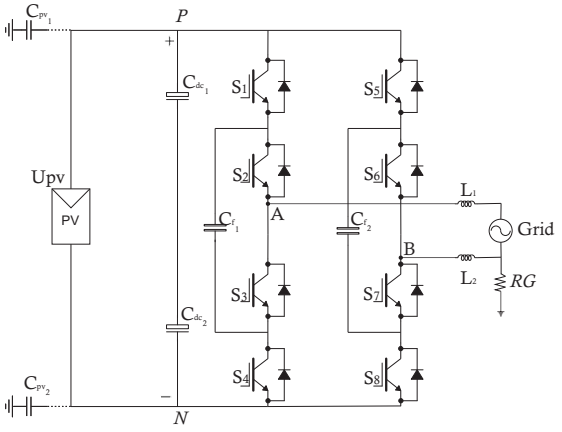

FIGURE 8. Floating Capacitors - five levels

The main benefit of this topology is that it reduces the number of semiconductor devices in the current path, providing lower conduction and switching losses compared to other multilevel topologies. However, a disadvantage of this configuration is the need for two robust floating capacitors, which can be a challenge in design and cost. Also, more complex control is required to balance the voltages across them [40].

IV. PROPOSED TOPOLOGY

The proposed topology of a grid-connected single-phase five-level inverter consisting of eight switches is shown in Fig. 9. The configuration switches switch from five levels to three levels at the output. The operating principle in the 5-level structure consists of using switches S7 and S8 to create an intermediate point between the input capacitors, thus allowing the voltage $\pm 1/2V_{dc}$, as presented in Tab. 2. In the 3-level configuration, the S7 and S8 switches are not used, limiting the use of S5 and S6 - this pair of switches is essential to the assure de level 0-mode, as shown in Tab. 3. To avoid interruption in the operation of the inverters, the allowed values comply with the standards VDE 0126-1-1 and IEC 62109-2.

TABLE 2. Switching to 5 levels.

Mode	[S1 S2 S3 S4 S5 S6 S7 S8]	VDM	VCM
Vdc	[1 0 0 1 0 0 0 0]	V_{dc}	V_{dc}/4
+1/2Vdc	[0 0 0 1 0 0 1 1]	$+1/2V_{dc}$	$3/4V_{dc}$
0	[0 0 0 0 1 1 0 0]	0	Not constant
-1/2Vdc	[0 0 1 0 1 0 1 1]	$-1/2V_{dc}$	$-3/4V_{dc}$
-Vdc	[0 1 1 0 1 0 0 0]	$-V_{dc}$	$-V_{dc}$/4

TABLE 3. Switching to 3 levels.

Mode	[S1 S2 S3 S4 S5 S6 S7 S8]	VDM	VCM
Vdc	[1 0 0 1 0 0 0 0]	V_{dc}	V_{dc}/2
0	[0 0 0 0 1 1 0 0]	0	Not constant
-Vdc	[0 1 1 0 1 0 0 0]	$-V_{dc}$	$-V_{dc}$/2

This configuration has the advantage of an agile change of operation from 5 levels to 3 levels, accompanied by a simplified control strategy for this transition, which will be described in more detail in section V. This puts it in a competitive position regarding operating modes compared to other topologies already recognized in the literature.

V. RESULTS

Tests were carried out on Typhoon's Hardware-in-the-Loop (HIL) 604 platform to develop and test complex embedded systems in real time. The controllers were implemented on a Texas Instruments F28335 digital signal processor (DSP), as shown in Fig.10. The parameters used in the simulation components are listed in the Tab.4.

TABLE 4. Parameters used in the simulations.

Parameters	Value
Input Voltage [V_{dc}]	400V
Grid Voltage [V_g]	220V
Switching Frequency [F_sw]	30kHz
Inductive Filter [L_1,L_2]	3mH
Parasitic Capacitance [C_{pv}]	50nF-75nF
Ground Resistor [R_g]	5Ω
PV Power [kW]	2kW
Simulation Time-Step [uS]	0.5 uS

Two control loops are used, an internal control loop and an external control loop; one controls the current injected into the electrical grid, and the other controls the DC link voltage, respectively, so the voltage is constant. For current control, a proportional resonant (P+RES) compensator ($C_i(s)$) was used, which has the function of reproducing a

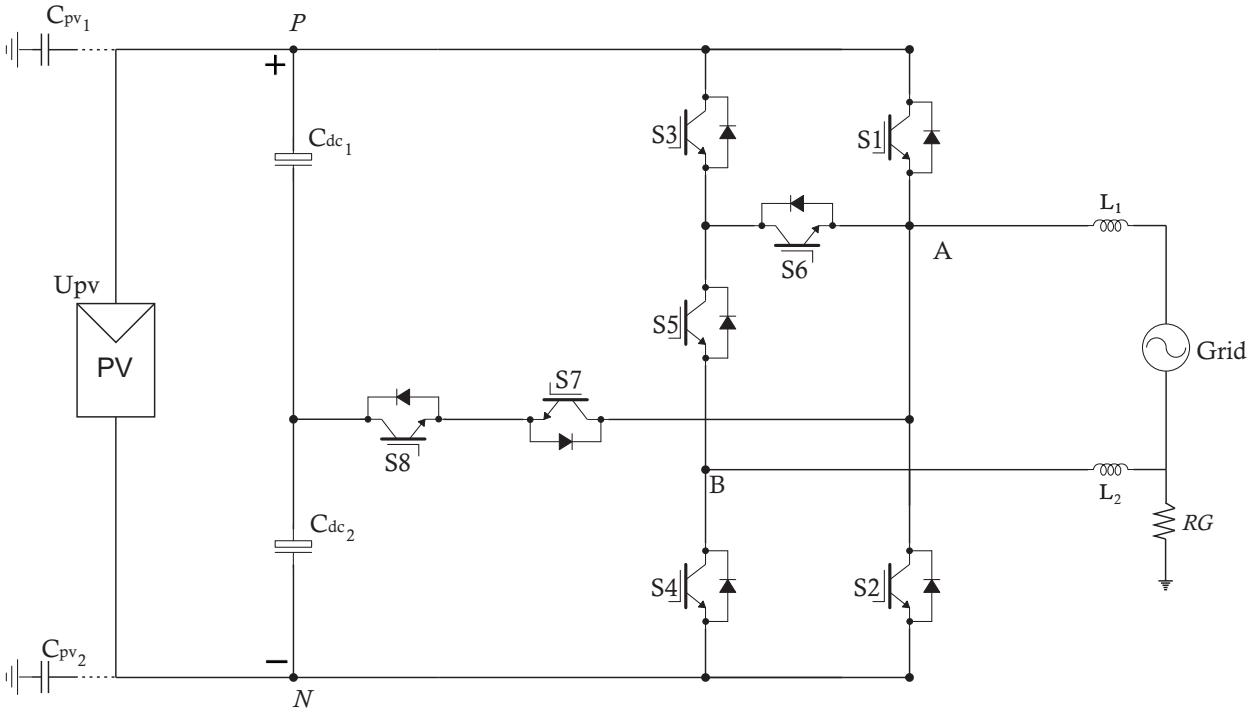

FIGURE 9. Proposed new topology.

current synchronized with the grid voltage at the inverter output to obtain a high power factor. Therefore, the current loop must be fast enough to produce the current without significant distortions. On the other hand, the voltage loop that uses a PI compensator ($C_v(s)$) aims to keep the DC bus voltage of the inverter constant, adjusting when variations in the irradiance of the photovoltaic array occur. Therefore, the voltage loop must be slow enough to decouple the current control loop dynamically. So, the outer loop controller must be tuned at least a decade below the inner loop controller.

The diagram of the control strategy used for the proposed inverter is illustrated in Fig. 11.

The converter system was built in the *Typhoon 604* virtual environment, with the control implemented in a Texas Instruments F28335 DSP. Fig.12 displays the control operation, showing the synchronism between the injected current and the grid voltage, achieving a very high power factor (left) and the stability of the DC bus voltage (right).

The I-V and P-V curves, referring to the *strings* used in the simulation, are in Fig.13. The Perturb and Observe (P&O) maximum power point tracking (MPPT) algorithm was used in this simulation.

Fig. 14 shows the effect of changing the number of levels at the inverter output. The operation starts with five levels and a parasitic capacitance of value $50nF$, considering that the panels are installed in a sunny and lightly humid environment [41]. The leakage current is within the acceptable limits, as shown in point A. Then, a disturbance was introduced at point B, varying the values from $50nF$ to $75nF$. This change in parasitic capacitance represents a climatic transition from a sunny, lightly humid environment to moderate rainfall. In heavy rain, these values can reach $167nF$ [41], [42], resulting in the leakage current values above the allowed by the standards. The system recognizes the current increase and starts processing the PWM to adjust the operating values. After 200 ms, the inverter selects a new PWM pattern, reducing the leakage current values that return to below standard limits by changing the output voltage to three levels, as shown in point C.

The advantage of three-level modulation is naturally the minimization of leakage current. Compared to five-level modulation, its disadvantage is the increase in current distortion and the more significant stress on the filter and switches (due to the higher current), as shown in Tab. 5.

TABLE 5. Results of injected current and THD for different levels.

Description	3 Levels	5 Levels
THD Current injection (to 50ª harmonic)	3.07%	2.03%
THD Current injection on Grid	3.58%	2.73%
Current Injection on Grid (RMS)	9.73A	8.53A

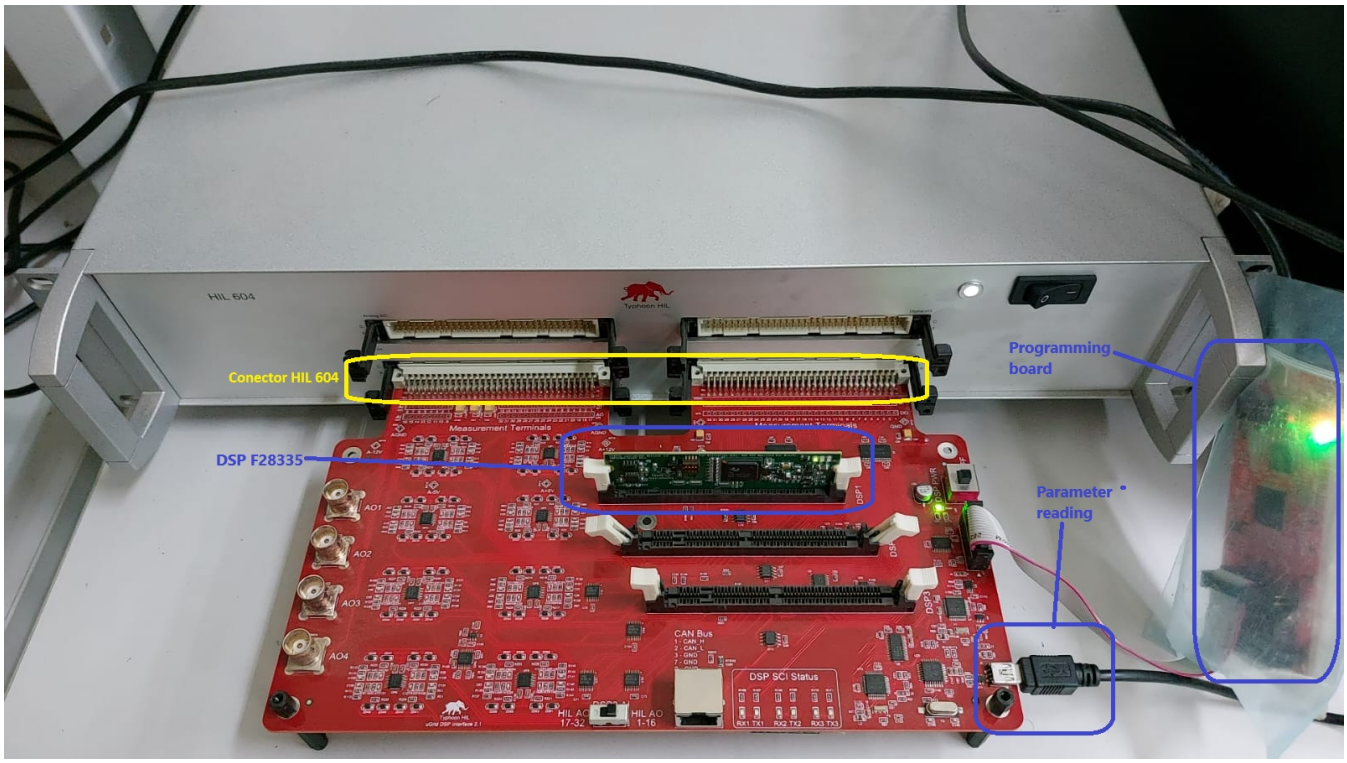

FIGURE 10. Typhoon HIL Setup Test.

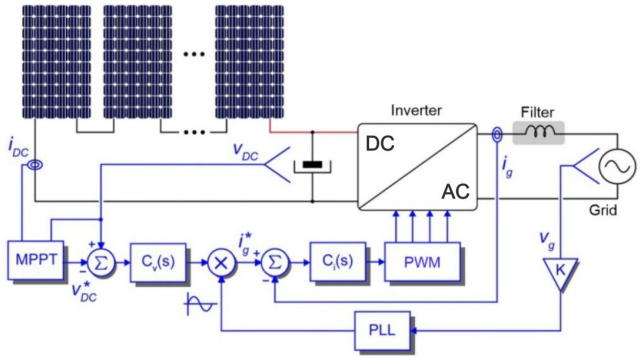

FIGURE 11. Control structure of the DC-AC converter.

Therefore, it is preferable to operate with five levels whenever possible, changing to three levels in the event of excessive leakage current. A management strategy monitors the leakage current and chooses the best output voltage form.

To compare the topologies presented and prove a sound performance of the proposed topology, an analysis of the relevant quantities for the study of leakage current in photovoltaic systems connected to the transformerless grid was carried out, presented in Tab. 6.

The High leakage current negatively impacts the quality of the energy injected into the grid by increasing the spectral content of the current and compromising residual current monitoring systems, which are critical for ensuring safety. The simulation analysis revealed that each topology presents distinct advantages and limitations.

The unipolar mode of the Full-Bridge topology, the focus of this study, achieves an efficiency above 90% and reduced switching losses due to its lower semiconductor requirements, delivering a three-level output. Despite these advantages, this configuration exhibits a high leakage current and a total harmonic distortion (THD) exceeding regulatory limits, making its operation unfeasible without appropriate mitigation techniques.

Derived topologies, such as HERIC and HB-ZVR, stand out for their efficient decoupling of the DC and AC sides, ensuring low leakage current and three-level output voltage. In contrast, the NPC and T-type topologies, both operating with five levels, offer satisfactory power quality with low leakage current and are less complex compared to the Floating Capacitor inverter, which demands a more robust control strategy to regulate its voltage and maintain efficient performance across its five levels of operation.

The proposed topology outperformed all others in the five-level operation mode and demonstrated a seamless transition to three levels, maintaining response times within the recommended limits. In the three-level mode, it exhibited competitiveness by achieving low leakage current and THD, while requiring a number of semiconductors comparable to the HERIC and HB-ZVR topologies.

VI. CONCLUSION

This paper proposed a novel transformerless inverter topology for PV power systems to minimize leakage currents and improve the system's reliability. Under normal conditions,

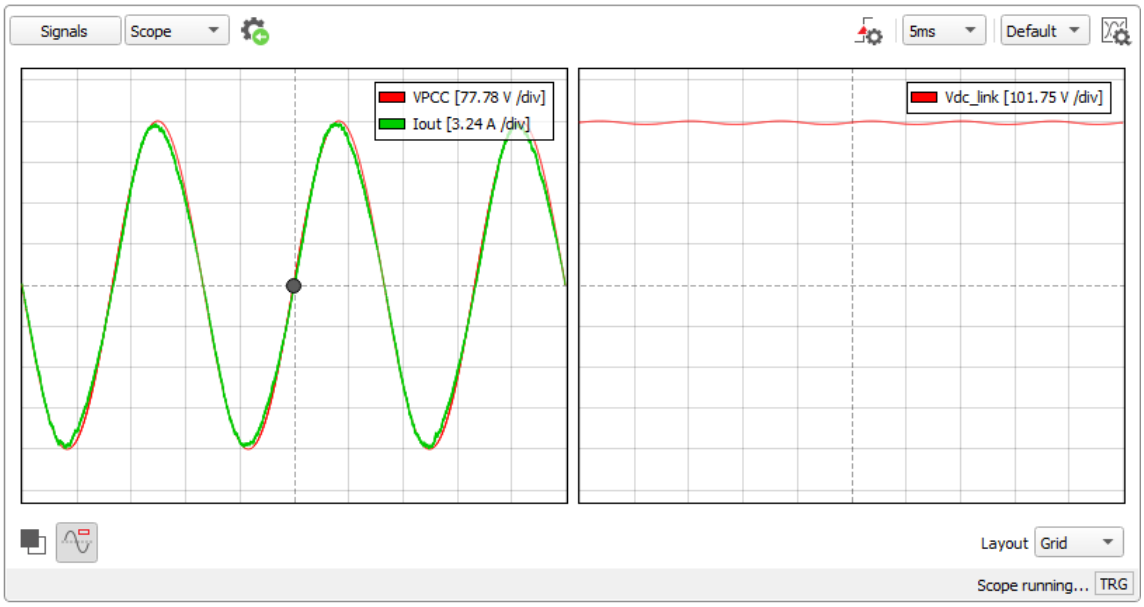

FIGURE 12. Inverter control results in the HIL environment.

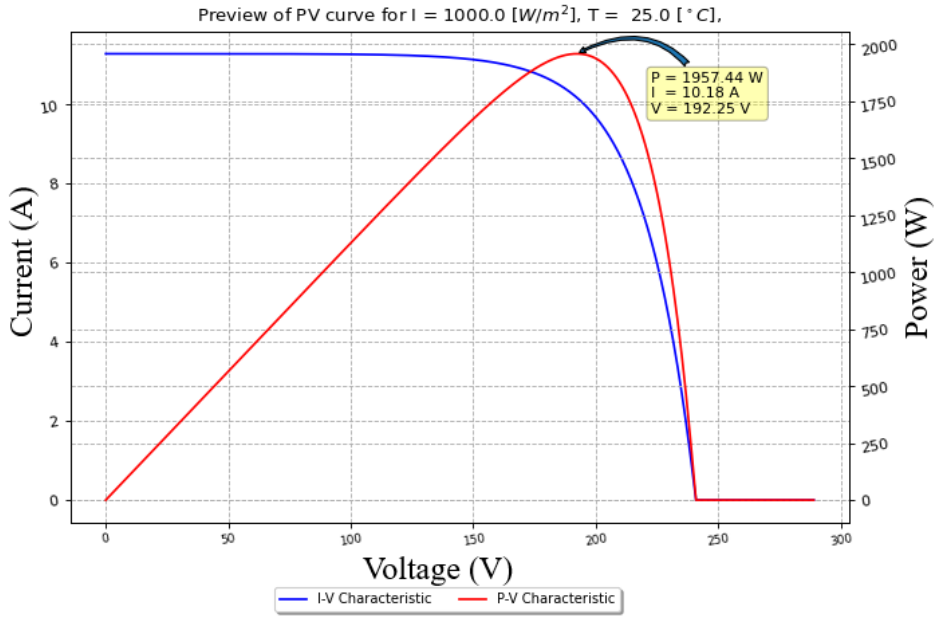

FIGURE 13. I-V and P-V curves of the photovoltaic system with P&O MPPT.

TABLE 6. Comparative results of closed-loop topology simulations.

Topology	Switches	Diodes	Levels	Icm (mA RMS)	THD (%)	Efficiency (%)
Full-Bridge - Unipolar	4	0	3	2168	7.83%	94.16%
HERIC	6	0	3	19.79	3.54%	95.65%
HB-ZVR	5	5	3	20.01	3.72%	94.34%
NPC - 5 levels	8	4	5	69.38	2.89%	95.90%
T-TYPE - 5 levels	8	4	5	69.55	2.93%	95.95%
Floating Capacitors - 5 levels	8	0	5	80.45	2.96%	96.03%
Proposed topology - 3 levels	**6**	**0**	**3**	**37.63**	**3.58%**	**95.60%**
Proposed topology - 5 levels	**8**	**0**	**5**	**97.04**	**2.73%**	**96.87%**

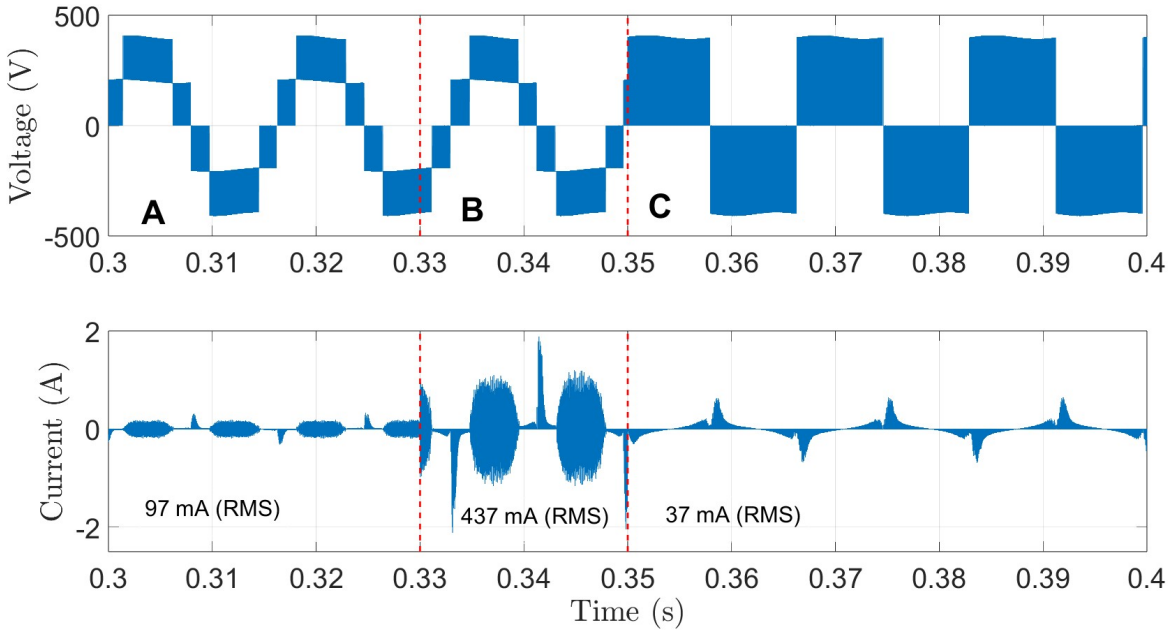

FIGURE 14. Results of level variations in response to leakage current.

the inverter operates with a five-level modulation strategy, ensuring high-quality performance. When leakage currents exceed standard upper limits, the topology is adapted by transitioning to a three-level configuration, utilizing a neutral clamping point to mitigate the issue effectively. By adopting six switches instead of eight, the design strikes a balance between reducing switching losses and maintaining efficiency. This flexible approach improves system availability, ensures compliance with standards, and provides a robust solution for modern photovoltaic applications.

As analyzed in the article, the *Full-Bridge* topology lacks an integrated leakage current mitigation mechanism, resulting in values exceeding normative limits for both leakage current and THD of grid-injected currents. This limitation demands advanced filtering techniques, significantly increasing system complexity and project costs. In contrast, The *HERIC* and *HB-ZVR* topologies incorporate mechanisms to stabilize the common-mode voltage, effectively suppressing leakage currents and improving the quality of the grid-connected output current.

Regarding five-level topologies, the *NPC - five levels* are introduced, offering the advantage of generating output voltage with minimal harmonic distortion. The *T-type - five levels* topology is also highlighted, recognized as a promising choice for photovoltaic applications due to its superior efficiency, reduced conduction losses, and fewer semiconductor components than other multilevel configurations. Lastly, the *Floating Capacitors* (Floating C) topology stands out for minimizing the number of semiconductor devices in the current path, effectively lowering both conduction and switching losses compared to alternative multilevel topologies.

For future work, we plan to assess the conversion efficiency of the proposed topology and conduct performance comparisons with well-established topologies from the literature, utilizing simulations and validation on a test bench.

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PLAGIARISM POLICY

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