Eletrônica de Potência
Open Journal of Power Electronics

Received November 13, 2024; accepted April 04, 2025; Date of publication April 16, 2025.
The review of this paper was arranged by Associate Editor Levy F. Costa and Editor-in-Chief Heverton A. Pereira.
Digital Object Identifier http://doi.org/10.18618/REP.e202533

Regular Extreme Fast Charging Station for E-buses with Low Current Harmonic Content

Dener A. de L. Brandao[1,*], **Thiago M. Parreiras**[2], **Igor A. Pires**[3], **Braz de J. Cardoso Filho**[4]

[1]Universidade Federal de Minas Gerais, Graduate Program in Electrical Engineering - Av. Antônio Carlos 6627, Belo Horizonte, MG, Brazil;
[2]Centro Federal de Educação Tecnológica de Minas Gerais, Department of Electrical Engineering, Belo Horizonte 30510-000, Brazil.
[3]Universidade Federal de Minas Gerais, Department of Electronic Engineering, Belo Horizonte, Brazil
[4]Universidade Federal de Minas Gerais, Department of Electrical Engineering, Belo Horizonte, Brazil.

e-mail: dalbrandao@ufmg.br*; thiago.parreiras@cefetmg.br; iap@ufmg.br; braz.cardoso@ieee.org.
*Corresponding author.

ABSTRACT Public transport vehicles based on electric vehicles are suitable for regular extreme fast charging (R-XFC) with supercapacitors as energy storage. Quick recharges cause power quality problems such as high harmonic injection. In this sense, grid-connected converter solutions must address this issue. The main objective of this paper is to present a solution for R-XFC stations with the Zero Harmonic Distortion (ZHD) Converter. The ZHD converter features elements consolidated in the industry and it does not need capacitive filters in the point of common coupling (PCC) with the grid, presenting sinusoidal currents with low harmonic content for regular extreme fast charging (R-XFC) stations. Hardware-in-the-loop (HIL) simulation results of an extreme fast recharge showed a total demand distortion (TDD) of 0.54%, and experimental results of a 280 kVA prototype had a TDD of 2.29%.

KEYWORDS extreme fast charging, vehicle charger, regular extreme fast recharge, electric vehicles, e-bus, TUPF, ZHD, energy storage.

I. INTRODUCTION

An alternative structure for electric public transport is the regular extreme fast charging (R-XFC) station. Usually, public transport buses have pre-defined stops, which allow the installation of R-XFC stations in specific locations. Based on this, the authors at [1] show the design of an electric minibus with hybrid storage of batteries and supercapacitors, with recharges providing autonomy of almost 1 km in 50 seconds. Since 2009, there have been bus projects in China with supercapacitors for extreme fast recharges that reach 5 to 8 km per recharge in a few minutes [2]. E-buses using up to 40 kWh supercapacitors can be found as a commercial alternative to compound an electric vehicle fleet [3].

Due to the high power of XFC stations, problems with the injection of harmonics into the grid are more evident. The high injection of harmonics into the grid caused by extreme fast recharge systems would be able to change the original resonance point of the Dutch transmission grid of Bronsbergen from 1600 Hz to 1250 Hz, reached by the characteristic harmonics of 12-pulse converters [4]. Resonances could generate overvoltages and overcurrents in the transmission line, damaging the electric system, and increasing losses. In [5], the authors show the impact of an ultra-fast charging station for electric buses. Some of the individual harmonic levels of the input current exceed the limits established by IEEE 519-2022 [6], mainly for low-order harmonics. These power quality issues are the subject of studies on prediction, modeling, and control for the mitigation of these harmonics [7], [8].

Thus, international standards and recommendations such as IEC 61000-3-6 [9] or IEEE-519-2022 define maximum limits for harmonic amplitudes in the electrical grid and limits for indices such as total harmonic distortion (THD) for voltage harmonics and total demand distortion (TDD) for current harmonics. In this context, a grid-connected converter that meets the harmonic injection standards is recommended.

For high-power applications such as R-XFC stations, the 12-pulse three-phase diode bridge can be used as a grid-connected converter. However, this solution has low power quality due to the high harmonic content of its current, requiring an ac filter and a bulky dc filter, besides not allowing the control of the output voltage [10].

Topologies such as Neutral Point Clamped (NPC) converter, Vienna rectifier, and Swiss rectifier are also presented as alternatives but, in general, require LCL filters to reduce the harmonic content [11]–[19]. When these topologies work at high frequency, problems such as high switching losses and electromagnetic interference arise. By reducing the frequency, the LCL passive filters connected to the grid become bulkier, create resonance points, and increase application costs [20].

Topologies that do not require second-order filters are more attractive to avoid points of resonance in the grid. Using a substantial number of levels enables the elimination

TABLE 1. Comparison between proposed topologies for extreme fast charging stations.

Grid-connected converter	LC Filter?	Diodes/Switches	Switches Technology	f_{sw} (kHz)	Sim. Power (kW)	Exp. Power (kW)	THD_i (%)
Conventional 2-level [11]	✓	0/6	SiC	100	50	✗	4.04[a]
Conventional NPC [12]	✗	6/12	Si	1.08	240	1.2	2.46[a]/✗
NPC 4-leg [13]	✓	8/16	Si	2.16	1200	3.6	5.39[a]/5.8[b]
Conventional Vienna [14]	✗	6/6	Si	12/50	60	1.865	3.27[a]/3.5[b]
Vienna 3-sw. [11]	✓	18/3	SiC	100	50	✗	1.26[a]
Vienna 6-sw. [11]	✓	12/6	SiC	100	50	✗	1.26[a]
Parallel Vienna [15]	✗	12/6	Si	15	30	6.0	0.847[a]/7.11[b]
Swiss [17]	✓	8/8	SiC	90	✗	10	4.9[b]
5-level E-type [22]	✗	12/36	Si	20	✗	25	4.7[b]
MMCC [26]	✓	120/120	Si	1.0	600	✗	1.25[a]
Proposal: ZHD converter	✗	**0/18**	**Si**	**1.14**	**280**	**280**	**0.54[a]/2.29[b]**

[a] Simulation results. [b] Experimental results.

of a second-order ac filter [21]. The authors in [22] use a 5-level E-type rectifier as a grid-connected converter in an ultra-fast charger for electric buses. However, even with a switching frequency of 20 kHz and a multilevel converter, the current THD reached 4.7%.

One solution that could be used in XFC stations is the Modular Multilevel Cascaded Converter (MMCC). It could be used in various applications for transportation electrification, such as rail interties, railway power conditioner, and propulsion systems [24]–[26]. However, galvanic isolation is necessary to protect consumers, avoiding electric shocks, in compliance with IEC 62955:2018 and IEC 61851-1:2017 regulations and IEEE Std 2030 [27]–[29], which requires the use of a transformer in MMCC solution, such as the solid-state transformer [18]. In addition, the MMCC has a high number of components, bringing additional reliability and control challenges.

Table 1 presents a comparison of various aspects of different papers with topologies and prototypes focusing on extreme fast charging stations. The performance of all mentioned systems is strongly dependent on the control scheme and parameters, as it is in the proposed system. The power quality metrics in XFC based on the converter proposed in this paper are achieved through proper modulation strategy and control implementation as discussed in the following sections. Therefore, an analysis of the control adequacy for the several mentioned systems is not within the scope of this paper.

Figure 1 illustrates the Zero Harmonic Distortion (ZHD) converter, which serves as an alternative to XFC stations. Introduced in [30], the ZHD converter is designed with a minimal component count and utilizes industry-standard elements. It also operates at a low switching frequency (1.14 kHz for 2-level converter), which is crucial for minimizing losses in converters that use high-power *Si* switches. Notably, it does not require capacitive filters at the point of common coupling (PCC), ensuring sinusoidal currents with low harmonic distortion. This design eliminates harmonics

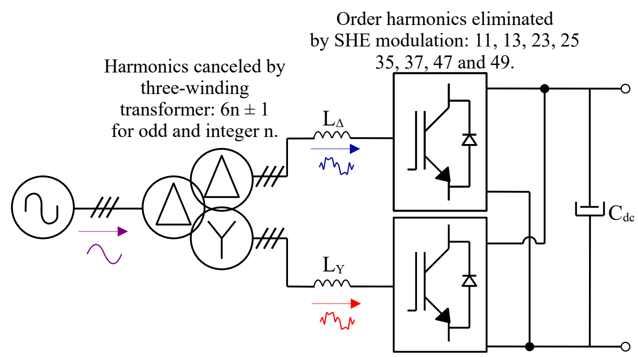

FIGURE 1. Zero Harmonic Distortion converter.

up to the 50th order, aligning with the IEEE 519-2022 recommendation [6].

The topology consists of a three-winding transformer with a 30-degree angular phase shift between the secondary windings, which cancels harmonics of the order $6n \pm 1$ It includes input reactors to attenuate the amplitude of harmonics present in the secondary windings and employs two- or three-level converters that utilize 9-pulse selective harmonic elimination pulse width modulation (SHE PWM) combined with dq-axis current control. The 9-pulse SHE PWM effectively eliminates harmonics of the order $12n \pm 1$.

Table 2 summarizes the key publications on the ZHD converter, previously referred to as the True Unity Power Factor (TUPF) converter. Despite advancements in ZHD current control and full-scale experimental validation, its application as a grid-connected converter for vehicular applications remains limited. The study by [20], which precedes this work, explores the use of the ZHD converter for regular extreme fast charging of electric buses. However, it does not address the control of the ZHD for this application nor provide details on the control of the DC-DC converter.

The main contribution of this paper is to address the gaps in [20] by providing detailed information on the voltage

TABLE 2. Main publications of ZHD converter (formerly True Unit Power Factor - TUPF).

Reference	Main area	Application	ZHD voltage control?	DC-DC converter control?	ZHD closed-loop experimental results?	Prototype power
[30][a]	Power systems	Not specified	✗	-	✗	No data
[20]	Vehicular	Electric charger	✗	✗	✗	No data
[31]	Mining industry	Electric drive system	✗	-	✗	No data
[32]	Power systems	Wind system	✓	-	✗	30 kW
[33]	Metal industry	Electric drive system	✓	-	✓	30 kW
[34]	Metal industry	Static compensator	✓	-	✓	280 kW
[35]	Metal industry	Not specified	✓	-	✓	280 kW
[36]	Power systems	Islanded microgrids	✗	-	✓	4 kW
[37]	Power systems	Islanded microgrids	✗	-	✗	-
This paper	**Vehicular**	**Electric charger**	✓	✓	✓	**280 kW**

[a] First study of the ZHD converter, still named TUPF.

and current controllers of the ZHD converter and the DC-DC converter, the design of the e-bus capacitor bank, and presenting hardware-in-the-loop simulations along with experimental results using a full-scale prototype of the ZHD converter. This paper also presents the power losses and efficiency of the ZHD converter prototype.

This paper is divided into six sections: after the Introduction, section II presents the characteristics of the selective harmonic elimination pulse width modulation (SHE PWM). Section III discusses the control design of the converters present in the R-XFC station. Sections IV and V present the hardware-in-the-loop and experimental results, respectively, and the conclusions are presented in Section VI.

II. SELECTIVE HARMONIC ELIMINATION

The SHE PWM used in the ZHD converter was initially proposed in [38] and improved in [39]. It consists of modifying the switching angles of the switches throughout the operation cycle, to eliminate harmonics up to $M-1$, where M is the number of switching state changes per half-cycle. The calculation of the switching angles depends on the number of converter levels, the number of harmonics to be eliminated, and the modulation index. It can be expressed in Fourier Series as shown in (1), which needs to be solved to meet a desired modulation index (m_i) while eliminating the chosen harmonics. Figure 2 presents a generic 2-level SHE PWM waveform.

$$\begin{bmatrix} 1-2cos(\alpha_1)+\cdots+2(-1)^M \cdot cos(\alpha_M) \\ 1-2cos(n_2 \cdot \alpha_1)+\cdots+2(-1)^M \cdot cos(n_2 \cdot \alpha_M) \\ \vdots \\ 1-2cos(n_i \cdot \alpha_1)+\cdots+2(-1)^M \cdot cos(n_i \cdot \alpha_M) \end{bmatrix} = \begin{bmatrix} m_i \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (1)$$

To find the solution for (1) it is necessary to use numerical methods, such as Newton's linear iteration method [30], [38] using the partial derivatives of $\vec{f}$ to improve the initial guess of the angles and find a solution.

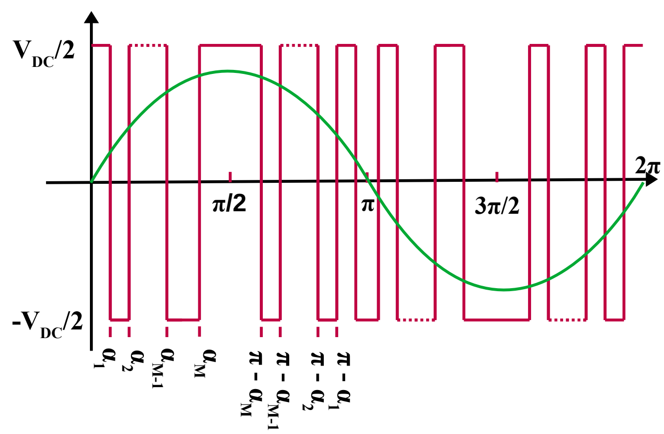

FIGURE 2. A generic 2-level SHE PWM waveform.

Switching angles are calculated offline using Newton's method, defined based on modulation indices, and stored in Lookup Tables (LUTs). SHE modulation needs high data processing to provide high-resolution switching angles. In this way, the ZHD control is subdivided into two parts, as shown in Fig. 4. DC bus voltage and grid current control loops are stored in a Digital Signal Processor (DSP). A Field-Programmable Gate Array (FPGA) performs the SHE PWM with superior processing based on the modulation rates sent by the DSP. The communication between the DSP and the FPGA is parallel, ensuring a high data exchange rate between the devices.

III. CONTROL DESIGN

Fig. 3 shows the schematic of the proposed solution for the R-XFC station using the ZHD converter emulated in the real-time simulation environment. Subsections A and B presents the ZHD converter control design and 3-arm interleaved DC/DC converter control design.

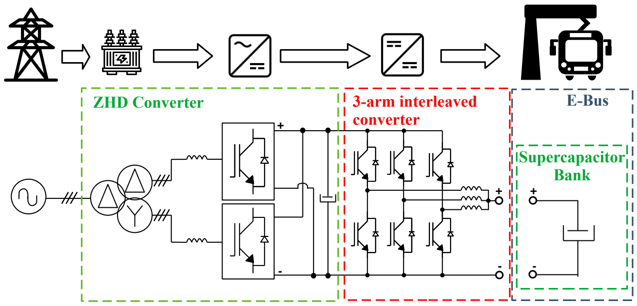

FIGURE 3. Proposed solution for extreme fast charger using ZHD.

A. ZHD control design

Fig. 4 shows the ZHD control. The current controller is composed of feedback control strategies, feed-forward command, axis decoupling, and a combination of the open-loop system with an estimate of the plant parameters. Based on the dynamic stiffness [40], the gains of the current controller are calculated so that the poles of the system are spaced in a decade and keep the SHE PWM technique working satisfactorily [33]. The expression for dynamic stiffness is presented in (2).

$$\frac{V^{dq}(s)}{I^{dq}(s)} = sL + K_p^{dq} + \frac{K_i^{dq}}{s} \tag{2}$$

The voltage controller sends the active power reference to the current controller. The controller chosen was the classic PI, combined with feed-forward strategies to anticipate disturbances in the current drained from the DC link and variations in the voltage reference.

The dc link voltage disturbance is the current drain. This current drained from the dc link has high-frequency components that impact the cascade current control. According to [33], the commands to the modulator must be slower than the frequency on the rotary axis dq of the first non-eliminating harmonics (720 Hz). Therefore, set the moving average filter dynamics at 50 Hz, at least a decade below the modulator. Equation (3) represents the mathematical model of the dynamic stiffness curve of the system for controller tuning.

$$\frac{I_{dc}(s)}{V_{dc}(s)} = sC_{eq} + k_{pv} + \frac{k_{iv}}{s} \tag{3}$$

Figure 5 presents the curves of dynamic stiffness for the ZHD converter current loop control and voltage loop control. Equations (4) and (5) present the tuning for current controller and voltage controller, respectively. Table 3 shows the controller gains.

$$K_{pdq} = \omega_{2i} L \text{ and } K_{idq} = \omega_{1i} K_{pdq} \tag{4}$$

$$K_{pv} = \omega_{2v} C \text{ and } K_{iv} = \omega_{1v} K_{pv} \tag{5}$$

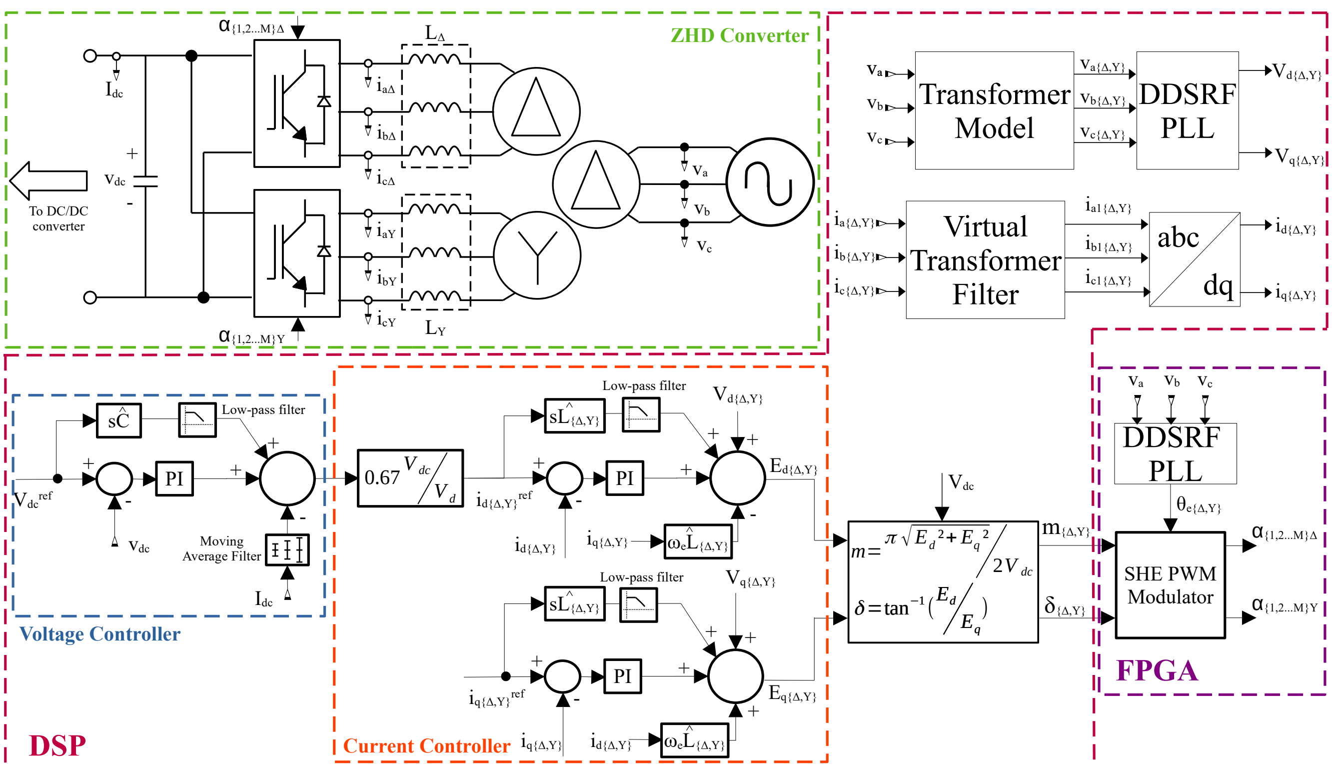

FIGURE 4. Schematic of controller in dq coordinates for the converters connected to the △ and Y bridges.

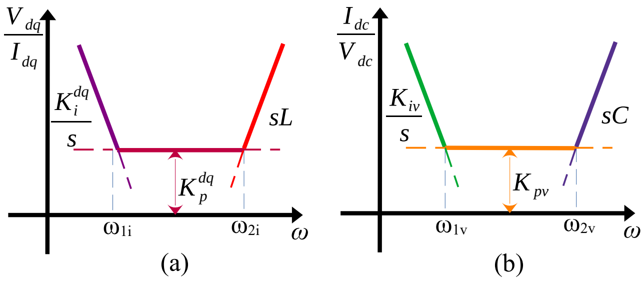

FIGURE 5. Dynamic stiffness curves for ZHD converter: (a) Current control. (b) Voltage control.

TABLE 3. ZHD Converter controllers adjust.

Parameter	Controller Values		
	Current Controller		Voltage Controller
	d-axis	q-axis	
Poles Frequency	72 Hz	{72, 7.2} Hz	{7.2, 0.72} Hz
Proportional Gains	0.18 Ω	0.18 Ω	0.5 S
Integral Gains	-	8.15 $\Omega \cdot s^{-1}$	2.2 $S \cdot s^{-1}$

B. 3-arm interleaved DC/DC converter control design

The dc/dc interleaved converter performs the interface between the dc link and the e-bus supercapacitor bank due to its simplicity, high current capacity, and reduced output current ripple [41]. Furthermore, non-isolated converters have greater efficiency than isolated converters [18] and galvanic isolation is guaranteed by the transformer present in the ZHD converter.

Fig. 6 presents the 3-arm interleaved dc/dc converter controller. It is important to emphasize that the current controller must be individual per converter arm. The reference of the current control loops of each arm comes from the output of the voltage controller. This output, in turn, is limited by a saturator with the maximum current value for the application. Such approach, performed in [42] for supercapacitor recharging, allows a simple Constant Current - Constant Voltage (CC-CV) charge control [43]. In addition, feed-forward actions anticipate supercapacitors' voltage disturbances and reference current variations.

Dynamic stiffness of the current controller, expressed by (6), defines the integral (K_{iib}) and proportional (K_{pib}) gains of the current controller. For current control, the disturbance is the variation of the voltage of the supercapacitor bank (V_{Cap}), and the output is the current in the inductor (I_L) according to (6). L_{dc} represents the inductance of the dc/dc converter.

$$\frac{V_{Cap}(s)}{I_L(s)} = sL_{dc} + K_{pib} + \frac{K_{iib}}{s} \tag{6}$$

The desired voltage for e-bus recharge defines the voltage controller reference of the dc/dc converter. The controller is composed of a classic PI with anti-windup due to the saturation of the controller output. Feed-forward strategies are used to anticipate variations in the reference voltage.

The dynamic stiffness of the voltage controller, shown in (7), defines the proportional (K_{pvb}) and integral (K_{ivb}) gains. For the presented system, the disturbance is the discharge current (I_{Load}) for the e-bus electrical and electronic systems. C_{eq} is the equivalent capacitor formed by the e-bus capacitor bank.

$$\frac{I_{Load}(s)}{V_{Cap}(s)} = sC_{eq} + K_{pvb} + \frac{K_{ivb}}{s} \tag{7}$$

Figure 7 presents the curves of dynamic stiffness for the 3-arm interleaved converter current loop control and voltage loop control. Equations (8) and (9) present the tuning for current controller and voltage controller, respectively. Table 4 shows the controller gains.

$$K_{pib} = \omega_{2ib} L_{dc} \text{ and } K_{iib} = \omega_{1ib} K_{pib} \tag{8}$$

$$K_{pvb} = \omega_{2vb} C \text{ and } K_{ivb} = \omega_{1vb} K_{pvb} \tag{9}$$

IV. HIL RESULTS

Table 5 shows the parameters of the ZHD converter based on a laboratory prototype. Table 5 also shows the main parameters of the dc/dc converter used in the extreme fast charger.

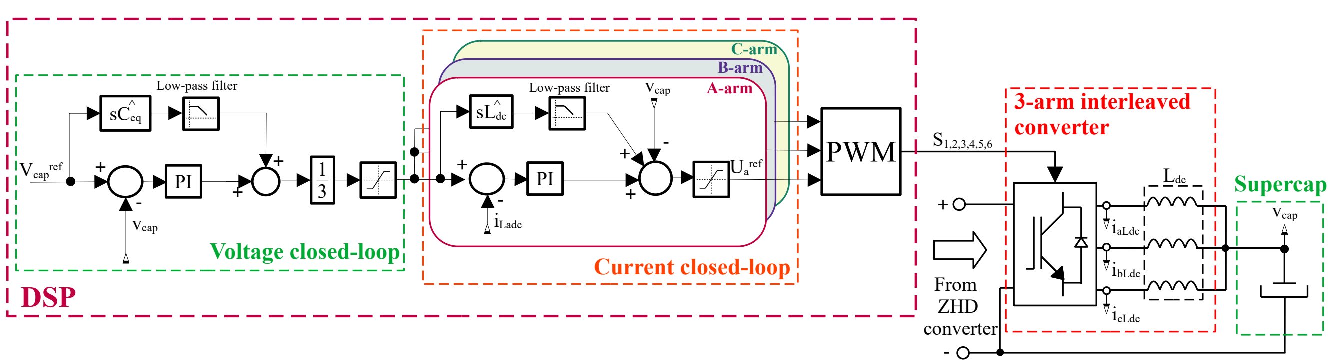

FIGURE 6. Schematic of the 3-arm interleaved dc/dc converter controller.

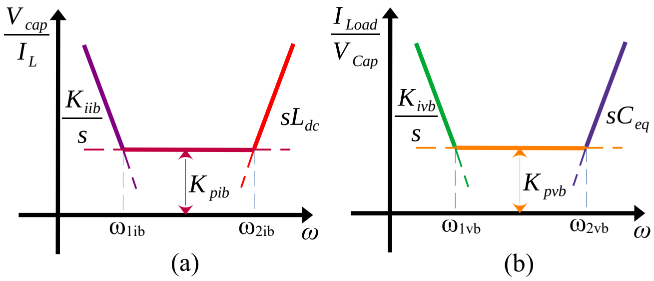

FIGURE 7. Dynamic stiffness curves for 3-arm interleaved converter: (a) Current control. (b) Voltage control.

TABLE 4. 3-arm interleaved converter controllers adjust.

Parameter	Controller Values	
	Current Controller	Voltage Controller
Poles Frequency	{500 Hz, 50 Hz}	{5, 0.5} Hz
Proportional Gains	1.88 Ω	3040 S
Integral Gains	592 $\Omega \cdot s^{-1}$	9551 $S \cdot s^{-1}$

The supercapacitor bank was designed based on AVX manufacturer SSC LE Series ultracapacitor [45]. Considering the manufacturer's recommendation of the maximum excursion of 50% of the voltage in the supercapacitor, a 3.37 kWh bank was designed, as shown in Table 6.

In the 3-arm interleaved dc/dc converter, the difference between reactors was introduced to compensate for the leakage inductance difference between transformer windings. Three half-bridge arms with carriers shifted by 120° compose the 3-arm interleaved dc/dc converter. The current in the inductor of each arm is three times lower than the output current of the supercapacitor bank. Equation (10) defines the inductance

TABLE 5. ZHD converter and 3-arm interleaved dc/dc converter parameters.

ZHD Converter		
Element	**Parameter**	**Value**
Grid	Voltage [V]	440
	Frequency [Hz]	60
Transformer	Nominal power [kVA]	305
	Primary voltage [V]	506
	Secundaries voltage [V]	440
	Connection	Dd0y1
ac reactors	Δ/Y inductance [μH]	590/506.8
dc link	Capacitance [mF]	10.5
	dc link voltage [V]	700

DC/DC Converter		
Parameter	**Symbol**	**Value**
Input voltage	V_i	700 V
Switching frequency	f_{sw}	5 kHz
Max power	$P_{charger}$	308 kW
Output voltage	V_o	250 to 500 V
Output current	I_o	570 A
Output current ripple	ΔI_o	3%
dc inductance per arm	L_{dc}	600 μH

TABLE 6. Capacitive cell and ultracapacitor bank characteristics.

Cell voltage	2.7 V
Cell capacitance	500 F
Cell series resistance	1.6 mΩ
Strings in parallel/series	36/186
Initial and final bank voltage	250-500 V
Bank capacitance (C_{eq})	97 F
Bank series resistance	8.3 mΩ

per arm, where N is the number of arms, f_{sw} is the switching frequency, V_{in} is the input voltage, and V_o and ΔI_o are the output voltage and current ripple, respectively.

$$L_{dc} = \frac{V_o - V_o^2/V_{in}}{\Delta I_o.N.f_{sw}} \tag{10}$$

Fig. 8 shows the Typhoon Hardware-in-the-loop (HIL) 604 test bench. A TMS320F28335 DSP [46] performs the 3-arm interleaved dc/dc converter control. Another TMS320F28335 DSP performs the control of the ZHD converter in a communication with a MAX 10 FPGA [47], which performs the SHE PWM and PLL algorithm at a sufficiently fast sample frequency (250 kHz). The modulation index and the space vector angle are encoded in unsigned 10 bits and signed 13 bits, respectively, and sent simultaneously over a 23-bit parallel channel from the FPGA to the DSP. There is no traditional communication protocol between the DSP and the FPGA, only a 23-bit parallel synchronous communication with a 2.58 kHz clock.

The PLL algorithm has a significant influence on the control performance of converters connected to grids increasingly disturbed by the presence of nonlinear loads and sources, which has driven extensive research aimed at proposing increasingly robust and reliable PLLs [48]. In this paper, the Double Decoupled Synchronous Reference Frame PLL (DDSRF-PLL) was chosen, as it is capable of accurately

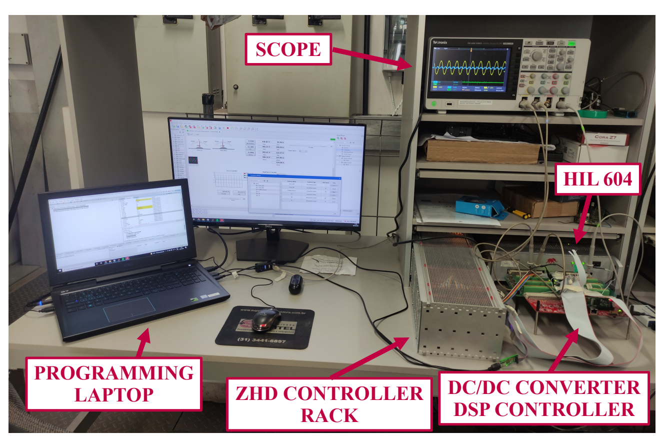

FIGURE 8. HIL bench for extreme fast charger implementation.

tracking the positive sequence angle in unbalanced grids and demonstrated good performance even in highly distorted electric grids [49].

Fig. 9 shows the dc link voltage of the ZHD converter and the supercapacitor voltage and current during the 46 second charging period. The current in the supercapacitor remains constant during most of the charging period until it reaches zero when the voltage across the capacitor reaches 500 V. It is also possible to highlight the automatic change from the constant current mode to the constant voltage mode near the end of the recharge.

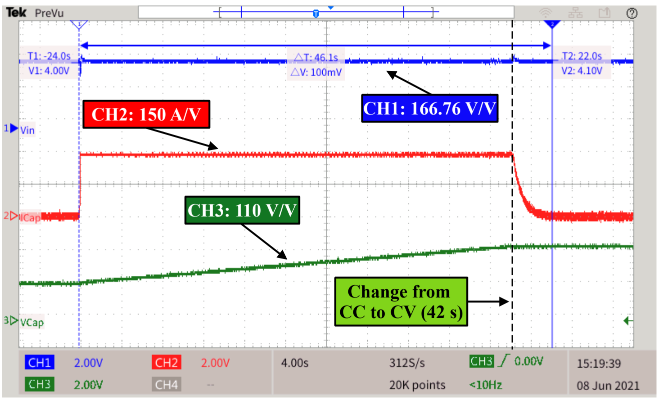

FIGURE 9. ZHD dc link voltage (CH1), supercapacitor current (CH2) and voltage (CH3).

Fig. 10 shows the currents in the supercapacitor and arms of the dc/dc converter. The ripple in the supercapacitor current is 24 A, three times less than the ripple in each converter arm (72 A). Fig. 11 shows the voltage and currents on the grid during supercapacitor recharge.

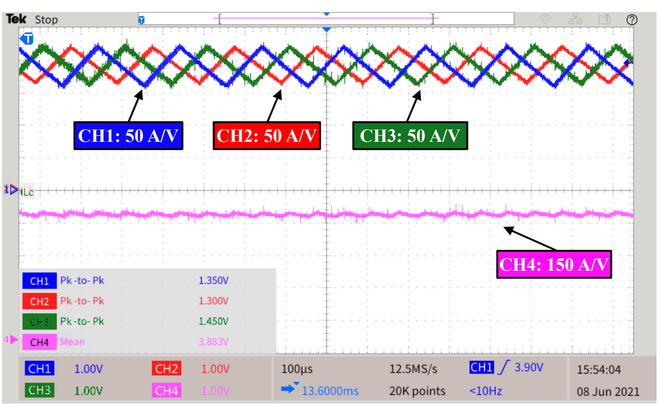

FIGURE 10. A-arm current (CH1), B-arm current (CH2), C-arm current (CH3) of dc/dc converter and supercapacitor current (CH4).

Fig. 12 shows a sinusoidal aspect of the currents in the grid due to the low harmonic content. There are no significant harmonics in the current phase A of the grid. Total demand distortion has a value of 0.54%.

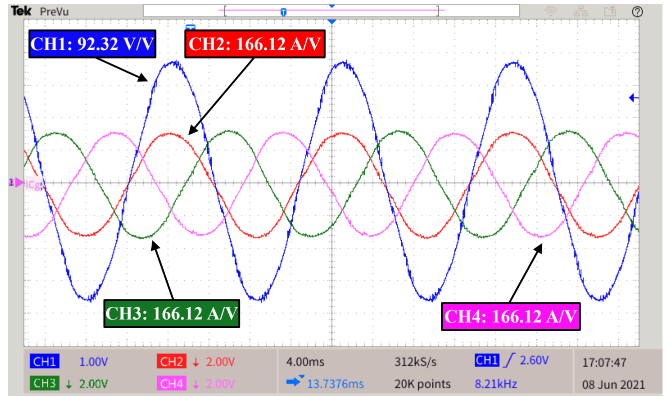

FIGURE 11. Grid voltage (CH1) and currents in phase A (CH2), phase B (CH3) and phase C (CH4) during supercapacitor recharging.

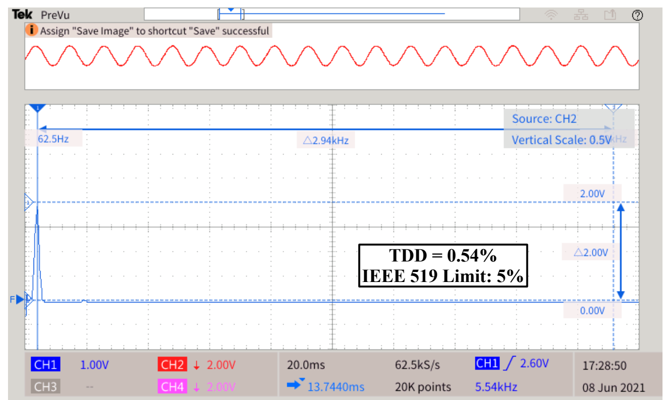

FIGURE 12. Harmonic content of the current in phase A of the grid.

V. ZHD EXPERIMENTAL RESULTS

A. Half Power Tests

In order to experimentally validate the grid side portion of the proposed solution, the 280 kVA 2-level Zero Harmonic Distortion converter of Fig. 13 was used. The IGBTs used in 2-level converters are the FS450R12KE3 model from Infineon. Fig. 14 shows the scheme of back-to-back test. The back-to-back test allows the converter to be submitted to full power without a load, using the grid to supply only the system losses and, therefore, saving energy during the tests.

For half power tests, the substation selector switch is connected to position 1, supplying the converter with 220 V. Figure 15 presents a dynamic ramp current variation test on the grid. The ramp was applied with a variation of 1173 A/s, ranging from 0 to 352 A in 300 ms. It can be observed that there is no current overshoot, and the system behaves smoothly. Figure 16 shows, in steady state, the voltage V_{AB} and the current in phase A of the transformer primary, in addition to the currents in the A phases of the secondaries in Δ and Y.

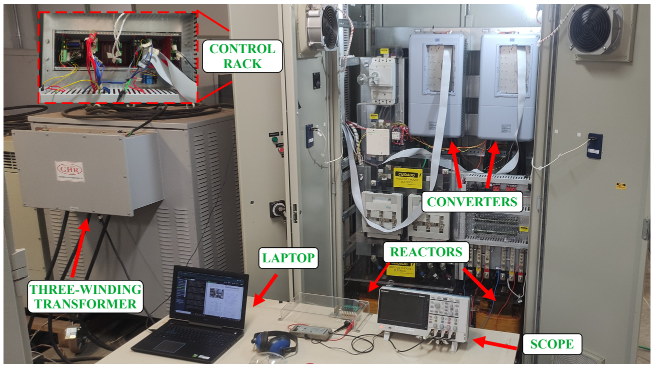

FIGURE 13. ZHD converter prototype.

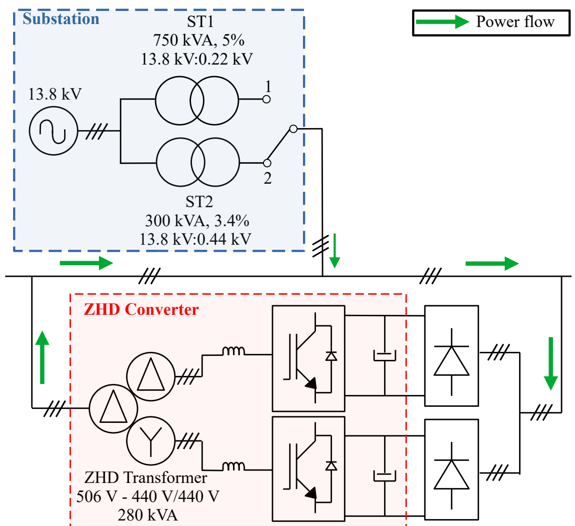

FIGURE 14. Back-to-back test scheme.

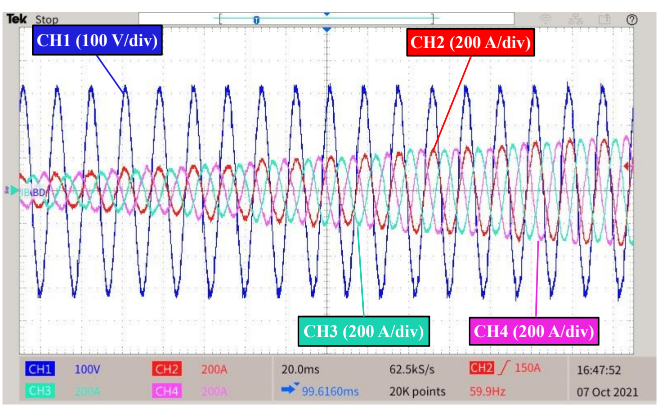

FIGURE 15. Ramp test: Grid Voltage V_{AB} (CH1) and line currents of the transformer primary (CH2, CH3 and CH4).

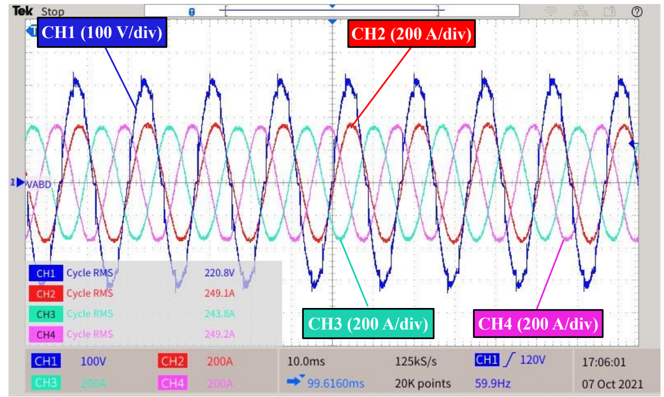

FIGURE 16. Half Power Test (steady state): Grid Voltage V_{AB} (CH1) and line currents of the transformer primary (CH2, CH3 and CH4).

B. Full Power Tests

For full power tests, the substation selector switch is connected to position 2. The substation transformer 2 (ST2) impedance is $8.88+j20.3\ m\Omega$ (X/R = 2.3 and SCR = 29.12), characterizing a strong grid. It is also worth noting that the power of the substation transformer is nearly the same as that of the prototype transformer. The use of non-linear loads, like a diode rectifier, close to the rated power of the electric grid increases its voltage distortion, as shown in Fig. 17. It is worth noting that the rectifier diode is not part of the ZHD converter.

Fig. 17 shows the voltage V_{AB} and the current in phase A in the transformer primary, in addition to the currents in the A phases of the secondaries in Δ and Y. The phase difference between the line voltage and line current is 30 degrees, as expected. Due to distortions caused by the rectifier diodes in the back-to-back test, the primary voltage has a distorted appearance. The currents in the secondaries are distorted due to the presence of harmonics of order $6n \pm 1$.

Despite the harmonic distortion of the grid voltage caused by the back-to-back test, the primary current has a sinusoidal aspect, corroborated by Fig. 18, which shows the harmonic content of the grid current. There is no harmonic content above the limits established by IEEE 519.

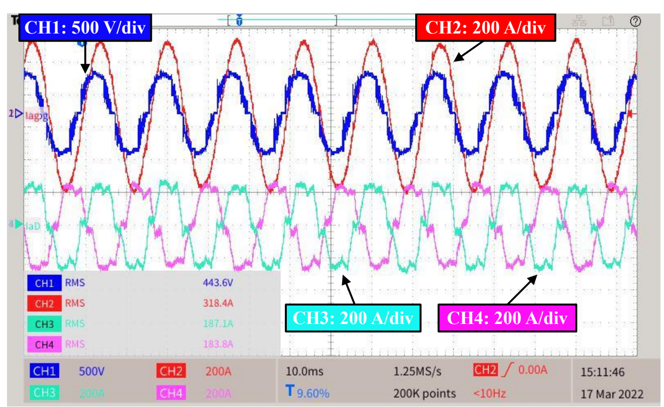

FIGURE 17. Grid Voltage V_{AB} (CH1) and phase A current of the transformer primary (CH2), in the secondary in Δ (CH3) and in the secondary in Y of the transformer (CH4).

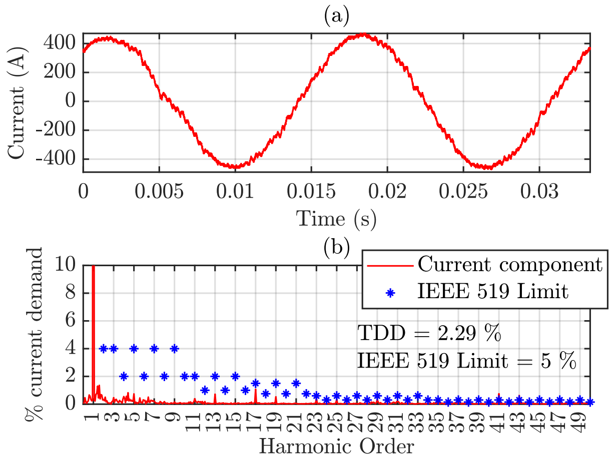

FIGURE 18. (a) Current in the transformer primary. (b) Harmonic content of the current in the transformer primary.

Fig. 18 also shows that the ZHD converter maintains low harmonic content in the grid current, even under adverse conditions of grid voltage distortion. The current total demand distortion (TDD) was 2.29%, below the IEEE 519 limit. Therefore, the ZHD converter is an alternative that does not overload the power grid with massive harmonic injection. Moreover, due to the lack of ac bulky filter, it does not create resonance points in the grid.

C. Power Losses

Figure 19 shows the setup for measuring power losses in the ZHD converter prototype. The Yokogawa WT1800 power analyzer was used to measure losses in each component.

Figure 20 shows the connection diagram used to measure power losses in the prototype, including the diode bridges. A similar diagram was realized to measure power losses in the transformer and reactors individually.

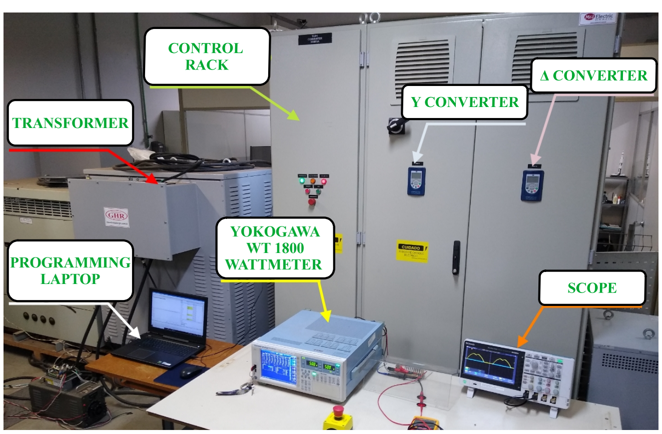

FIGURE 19. Setup for measuring power losses.

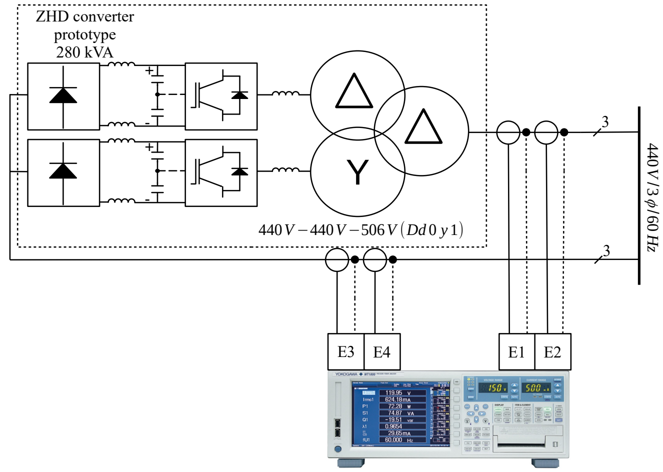

FIGURE 20. Diagram connection for measuring total power losses.

Since there is no accessible connection point to separate the power losses in the diode bridges, DC link, and 2-level converters, the input current in the diode bridges was measured, and power losses were calculated based on the diode datasheet. The power losses in the 2-level converters were calculated using the IGBT datasheet, phase current, and gate driver commands. DC link power losses were calculated as the difference between the total power loss and the losses in the other components. Table 7 presents the power losses in each element of the ZHD converter prototype. The inverter operation is expected to produce more losses than the rectifier one, since losses in the freewheeling diodes are less than in the IGBTs.

TABLE 7. Loss distribution in full-scale prototype (Load at 86.4% of nominal active power).

Conversion	Power Losses		Efficiency
Stage	[W]	[%]	[%]
Diode bridges	922	7.77	99.63
DC link[a]	2730.61	23.02	98.90
IGBTs converters	1836.00	15.48	99.25
Reactors	3070	25.89	98.74
Transformer	3301.39	27.84	98.62
TOTAL	11,860	100	95.23
ZHD converter (w/o diode bridges)	10,938	92.23	95.58
ZHD converter (w/o DC link)	**8,207**	**69.21**	**96.65**

[a] Includes the DC link inductors, capacitors and resistors.

Figure 21 presents the simulated efficiency curve based on the prototype's component parameters. The efficiency calculation does not account for losses in the DC link, as obtaining its parameters—such as the capacitor type, DC inductors, and other components—was not feasible. From the analysis of the curve, it is observed that the ZHD with the transformer consistently achieves an efficiency above

96%, except at 10% load power. Meanwhile, the complete charger maintains an efficiency close to 95% across nearly the entire load range. The most significant losses occur in the transformer and reactor, primarily due to ohmic losses.

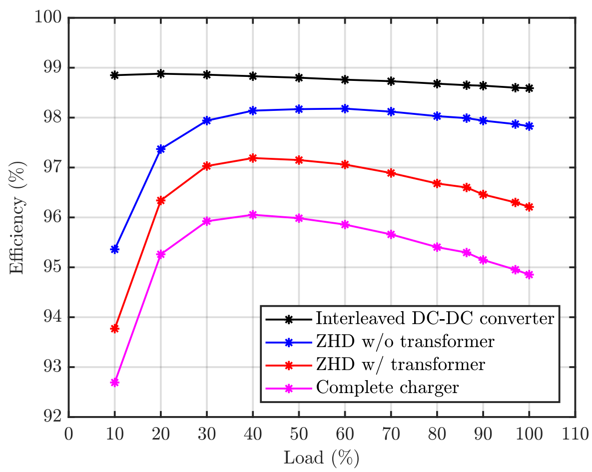

FIGURE 21. Efficiency by load.

VI. CONCLUSIONS

With the insertion of XFC in the power system, power quality is an important issue. The topologies that can be used in XFC have low power quality, lots of components, complex control, or do not comply with international standards and recommendations. In this context, the Zero Harmonic Distortion converter is a solution to meet power quality requirements according to international standards, using ordinary components and simple control.

Zero Harmonic Distortion converter showed grid current total demand distortion results of of 0.54% obtained in hardware-in-the-loop results and 2.29% in experimental results, below the limits established by IEEE 519, even in highly distorted grids.

Thus, the extreme fast charger based on the Zero Harmonic Distortion converter proved to be a viable solution to meet the various standards and recommendations. Supercapacitors are an interesting strategy, but the topology can also be used with batteries that support high-power recharges.

ACKNOWLEDGMENT

The authors would like to thank the support from Brazilian agencies CNPQ, CAPES and Minas Gerais state agency Fapemig.

AUTHOR'S CONTRIBUTIONS

D.A.L.BRANDAO: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **T.M.PARREIRAS:** Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Supervision, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **I.A.PIRES:** Conceptualization, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Supervision, Visualization, Writing – Original Draft, Writing – Review & Editing. **B.D.J.C.FILHO:** Conceptualization, Funding Acquisition, Methodology, Project Administration, Resources, Supervision, Visualization, Writing – Original Draft, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

REFERENCES

[1] F. Ortenzi, M. Pasquali, P. P. Prosini, A. Lidozzi, and M. Di Benedetto, "Design and Validation of Ultra-Fast Charging Infrastructures Based on Supercapacitors for Urban Public Transportation Applications," Energies, vol. 12, no. 12, p. 2348, Jun. 2019, doi:10.3390/en12122348.

[2] MIT Technology Review, Next Stop: Ultracapacitor Buses [Online], 2009. Available: https://www.technologyreview.com/2009/10/19/209306/next-stop-ultracapacitor-buses/, Accessed: [18 Jul 2024].

[3] Chariot Motors, 12 m ultracapacitor Chariot e-bus [Online], 2022. Available: https://chariot-electricbus.com/cmproduct/12m-ultracapacitor-chariot-e-bus/, Accessed: [24 Jul 2024].

[4] Y. Sun, E. C. W. de Jong, V. Cuk and J. F. G. Cobben, "Harmonic resonance risk of massive ultra fast charging station grid integration," 2018 18th International Conference on Harmonics and Quality of Power (ICHQP), Ljubljana, Slovenia, 2018, pp. 1-6, doi:10.1109/ICHQP.2018.8378897.

[5] A. Chudy, P. Hołyszko, and P. Mazurek, "Fast Charging of an Electric Bus Fleet and Its Impact on the Power Quality Based on On-Site Measurements," Energies, vol. 15, no. 15, p. 5555, Jul. 2022, doi:10.3390/en15155555.

[6] "IEEE Standard for Harmonic Control in Electric Power Systems," in IEEE Std 519-2022 (Revision of IEEE Std 519-2014) , vol., no., pp.1-31, 5 Aug. 2022, doi:10.1109/IEEESTD.2022.9848440.

[7] A. G. P. Alves, L. F. Crispino, M. S. Neves, C. M. Freitas, L. G. B. Rolim, and R. F. S. Dias, "Harmonic Analysis of Grid-Connected VSCs Controlled in the Stationary Frame: Disturbance Rejection, Resonant Controller Design and Limitations", Eletrônica de Potência, vol. 29, p. e202431, Sep. 2024, doi:10.18618/REP.e20431.

[8] J. M. S. Callegari, R. R. Bastos, A. F. Cupertino, D. I. Brandao, and H. A. Pereira, "Assessment of voltage detection-based Selective Harmonic Current Compensation Strategies for Different Non-linear Load Signatures", Eletrônica de Potência, vol. 29, p. e202425, Aug. 2024, doi:10.18618/REP.2005.2.053060.

[9] International Electrotechnical Commission (IEC), IEC 61000-3-6 - Assessment of emission limits for the connection of distorting installations to MV, HV and EHV power systems, 2008.

[10] S. Bai and S. M. Lukic, "Unified Active Filter and Energy Storage System for an MW Electric Vehicle Charging Station," in IEEE Trans. on Power Electron., vol. 28, no. 12, pp. 5793-5803, Dec. 2013, doi:10.1109/TPEL.2013.2245146.

[11] I. Aretxabaleta, I. M. De Alegría, J. Andreu, I. Kortabarria and E. Robles, "High-Voltage Stations for Electric Vehicle Fast-Charging: Trends, Standards, Charging Modes and Comparison of Unity Power-Factor Rectifiers," in IEEE Access, vol. 9, pp. 102177-102194, 2021, doi:10.1109/ACCESS.2021.3093696.

[12] L. Tan, B. Wu, V. Yaramasu, S. Rivera and X. Guo, "Effective Voltage Balance Control for Bipolar-DC-Bus-Fed EV Charging Station With Three-Level DC–DC Fast Charger," in IEEE Trans. Ind. Electron., vol. 63, no. 7, pp. 4031-4041, July 2016, doi:10.1109/TIE.2016.2539248.

[13] S. Rivera, B. Wu, S. Kouro, V. Yaramasu and J. Wang, "Electric Vehicle Charging Station Using a Neutral Point Clamped Converter With Bipolar DC Bus," in IEEE Trans. Ind. Electron., vol. 62, no. 4, pp. 1999-2009, April 2015, doi:10.1109/TIE.2014.2348937.

[14] G. Rajendran, C. A. Vaithilingam, N. Misron, K. Naidu and M. R. Ahmed, “Voltage Oriented Controller Based Vienna Rectifier for Electric Vehicle Charging Stations,” in IEEE Access, vol. 9, pp. 50798-50809, 2021, doi:10.1109/ACCESS.2021.3068653.

[15] S. -C. Peng, Z. -L. Li, S. C. Gulipalli, W. -C. Chen and C. -C. Chu, “Mitigating Circulating Currents of Parallel Three-Phase Vienna Rectifiers With Unbalanced Filter Inductors,” in IEEE Trans. Ind. Appl., doi:10.1109/TIA.2023.3289790.

[16] S. S. G. Acharige, M. E. Haque, M. T. Arif, N. Hosseinzadeh, K. N. Hasan and A. M. T. Oo, “Review of Electric Vehicle Charging Technologies, Standards, Architectures, and Converter Configurations,” in IEEE Access, vol. 11, pp. 41218-41255, 2023, doi:10.1109/ACCESS.2023.3267164.

[17] B. Zhang, S. Xie, Z. Li, P. Zhao and J. Xu, “An Optimized Single-Stage Isolated Swiss-Type AC/DC Converter Based on Single Full-Bridge With Midpoint-Clamper,” in IEEE Trans. on Power Electron., vol. 36, no. 10, pp. 11288-11297, Oct. 2021, doi:10.1109/TPEL.2021.3073742.

[18] H. Tu, H. Feng, S. Srdic and S. Lukic, “Extreme Fast Charging of Electric Vehicles: A Technology Overview,” in IEEE Trans. Transport. Electrific., vol. 5, no. 4, pp. 861-878, Dec. 2019, doi:10.1109/TTE.2019.2958709.

[19] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii and I. Batarseh, “A Comprehensive Review of Power Converter Topologies and Control Methods for Electric Vehicle Fast Charging Applications,” in IEEE Access, vol. 10, pp. 40753-40793, 2022, doi:10.1109/ACCESS.2022.3166935.

[20] J. C. G. Justino, T. M. Parreiras and B. J. Cardoso Filho, ”Hundreds kW Charging Stations for e-Buses Operating Under Regular Ultra-Fast Charging,” in IEEE Trans. Ind. Appl., vol. 52, no. 2, pp. 1766-1774, March-April 2016, doi:10.1109/TIA.2015.2495279.

[21] H. Akagi, ”Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC),” in IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3119-3130, Nov. 2011, doi:10.1109/TPEL.2011.2143431.

[22] M. di Benedetto, F. Ortenzi, A. Lidozzi, and L. Solero, “Design and Implementation of Reduced Grid Impact Charging Station for Public Transportation Applications,” World Electric Vehicle Journal, vol. 12, no. 1, p. 28, Feb. 2021, doi:10.3390/wevj12010028.

[23] J. Falck, C. Felgemacher, A. Rojko, M. Liserre and P. Zacharias, “Reliability of Power Electronic Systems: An Ind. Perspective,” in IEEE Industrial Electronics Magazine, vol. 12, no. 2, pp. 24-35, June 2018, doi:10.1109/MIE.2018.2825481.

[24] D. Ronanki and S. S. Williamson, “Modular Multilevel Converters for Transportation Electrification: Challenges and Opportunities,” in IEEE Trans. Transport. Electrific., vol. 4, no. 2, pp. 399-407, June 2018, doi:10.1109/TTE.2018.2792330.

[25] L. Camurca, T. Pereira, F. Hoffmann and M. Liserre, “Analysis, Limitations, and Opportunities of Modular Multilevel Converter-Based Architectures in Fast Charging Stations Infrastructures,” in IEEE Trans. on Power Electron., vol. 37, no. 9, pp. 10747-10760, Sept. 2022, doi:10.1109/TPEL.2022.3167625.

[26] M. Mao et al., “Multi-Objective Power Management for EV Fleet With MMC-Based Integration Into Smart Grid,” in IEEE Trans. on Smart Grid, vol. 10, no. 2, pp. 1428-1439, March 2019, doi:10.1109/TSG.2017.2766363.

[27] Residual Direct Current Detecting Device (RDC-DD) to be Used for Mode 3 Charging of Electric Vehicles, Std IEC 62955:2018, 2018.

[28] International Electrotechnical Commission - IEC. IEC 61851: Electrical power/energy transfer systems for electrically propelled road vehicles and industrial trucks, 2020.

[29] “IEEE Standard for Technical Specifications of a DC Quick and Bidirectional Charger for Use with Electric Vehicles,” in IEEE Std 2030.1.1-2021 (Revision of IEEE Std 2030.1.1-2015), vol., no., pp.1-147, 18 Feb. 2022, doi:10.1109/IEEESTD.2022.9714435.

[30] Parreiras, Thiago M. and Justino, Júlio C. G. and Cardoso Filho, Braz de J., The True Unity Power Factor converter — A practical filterless solution for sinusoidal currents, Paper presented at 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), p. 2557-2565, 2015, doi:10.1109/ICPE.2015.7168134.

[31] Parreiras, Thiago Morais and Justino, Júlio César Guerra and Rocha, Anderson Vagner and Filho, Braz de Jesus Cardoso, True Unit Power Factor Active Front End for High-Capacity Belt-Conveyor Systems, IEEE Trans. Ind. Appl., vol. 52, n.3, p. 2737-2746, 2016, doi:10.1109/TIA.2016.2533499.

[32] C.E. Almeida and B.J. Cardoso Filho,Shifting Resonances in Wind Farms to Higher Frequencies due to TUPF Converters, J Control Autom Electr Syst, vol. 29, p. 1-6, 2018, doi:10.1007/s40313-018-0414-7.

[33] Parreiras, Thiago M. and Alves, Marcos H. da S. and Bastos, Rodrigo R. and Pires, Igor A. and Cardoso Filho, Braz de J., The True Unity Power Factor Converter for Basic Oxygen Furnace Charging Cranes, IEEE Trans. Ind. Appl., vol. 57, n.5, p. 5507-5516, 2021, doi:10.1109/TIA.2021.3085800.

[34] D. A. d. L. Brandão, T. M. Parreiras, I. A. Pires and B. d. J. Cardoso F, “Electric Arc Furnace Reactive Compensation System using Zero Harmonic Distortion Converter,” in IEEE Trans. Ind. Appl., 2022, doi:10.1109/TIA.2022.3187392.

[35] D. A. d. L. Brandao, T. M. Parreiras, M. H. d. S. Alves, I. A. Pires and B. d. J. C. F., “Practical Implementation of the Zero Harmonic Distortion Converter in Distorted Grids,” in IEEE Trans. Ind. Appl., vol. 59, no. 6, pp. 7829-7838, Nov.-Dec. 2023, doi:10.1109/TIA.2023.3292323.

[36] G. V. Ramos, D. A. d. L. Brandao, T. M. Parreiras, S. M. Silva and B. J. C. Filho, “A Zero Harmonic Distortion Grid-Forming Converter for Medium Voltage Islanded Microgrids,” in IEEE Trans. Ind. Appl., doi:10.1109/TIA.2024.3462913.

[37] G. V. Ramos, T. M. Parreiras, and B. J. Cardoso Filho, “Control Performance Assessment of a Zero Harmonic Distortion Grid-Forming Converter for Medium Voltage Islanded Microgrids”, Eletrônica de Potência, vol. 29, p. e202441, Oct. 2024, doi:10.18618/REP.e202441.

[38] H. S. Patel and R. G. Hoft, ”Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I–Harmonic Elimination,” in IEEE Trans. Ind. Appl., vol. IA-9, no. 3, pp. 310-317, May 1973, doi:10.1109/TIA.1973.349908.

[39] H. S. Patel and R. G. Hoft, ”Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part II — Voltage Control Techniques,” in IEEE Trans. Ind. Appl., vol. IA-10, no. 5, pp. 666-673, Sept. 1974, doi:10.1109/TIA.1974.349239.

[40] Lorenz, R. D.; Lipo, T. A.; Novotny, D. W., Motion control with induction motors, Proc. of the IEEE, v. 82, n. 8, p. 1215–1240, 1994.

[41] H. Dan, S. Zhou, J. Xu, S. Wu, Y. Sun and M. Su, “Stability Analysis of the Interleaved Buck Converter With Coupled Inductor,” in IEEE Trans. Transport. Electrific., vol. 8, no. 2, pp. 2299-2310, June 2022, doi:10.1109/TTE.2022.3150920.

[42] F. Dias-Gonzáles and A. Sumper and O. Gomis-Bellmunt, Energy Storage in Power Systems, Wiley, 2016.

[43] D. Linden and T. B. Reddy, Handbook of Batteries, 3rd Edition. McGraw-Hill, New York, NY, USA, 2002.

[44] A. -S. A. Luiz and B. J. C. Filho, ”Minimum reactive power filter design for high power converters,” 2008 13th Intern. Power Electron. and Motion Control Conf., Poznan, Poland, 2008, pp. 1345-1352, doi:10.1109/EPEPEMC.2008.4635455.

[45] AVX, SCC LE Series (Online), 2020. Available: https://datasheets.avx.com/AVX-SCC-LE.pdf, Accessed: [23 Aug 2024].

[46] Texas Instruments, TMS320F28335 (Online), 2022. Available: https://www.ti.com/product/TMS320F28335. Accessed: [22 Aug 2024].

[47] Terasic, DE10-Lite Board (Online), 2022. Available: http://de10-lite.terasic.com. Accessed: [17 Aug 2024].

[48] E. F. C. Grabovski, S. A. Mussa, and M. L. Heldwein, “Large-Signal Models of the Park Transformation and Phase-Locked Loop Algorithms”, Eletrônica de Potência, vol. 29, p. e202417, Jul. 2024, doi:10.18618/REP.2005.1.045052.

[49] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos and D. Boroyevich, “Decoupled Double Synchronous Reference Frame PLL for Power Converters Control,” in IEEE Trans. Power Electron., vol. 22, no. 2, pp. 584-592, March 2007, doi:10.1109/TPEL.2006.890000.

BIOGRAPHIES

Dener A. de L. Brandao was born in Brazil in 1994. He received the Master’s degree in Electrical Engineering in 2021 from the Universidade Federal de Minas Gerais, Belo Horizonte, Brazil, where he is currently a doctoral student. His current research interests include industry applications, transportation electrification and microgrid control.

Thiago M. Parreiras received the Doctorate degree in Electrical Engineering in 2020 from the Universidade Federal de Minas Gerais, Belo Horizonte, Brazil, where he has been with TESLA Power Engineering Laboratory since 2013. Since 2023, he has been a Faculty Member with the Departament of Electrical Engineering, Centro Federal de Educação Tecnológica de Minas Gerais, Belo Horizonte, Brazil, where he is currently an assistant professor. His current research interests include high-power converters and drives, power quality, renewable energy and transportation electrification.

Igor A. Pires was born in Brazil in 1980. He received the Doctorate in electrical engineering from Universidade Federal de Minas Gerais (UFMG), Belo Horizonte, Brazil, in 2011. Since 2011, he is an assistant professor in Electronics Engineering Department of UFMG. His research interests include metal industry applications, power electronics, power quality, and vehicle electrification.

Braz de J. Cardoso F. received the Ph.D. degree in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, in 1998. Since 1989, he has been a Faculty Member with the Department of Electrical Engineering, Universidade Federal de Minas Gerais, Belo Horizonte, Brazil, where he is currently a Full Professor, and the Founder and the Head of the TESLA Power Engineering Laboratory. He has authored/coauthored about 200 technical papers on the topics of power electronics and electrical drives and holds eight patents. His research interests include utility applications of power electronics, renewable energy sources, semiconductor power devices, electrical machines and drives, and vehicle electrification.