Eletrônica de Potência
Open Journal of Power Electronics

Received November 30, 2024; accepted April 13, 2025; Date of publication May 08, 2025.
The review of this paper was arranged by Associate Editor Francisco D. Freijedo and Editor-in-Chief Heverton A. Pereira.
Digital Object Identifier http://doi.org/10.18618/REP.e202535

Analysis and Implementation of a Single-Phase Bridgeless Hybrid Switched-Capacitor Rectifier in Discontinuous Conduction Mode for Power Factor Correction

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ABSTRACT This work presents the quantitative and qualitative analysis, as well as the experimental results of a practical implementation of the Single-Phase Bridgeless Hybrid Switched Capacitor Rectifier operating in discontinuous conduction mode (DCM) to achieve a high input power factor. Operating in DCM provides several advantages, including natural power factor correction (PFC) behavior of the input current and reduced semiconductor switching losses. The paper begins with a literature review on key studies of hybrid switched-capacitor converters with a high power factor. Subsequently, the converter analysis, including its modulation scheme, operational stages and design methodology, is detailed. The proposed approach is validated with results from a practical prototype implementation, achieving an output voltage of 1200 V and an output power of 315 W from an input voltage of 220 V. The converter demonstrated an efficiency of 97.3%, a power factor of 0.99, and harmonic distortion levels within the limits specified by IEC61000-3-2.

KEYWORDS Bridgeless Rectifier, Discontinuous Conduction Mode, Duty Cycle Control, Hybrid Switched-Capacitor Converters, Power Electronics, Power Factor Correction, Static Gain Multiplication, Voltage Balancing, Voltage Stress Reduction.

I. INTRODUCTION

In recent years, the demand for enhanced power quality in energy conversion systems has driven research into innovative topologies that incorporate switched-capacitor concepts.

The work presented by [1] proposes two topologies derived from the Cúk converter, which incorporate switched-capacitor networks: one with a bridge configuration for alternating voltage rectification and another bridgeless topology. Both topologies reduce the static gain of the conventional Cúk converter by half, making these structures more suitable for step-down applications. Operating in discontinuous conduction mode, the waveform of the input current naturally follows the shape of the input voltage. Although these topologies employ a greater number of components compared to the conventional solution, they demonstrate improvements in efficiency and power factor.

An integration of the buck-boost converter with switched capacitors is suggested by [2] for controlling the speed of a BLDC motor with a high power factor. Similar to the previously mentioned converter, the buck-boost operates in DCM, requiring only a voltage control loop to regulate the bus voltage applied to a voltage inverter. The power factor correction converter is designed for an output power of 300 W, switching at a frequency of 30 kHz, and regulating the output voltage between 50 V and 200 V, with an input voltage of 220 V and a frequency of 50 Hz. The total harmonic distortion observed was below 4.81%, which is within the limits set by the IEC 61000-3-2 standard.

A recent study published in the specialized literature by [3] proposed an integration of a boost converter with a switched capacitor cell, effectively halving the static gain of the conventional converter. This configuration enables the converter to operate both as a step-down and a step-up converter. The proposed converter is primarily designed for low output voltage applications, aiming to provide a more compact and feasible alternative to converters that utilize cascaded configurations of boost and buck converters. This design seeks to achieve low gain with a high power factor while avoiding issues with the dead zone of the input current, which are commonly encountered in conventional buck PFC converters. The proposed topology was experimentally validated using a 1 kW prototype under two distinct operational

conditions: (A) 127V AC and 100V DC; and (B) 220V AC and 200V DC for the input and output voltages, respectively. The experimental results demonstrate that the power factor is approximately unity, while the total harmonic distortion of the input current is measured at 4.6%. The maximum efficiency achieved was 96.5% under condition B.

A variation of this converter is proposed by [4] as a less bulky alternative to two-stage conversion. This design employs a boost inductor on the AC side and requires the use of a bidirectional switch. The viability of the proposed converter for 1 kW operation was confirmed through an experimental prototype utilizing SiC semiconductor technology for the bidirectional switch. The converter has an input voltage range of 90 to 270 V and is capable of generating a regulated DC voltage from 72 to 400 V while meeting the stringent total harmonic distortion (THD) limits for input current established by IEC 61000-3-2. At nominal power, the efficiency is 97.35%, with a THD of 2.78% and a power factor of 0.99. The continuation of this study is presented by [5], who propose a bridgeless totem-pole structure. This converter is capable of functioning as a component of an onboard charging (OBC) system, specifically for low-voltage battery charging, and is suitable for power levels of up to 3.3 kW. A 1 kW prototype of the converter design was simulated and developed. The results indicate that the converter can operate within a wide input voltage range of 90-270 V, with the prototype achieving a THD of 2.19% and a power factor (PF) of 0.99.

A boost rectifier with a switched capacitor network was proposed by [6]. This converter features only one controlled switch, a minimal number of passive components, high gain without a transformer, and reduced voltage stress on the switch compared to the output voltage. Simulation results for a converter with an output of 1600 V, 2.5 kW, and a switching frequency of 25 kHz demonstrated a PF of 0.99 and a THD of 2.73%.

Significant results were also achieved in the work by [7], which proposed a family of six unidirectional, three-level converters with pulse width modulation based on a hybrid switched capacitor. The objective was to achieve high gain, reduced voltage stress, and high power factor while utilizing a minimal number of controlled switches. The proposal was validated through the implementation of a prototype of one of the topologies, which featured an output voltage of 1600 V, an output power of 2.5 kW, and a switching frequency of 90 kHz. The prototype demonstrated a high power factor and low THD, achieving an efficiency of 97.91%, with the semiconductors operating at only one-quarter of the output voltage.

In [8], a rectifier derived from the SEPIC converter with a switched capacitor network was proposed. This converter exhibits a significantly higher static gain compared to conventional designs. Simulations of the SEPIC switched capacitor rectifier for an output voltage of 1600 V resulted in a PF that is nearly unity, and the THD remained within the limits set by the IEC 61000-3-2 standard. The article suggests that this topology is suitable for applications requiring high DC voltages and low current levels, such as in X-ray systems.

In [9], a series of AC-DC converters based on the SEPIC voltage doubler rectifier aiming a high power factor are presented. This structure utilizes a three-stage switch that can be implemented with a combination of controlled switches and diodes. Operating in discontinuous conduction mode, the converter exhibits intrinsic power factor correction. It can achieve a high power factor, reduced THD, elevated gain, and low voltage stress on the switches. To validate the design, a prototype was developed with an output voltage of 800 V and an output power of 1 kW, operating at a switching frequency of 50 kHz. The results demonstrated a power factor of 0.99, a THD of 1.96%, and an efficiency of 93.9%.

In [10], a single-phase bridgeless PFC rectifier with hybrid switched-capacitor cell operating in continuous conduction mode (CCM) was introduced. The proposed converter utilize switched-capacitor voltage multipliers to enhance the voltage gain of conventional boost rectifiers while simultaneously reducing the voltage stress on the switches. The integration of the boost switching cell with the ladder cell leads to a reduction in the number of semiconductor devices compared to traditional hybrid boost rectifiers. The theoretical analysis was experimentally validated using a 1 kW prototype, which operates with a 220 V input and delivers an 800 V DC output. The converter achieved a maximum efficiency of approximately 97.9% and an input PF exceeding 0.99. Although an extensive analysis has been presented for CCM, no information is given related to DCM operation. To fill this gap, the paper [11] presented the qualitative and quantitative analyses of this converter operating in discontinuous conduction mode. The advantages of the DCM operation include the requirement of only one output voltage control loop for load regulation, eliminating the need for a current control loop to achieve a high input power factor, and reducing semiconductor switching losses.

This paper builds upon the previous research by incorporating a comprehensive literature review of hybrid switched-capacitor static converters designed for high power factor, as outlined in this introduction. Furthermore, it presents experimental results from the implementation of a physical prototype, which serves to validate the proposed methodology that was previously supported only by simulation outcomes.

II. SINGLE-PHASE HYBRID BOOST PFC RECTIFIER

The structure proposed by [10] is composed of two controllable switches (S_1 and S_2), a boost inductor (L), a boost diode (D_b), two low-frequency output capacitors (C_{o1} and C_{o2}), and a switched capacitor cell consisting of a switched capacitor (C_s) and two diodes (D_{c1} and D_{c2}), as presented in Fig. 1. The addition of switched capacitor cells and output capacitors can enhance the static gain of the converter while preserving the number of controlled switches, without

increasing the voltage stress on all components. In this work, the analysis is presented considering a single switched capacitor cell employed in the converter. One advantage of this converter is that the ground reference of the active switches is connected to each other and to the output voltage, simplifying the switch gate driver circuits.

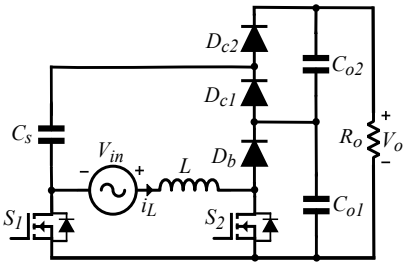

FIGURE 1. Converter Topology.

A. Modulation Scheme

To mitigate conduction losses, the chosen modulation technique requires one of the switches to remain continuously conducting for the entire half-period of the input voltage. For this purpose, the input voltage must be measured using a differential amplifier and compared with the zero level. Additionally, logic circuits, such as OR gates, are employed to keep the control signal of the switch active throughout half of the input voltage cycle. This approach effectively minimizes conduction losses by avoiding current flow through the device body diodes. A graphical representation of the PWM signal generator circuit and the modulation scheme are visually depicted in Fig. 2.

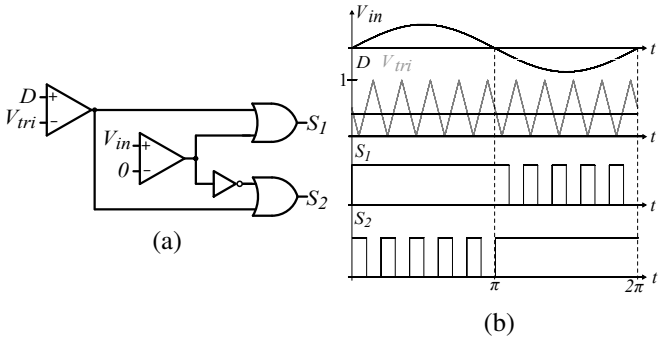

FIGURE 2. (a) PWM signal generator circuit. (b) Modulation scheme.

B. Operational Stages

The DCM operation of the converter consists of six operational stages, three for each half of the grid cycle, as shown in Fig. 3. The converter exhibits an asymmetric operation, considering that the switched capacitor C_s only transfers energy during the negative half-cycle. It is also only during this half-cycle that the output capacitor C_{o2} is charged. This is why the output capacitors must be designed considering the grid frequency, presenting a drawback when compared to conventional boost PFC rectifiers, where the output capacitors are dimensioned to operate at twice the grid frequency.

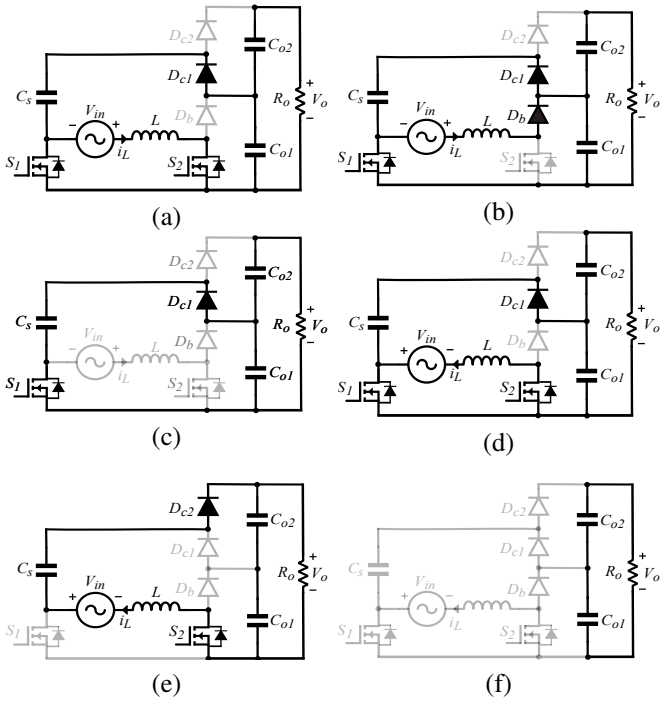

FIGURE 3. Converter operational stages. (a) Positive cycle - First stage. (b) Positive cycle - Second stage. (c) Positive cycle - Third stage. (d) Negative cycle - First stage. (e) Negative cycle - Second stage. (f) Negative cycle - Third stage.

Throughout the entire positive half cycle, the switch S_1 remains turned on, the diode D_{c1} is forward-biased, connecting C_s and C_{o1} in parallel, and the output capacitors C_{o1} and C_{o2} supply energy to the load. In the first operational stage [see Fig. 3 (a)], the switch S_2 is turned on, connecting the input power supply V_{in} to the inductor L which stores energy. In the second stage [see Fig. 3 (b)], the switch S_2 is turned off, and the energy stored in the inductor is transferred to the output capacitor C_{o1} and to the switching capacitor C_s through the diode D_b, until the current reaches zero. Since C_s does not transfer energy during this half-cycle, the current in D_{c1} can be neglected in the quantitative analysis of the converter, as demonstrated by the theoretical waveforms presented in Figure 4 (a). The time represented by D_2T_s corresponds to the moment that the inductor current reaches zero. The third stage [see Fig. 3 (c)] only involves the transfer of energy from capacitors C_{o1} and C_{o2} to the load.

During the negative half cycle, switch S_2 remains turned on. In the first stage [see Fig. 3 (d)], the switch S_1 is turned on, connecting the power input V_{in} to the inductor L. The capacitor C_{o1} charges the switching capacitor C_s through the diode D_{c1}. Considering that there is a voltage difference between the output capacitor C_{o1} and the switched capacitor C_s, special attention must be given to this energy transfer. This is because the charging current is limited only by the intrinsic resistances of the components in the current

flow path, including the forward resistance of diode D_{c1}, the drain-source resistance of switch S_1, and the series-equivalent resistances of the capacitors. The load energy is provided by the output capacitors C_{o1} and C_{o2}.

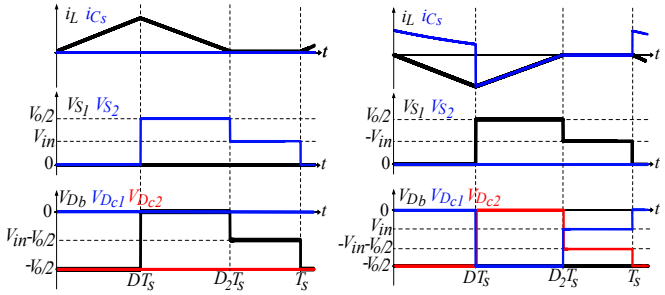

FIGURE 4. Main theoretical waveforms. (a) Positive half cycle. (b) Negative half cycle.

The second stage [see Fig. 3 (e)] initiates when S_1 is switched OFF. Energy is transferred from the inductor L and the switched capacitor C_s to the output capacitors C_{o1} and C_{o2}, as well as to the output load, until the inductor current reaches zero. In the third stage, the output current is maintained by the output capacitors C_{o1} and C_{o2} [see Fig. 3 (f)]. The main theoretical waveforms associated with the negative half cycle are depicted in Figure 4 (b).

III. DESIGN METHODOLOGY

For the converter analysis, the input voltage frequency is considered significantly lower than the switching frequency. Therefore, approximating the input voltage as a continuous signal within a switching period is valid, as presented in the converter's operational stages. For each switching period, the voltage and current amplitudes vary according to the magnitude of the input voltage. The input voltage is defined by:

$$V_{in}(t) = V_p \sin(\omega t) \tag{1}$$

The conduction time of the switch that commutates during the half-cycle is constant for each switching period and is defined by:

$$\Delta t_1 = DT_s \tag{2}$$

Thus, the peak current in the inductor can be determined by:

$$i_p(t) = \frac{V_p \sin(\omega t)}{L} \Delta t_1 \tag{3}$$

Since, during the second operational stage, the current decreases to zero, the current variation in the inductor will be the same as in the first stage, as described by:

$$\Delta i_L(\Delta t_1) = \Delta i_L(\Delta t_2) \tag{4}$$

$$\frac{V_p \sin(\omega t)}{L} \Delta t_1 = \frac{\frac{V_o}{2} - V_p \sin(\omega t)}{L} \Delta t_2 \tag{5}$$

By isolating Δt_2 in Equation 5, the duration of the second operational stage is obtained:

$$\Delta t_2 = D_2 T_s - DT_s = \frac{V_p \sin(\omega t)}{\frac{V_o}{2} - V_p \sin(\omega t)} \Delta t_1 \tag{6}$$

Defining α:

$$\alpha = \frac{V_p}{V_o} \tag{7}$$

And rewriting Δt_2 as a function of α, we obtain:

$$\Delta t_2 = \frac{\alpha \sin(\omega t)}{\frac{1}{2} - \alpha \sin(\omega t)} \Delta t_1 \tag{8}$$

A. Maximum Duty Cycle for DCM

To ensure the converter operates in DCM throughout the entire grid period, the maximum duty cycle must be calculated. Considering the worst-case scenario, at the limit of discontinuity where the conduction is critical, it follows that:

$$\Delta t_{2_{crit}} = (1 - D_{max}) T_s \tag{9}$$

At the peak of the input voltage, the current in the inductor reaches its highest value, and consequently, the longest demagnetization time occurs, as described by:

$$\Delta t_{2_{max}} = \frac{\alpha}{\frac{1}{2} - \alpha} D_{max} T_s \tag{10}$$

Equating (9) and (10) and isolating the duty cycle ratio, D, yields the function that calculates the maximum duty cycle, as presented:

$$D_{max} = 1 - 2\alpha \tag{11}$$

B. Output Characteristic

Similar to the conventional boost converter, the average output current, I_{avo}, for a switching period is obtained by:

$$I_{avo} = \frac{1}{T_s} \frac{i_p \Delta t_2}{2} = \frac{V_p D^2}{f_s L} \frac{\alpha \sin^2(\omega t)}{1 - 2\alpha \sin(\omega t)} \tag{12}$$

The average output current for half of the grid period is calculated by:

$$I_o = \frac{1}{\pi} \int_0^{\pi} I_{avo}\, d\omega t = \frac{V_p D^2}{2\pi f_s L} \int_0^{\pi} \frac{\alpha \sin^2(\omega t)}{\frac{1}{2} - \alpha \sin(\omega t)}\, d\omega t \tag{13}$$

Defining $Y_1(\alpha)$:

$$Y_1(\alpha) = \int_0^{\pi} \frac{\alpha \sin^2(\omega t)}{\frac{1}{2} - \alpha \sin(\omega t)}\, d\omega t \tag{14}$$

Rewriting I_o as a function of $Y_1(\alpha)$:

$$I_o = \frac{V_p D^2}{2\pi f_s L} Y_1(\alpha) \tag{15}$$

C. Maximum Inductance for DCM

To ensure operation in DCM throughout the entire grid period, the maximum inductance must also be calculated. The output current will be maximum when the duty cycle is at its maximum; therefore:

$$I_{o_{max}} = \frac{V_p(1-2\alpha)^2}{2\pi f_s L} Y_1(\alpha) \tag{16}$$

The maximum output power is defined by:

$$P_{o_{max}} = V_o I_{o_{max}} \tag{17}$$

The maximum output current can be written as follows:

$$I_{o_{max}} = \frac{P_{o_{max}}}{V_o} \tag{18}$$

Substituting (18) into (16) and isolating L, the inductance for critical conduction mode operation is obtained, which defines the maximum inductance value for operation in DCM.

$$L_{max} = \frac{V_p^2}{2\pi f_s P_{o_{max}}} \frac{Y_1(\alpha)(1-2\alpha)^2}{\alpha} \tag{19}$$

D. Switched Capacitor

The dimensioning of the switched capacitor is based on the operational stages of the negative half cycle. The criterion is to ensure that the charge of capacitor C_s in the first operational stage occurs in a partial charge (PC) mode [12], as described in [7]. This mode creates a near constant current shape, similar to the no charge (NC) mode, without the need for oversizing the capacitor. Furthermore, by adopting the PC mode, the peak current is reduced compared to a "complete charge" mode, thereby minimizing additional conduction losses.

The energy transfer between capacitors during the first operational stage in the negative half-cycle can be represented by the equivalent circuit shown in Figure 5.

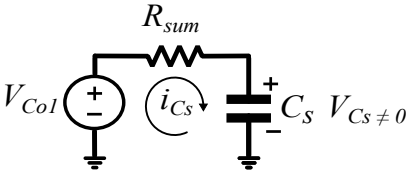

FIGURE 5. Switching Capacitor Charge - Equivalent Circuit

Here, R_{sum} represents the summation of the intrinsic resistances of the components in the path of the capacitor charging current, S_1, D_{c1}, C_s and C_{o1}.

By superposition, adding the effect of the power supply with the effect of the initial charge of the switched capacitor, the voltage across the capacitor C_s is obtained:

$$V_{Cs}^{n1}(t) = V_{C_{o1}} \cdot (1 - e^{-\frac{t}{R_{sum} \cdot C_s}}) + V_{C_s}(T_s) \cdot e^{-\frac{t}{Rsum \cdot C_s}} \tag{20}$$

The current evolution in the capacitor C_s during the first stage of the negative half cycle can be determined using:

$$i_{Cs}^{n1}(t) = \frac{(V_{C_{o1}} - V_{C_s}(T_s)) \cdot e^{-\frac{t}{(R_{sum}) \cdot C_s}}}{R_{sum}} \tag{21}$$

The final voltage value $V_{C_s}(T_s)$ is equal to the switching capacitor voltage in $D_2 T_s$, because C_s does not transfer energy in the third operational stage, and is calculated by:

$$V_{Cs}(T_s) = \frac{(V_{in} + V_{Co1})\Delta t_2^2 + 2V_{in} D T_s \Delta t_2}{2LC_s \left(1 - e^{\frac{-DT_s}{C_s R_{sum}}}\right)} + V_{Co1} \tag{22}$$

In the second operational stage the switching capacitor current is forced by the inductor discharge [see Fig. 3 (e)], as described by:

$$i_{Cs}^{n2}(t) = i_L(t) = \frac{(2V_{in} + V_o) \cdot t}{2L} + \frac{V_{in} D T_s}{L} \tag{23}$$

Following the design methodology given in [10], in order to select the switching capacitor, the calculation of the instantaneous RMS switching capacitor current is performed for various capacitance values at the peak negative input voltage. The discontinuous period of the boost inductor current, during which the switching capacitor current is zero, was excluded from the calculation. The RMS current in C_s is given by:

$$\begin{aligned} i_{Cs_{RMS}} = \Bigg(& \frac{(V_{Co1} - V_{Cs}(T_s))^2 C_s (1 - e^{\frac{2DT_s}{C_s R_{sum}}})}{2R_{sum} T_s} \\ & + \frac{(2V_{in} + V_o)^2}{6LT_s} \Delta t_2^3 + \frac{V_{in} D (2V_{in} + V_o)}{2L^2} \Delta t_2^2 \\ & + \frac{V_{in}^2 D^2 T_s^2}{L^2 T_s} \Delta t_2 \Bigg)^{\frac{1}{2}} \end{aligned} \tag{24}$$

The relationship between the capacitances and the calculated RMS currents of the switching capacitor for three different switching frequency f_s values (50 kHz, 100 kHz and 200 kHz) is presented in Fig. 6.

Observing Fig. 6, it can be concluded that the RMS value of the capacitor current decreases exponentially with the increase in capacitance value. However, beyond certain capacitance values, the RMS current reaches a nearly constant value, where further increases in capacitance no longer provide a significant reduction in the RMS current. Therefore, choosing larger capacitors does not provide significant benefits in terms of converter losses but increases the cost and volume of the solution. Analyzing the effect of switching frequency on the RMS current of the switched capacitor, an increase in switching frequency significantly reduces the RMS value for lower capacitances, where the charging of the switched capacitor occurs in complete-charge mode. However, since the goal is to charge the switched capacitor in a partial charge mode, it is important to note that the switching

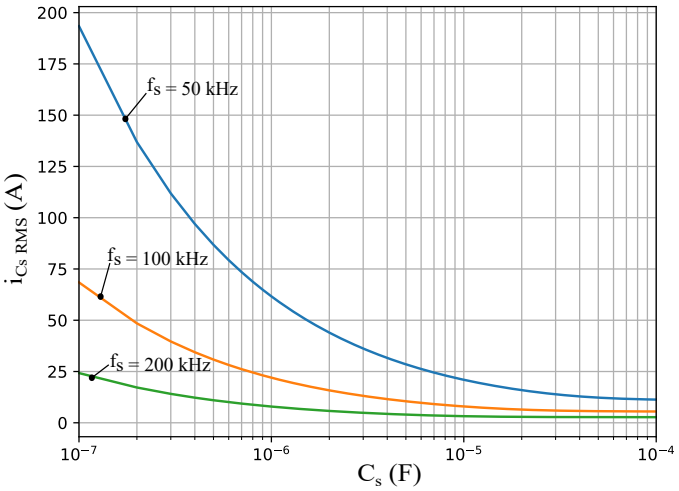

FIGURE 6. RMS Current - Switching Capacitor

frequency determines the minimum achievable RMS current. However, an excessive increase in frequency results in higher switching losses, which requires the designer to find the optimal point that meets the converter specifications.

E. Output Capacitors

The output capacitors are designed to reduce the low-frequency voltage ripple, based on the determination of an equivalent capacitance, C_o', which corresponds to the series connection of the two output capacitors. Considering that the converter behaves similarly to a single-phase half-wave rectifier, and since capacitor C_{o2} charging occurs only during one half cycle, these capacitors are dimensioned for filtering at the frequency of the input voltage.

The equivalent capacitance C_o' can be determined by:

$$C_o' = \frac{P_o}{\pi \cdot f \cdot V_o \cdot \Delta V_o} \tag{25}$$

Here, ΔV_o represents the desired ripple in the output voltage.

Individual capacitance values can be obtained by multiplying the equivalent capacitance by the number of capacitors, as seen in:

$$C_{o1} = C_{o2} = \frac{2 \cdot P_o}{\pi \cdot f \cdot V_o \cdot \Delta V_o} \tag{26}$$

F. Input LC Filter

The converter operates at a high switching frequency, and the input current becomes distorted due to this switching. Therefore, an LC input filter is inserted at the converter's input to make the input current waveform less distorted, minimizing the high-frequency harmonics flowing through the grid.

The criteria for the filter design are:

- The cutoff frequency, f_{cutoff} should be one decade below the switching frequency for significant harmonic attenuation and approximately 20 times higher than the grid frequency to avoid introducing phase shifts between voltage and input current.
- The damping coefficient, ζ, should be between 0.7 and 1 to prevent oscillations around the cutoff frequency and to avoid introducing phase shifts between voltage and input current.

To obtain the values of the input filter capacitor and inductor, the equivalent resistance of the converter as seen from the input filter perspective must be calculated using:

$$R_{eq} = \frac{L \cdot f_s}{D} \tag{27}$$

Once the equivalent resistance is known, the filter capacitor is calculated as follows:

$$C_f = \frac{1}{2 \cdot \zeta \cdot (2 \cdot \pi \cdot f_{cutoff}) \cdot R_{eq}} \tag{28}$$

Using the capacitor value obtained, the filter inductor can be determined by:

$$L_f = \frac{1}{(2 \cdot \pi \cdot f_{cutoff})^2 \cdot C_f} \tag{29}$$

IV. VOLTAGE AND CURRENT STRESSES OF SWITCHES AND DIODES

The following equations present the methodology for current stress determination for the semiconductors, along with the considerations for obtaining the maximum voltage stresses.

A. Current Stress - Switches

For the determination of the current stresses on the switches, the instantaneous RMS currents (during the switching period) are initially calculated for both the positive and negative half-cycles.

In the positive half-cycle, the current through the switch S_1 is equal to the current in the boost inductor.

The instantaneous RMS current of switch S_1 during the positive half-cycle is given by:

$$i_{S_1-effp}(\omega t) = \left[\frac{(2V_p \sin(\omega t) - V_o)V_p \sin(\omega t) D \Delta t_2^2}{2L^2} + \frac{V_p^2 \sin(\omega t)^2 D^3}{3L^2 f_s^2} + \frac{(2V_p \sin(\omega t) - V_o)^2 \Delta t_2^3}{12 L^2 T_s} + \frac{V_p^2 \sin(\omega t)^2 D^2}{L^2} \frac{\Delta t_2}{T_s}\right]^{\frac{1}{2}} \tag{30}$$

In the first operational stage of the negative half-cycle, S_1 conducts the magnetization current of the boost inductor and the charging current of the switched capacitor.

The instantaneous RMS current in the negative half-cycle can be described by:

$$i_{S_1-effn}(\omega t) = \left\{ \frac{1}{T_s} \left[-\left(\frac{\frac{V_o}{2} - V_{C_s}(T_s)}{R_{eq}} \right)^2 \frac{R_{eq}C_s \left(e^{\frac{-DT_s}{C_s R_{eq}}} - 1 \right)}{2} + 2\frac{V_{C_s}(T_s) - \frac{V_o}{2}}{R_{eq}} \frac{-V_p \sin(\omega t)}{L} \left(-C_s R_{eq} DT_s e^{\frac{DT_s}{C_s R_{eq}}} - C_s^2 R_{eq}^2 DT_s e^{\frac{DT_s}{C_s R_{eq}}} + C_s^2 R_{eq}^2 \right) + \frac{-V_p^2 \sin^2(\omega t)}{L^2} \frac{D^3 T_s^3}{3} \right] \right\}^{\frac{1}{2}} \quad (31)$$

During the positive half-cycle, switch S_2 conducts the magnetization current of the inductor L. The instantaneous RMS current in switch S_2 in the positive half-cycle is determined by:

$$i_{S_{2-effp}}(\omega t) = \frac{V_p \sin(\omega t)}{L f_s} \sqrt{\frac{D^3}{3}} \quad (32)$$

During the negative half-cycle, the current through the switch S_2 is equal to the inductor current. The instantaneous RMS current in the switch S_2 in the negative half-cycle:

$$i_{S_2-effn}(\omega t) = \left[\frac{(2V_p \sin(\omega t) + V_o) V_p \sin(\omega t) D\Delta t_2^2}{2L^2} + \frac{V_p^2 \sin(\omega t)^2 D^3}{3L^2 f_s^2} + \frac{(2V_p \sin(\omega t) + V_o)^2 \Delta t_2^3}{12L^2 T_s} + \frac{V_p^2 \sin(\omega t)^2 D^2}{L^2} \frac{\Delta t_2}{T_s} \right]^{\frac{1}{2}} \quad (33)$$

The RMS current in the switches over the complete grid period is calculated by:

$$i_{S_{1,2-RMS}} = \sqrt{\frac{1}{2\pi} \left(\int_0^{\pi} i_{S_{1,2-effp}}^2(\omega t)\, d\omega t + \int_{\pi}^{2\pi} i_{S_{1,2-effn}}^2(\omega t)\, d\omega t \right)} \quad (34)$$

Given the complexity involved in solving the equation above, it is recommended to employ computational methods for the resolution.

B. Voltage Stress - Switches

The maximum voltage stress on switch S_1 occurs during the second operational stage in the negative half-cycle. In this stage, the voltage across the switch is given by the sum of the output capacitors C_{o1} and C_{o2} voltages, subtracting the voltage across the switched capacitor C_s. Since the voltage across the capacitors are ideally equal and equivalent to half of the output voltage, it follows that:

$$V_{S_{1-max}} = V_{C_{o1}} + V_{C_{o2}} - V_{C_s} = \frac{V_o}{2} \quad (35)$$

The maximum voltage stress on the switch S_2 occurs during the second operational stage in the positive half-cycle. In this stage, diode D_b is forward biased, connecting capacitor C_{o1} in parallel with switch S_2. Therefore, the maximum voltage on the switch S_2 is given by:

$$V_{S_{2-max}} = V_{C_{o1}} = \frac{V_o}{2} \quad (36)$$

C. Current Stress - Diodes

For the sizing and loss estimation of the diodes, the equations for determining the average current in the diodes will be presented based on the described operational stages.

During the positive half-cycle, in the second operational stage, diode D_b conducts the demagnetization current of inductor L. This is the only operational stage which D_b is forward biased. The equation for obtaining the average current is given by:

$$i_{D_{b-AVG}} = \frac{1}{2\pi} \int_0^{\pi} \frac{1}{T_s} \left(\frac{V_p \sin(\omega t) D\Delta t_2 T_s}{L} + \frac{2V_p \sin(\omega t) - V_o}{4L} \Delta t_2^2 \right) d\omega t \quad (37)$$

During the positive half-cycle, diode D_{c1} is forward biased, connecting C_s and C_{o1} in parallel. However, the voltage difference between the capacitors is so small that the circulating current through diode D_{c1} is neglected in the component stress analysis. During the negative half-cycle, diode D_{c1} conducts the charging current of the switched capacitor. The average current of diode D_{c1} in the grid period is determined by:

$$i_{D_{c1-AVG}} = \frac{1}{2\pi} \int_{\pi}^{2\pi} \frac{V_{C_s}(T_s) - \frac{V_o}{2}}{T_s} C_s \frac{-(e^{\frac{-DT_s}{C_s R_{eq}}} - 1)}{1}\, d\omega t \quad (38)$$

During the positive half-cycle, no current flows through diode D_{c2}. During the negative half-cycle, diode D_{c2} conducts the demagnetization current of the boost inductor, which also corresponds to the discharge current of the switched capacitor. The average current in diode D_{c2} is calculated by:

$$i_{D_{c2-AVG}} = \frac{1}{2\pi} \int_{\pi}^{2\pi} \frac{1}{T_s} \left(-\frac{V_p \sin(\omega t) DT_s \Delta t_2}{L} - \frac{2V_p \sin(\omega t) + V_o}{4L} \Delta t_2^2 \right) d\omega t \quad (39)$$

D. Voltage Stress - Diodes

The maximum blocking voltage on diode D_b occurs during the first operational stage in the positive half-cycle, when diode D_b is connected in parallel with the output capacitor C_{o1}. Therefore, the maximum voltage stress on diode D_b is given by:

$$V_{D_{b-max}} = V_{C_{o1}} = \frac{V_o}{2} \tag{40}$$

On the diode D_{c1}, the maximum blocking voltage occurs in the second operational stage of the negative half-cycle, when it is connected parallel with output capacitor C_{o2}. The maximum voltage stress on diode D_{c2} is determined by:

$$V_{D_{c1-max}} = V_{C_{o2}} = \frac{V_o}{2} \tag{41}$$

The maximum blocking voltage on diode D_{c2} occurs in the first operational stage of the positive cycle. In this stage, D_{c2} is connected parallel with C_{o2} and the maximum voltage stress is obtained by:

$$V_{D_{c1-max}} = V_{C_{o1}} = \frac{V_o}{2} \tag{42}$$

V. EXPERIMENTAL RESULTS

To validate the proposed design methodology, a prototype was developed. The main specifications are outlined in Table 1. The specifications were defined based on the work presented in [13], with the aim of obtaining an input boost converter for cascading with an inverter structure. The target application for this converter is in electroporation, where the introduction of chemicals into a cell can be improved by using high-voltage and short-duration electrical pulses to enhance the cellular transport permeability.

TABLE 1. Converter Specifications.

Component	Symbol	Specification
Switching Frequency	f_s	$100kHz$
Output Voltage	V_o	$1200V$
Output Power	P_o	$315W$
Input Voltage	V_{in}	$220V$
Input Frequency	f	$60Hz$
Duty Cycle	D	0.32
Boost Inductor	L	$290\mu H$
Resistance Association	R_{sum}	1.5Ω
Output Capacitors	$C_{o1,2}$	$165\mu F$ (2 x $330\mu F$) B43509
Switching Capacitor	C_s	$20\mu F$ C4AQQBW5200A3LJ
Diodes	$D_{c1,2,3}$	1200V@40A IDW40G120C5B
MOSFETs	$S_{1,2}$	1000V@8A FQA8N100C
Filter Capacitor	C_f	$1\mu F$ B32922
Filter Inductor	L_f	$2.53mH$

The physical prototype, with dimensions of 162.68 mm × 124.58 mm × 51.6 mm (L × W × H), is shown in Figure 7. The achieved power density was 306 kW/m³, demonstrating the compactness of the proposed design.

The converter was tested at its rated power, successfully delivering an output voltage of 1200 V from a input of 220 V. The input current exhibited a sinusoidal waveform with the expected distortion of the boost DCM PFC converters, remaining in phase with the input voltage and achieving a power factor of 0.99. Figure 8 illustrates the voltage and current waveforms in both the input and output when operating at rated power. The efficiency achieved under these conditions was 97.3%.

FIGURE 7. Physical Prototype

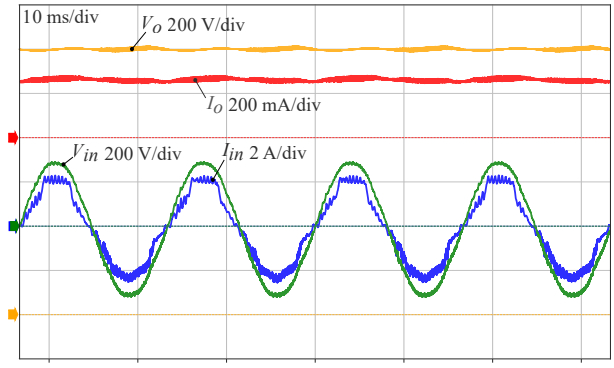

FIGURE 8. Rated power operation

The results presented in this article were obtained with the converter operating with a constant duty cycle to validate its steady-state operation. The control signals were generated using the SG3525 integrated circuit in conjunction with operational amplifiers to maintain one of the switches activated throughout the entire half-cycle. Under these operating conditions, the converter achieved a THD of the input current of 12.70%. A methodology for reducing the current harmonic distortion for this converter was proposed and validated through simulation in [11], and it can be easily implemented when using active control with signal generation from a microprocessor.

To confirm the effectiveness of power factor correction in the DCM operation of the converter, an FFT analysis was performed on the input current of the converter, as illustrated in Figure 9. The analysis revealed that the harmonic levels were well below the thresholds established by the relevant standard, ensuring compliance for integration into Class A electronic equipment. These results underscore

the converter's suitability for modern applications requiring stringent harmonic performance criteria.

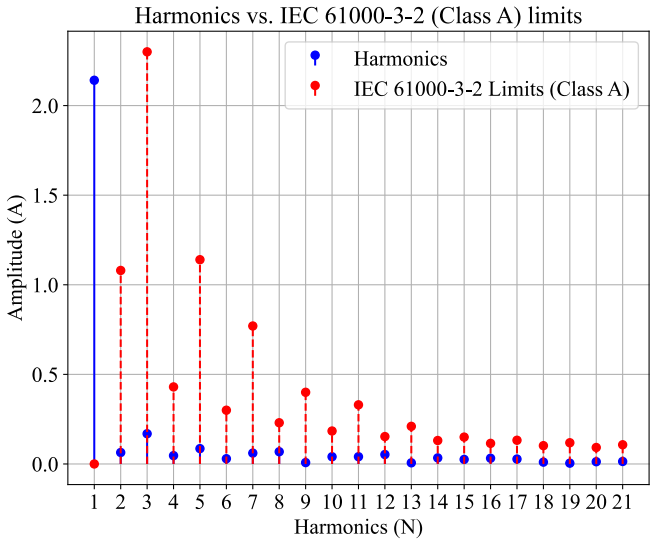

FIGURE 9. FFT comparison with IEC61000-3-2 limits

One of the most significant features of this converter is the reduction of voltage stress on the semiconductors compared to the output voltage. This allows the use of switches and diodes with lower voltage ratings than those required by conventional boost converters. Figure 10 shows the drain-source voltage of MOSFETs S_1 and S_2 in the grid period.

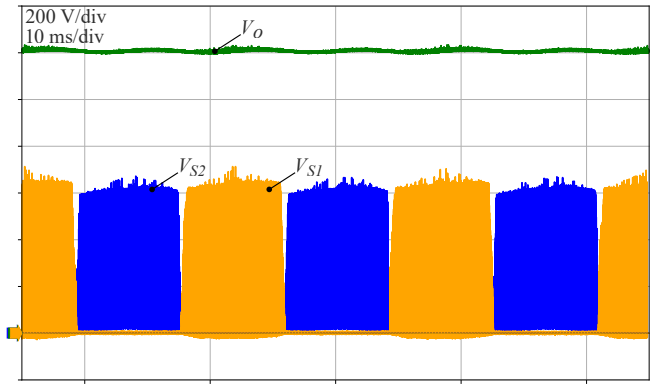

FIGURE 10. Voltage on Switches S_1 and S_2 - grid period

In Figure 10, the operation of the modulation technique, which keeps one of the switches continuously activated for half of the grid period to reduce the switching and conduction losses, can be observed. It also shows that the maximum voltage on the switches is limited to approximately half of the converter's output voltage.

The voltage and current waveforms of the switches in the positive half of the grid period at the switching frequency are presented in Figure 11. The voltage and current waveforms of the switch S_2 highlight the main advantage of operating the converter in discontinuous conduction mode, as the only switching event that incurs power losses occurs during the switch turn off. Due to the chosen modulation strategy for converter operation, which keeps one of the switches turned on throughout the entire half-cycle, the waveforms of switch S_1 indicate that it experiences only switching losses during this period. These losses are further reduced since the current path occurs through the main channel of the MOSFET rather than through the body diode.

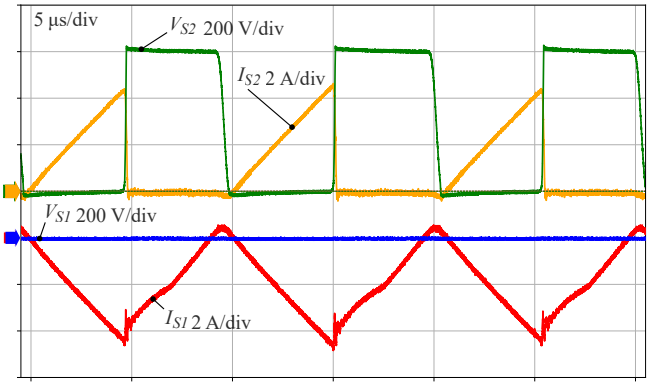

FIGURE 11. Voltage and Current on Switches - switching period on positive half cycle

Figure 12 presents the waveforms of the switches during the negative half-cycle at the switching period. The current waveform of switch S_1 differs from that of switch S_2 during the positive half-cycle, as expected, due to the sum of the switching capacitor C_s charging current and the inductor current flowing through S_1 in this operational stage. Once again, it is observed that the only dissipative switching event occurs during the switch S_1 turn off, while switch S_2 experiences only conduction losses since it remains turned on throughout the entire negative half-cycle.

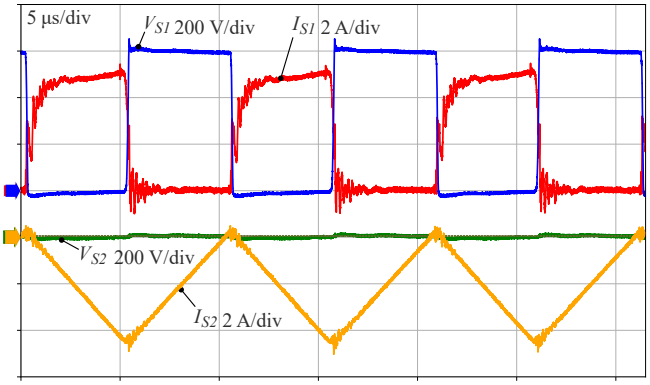

FIGURE 12. Voltage and Current on Switches - switching period on negative half cycle

Figure 13 illustrates the voltage waveforms across the diodes D_b, D_{c1} and D_{c2} along with the output voltage. The results confirm that the diodes experience a maximum blocking voltage of approximately half the output voltage.

Figure 14 illustrates the voltage waveforms across the output capacitors C_{o1} and C_{o2}, as well as the switched capacitor C_s. It can be observed that the average voltage is inherently limited to half of the output voltage without employing any

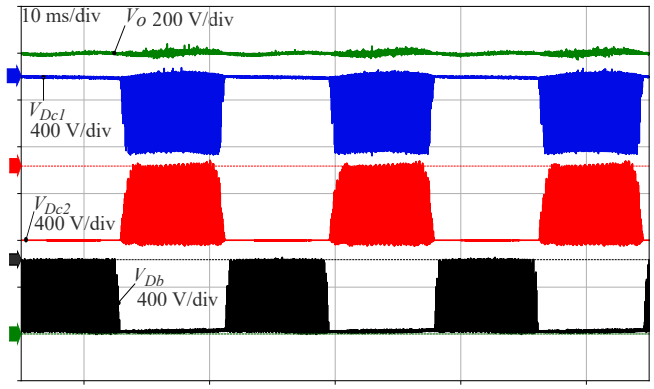

FIGURE 13. Voltage on Diodes D_b, D_{c1} and D_{c2}

specific voltage control technique for the capacitors which is an advantage compared to some multilevel converters. The voltage amplitude across the switched capacitor C_s is slightly lower than that of the output capacitor C_{o1}, as detailed in the converter's operating principles. Additionally, it is evident that the charging of the output capacitor C_{o2} occurs exclusively during the negative half-cycle. During the positive half-cycle, no energy transfer takes place between the converter's input and this capacitor.

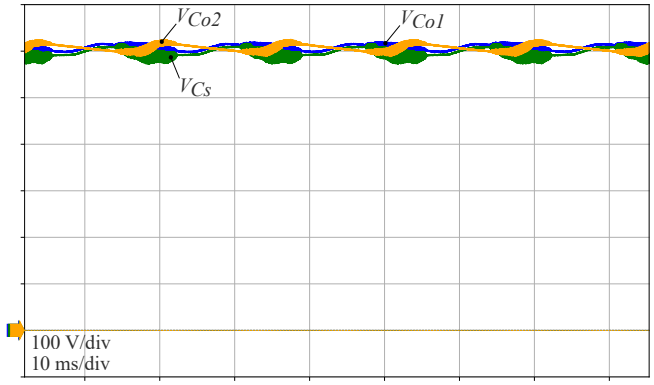

FIGURE 14. Voltage on Capacitors C_{o1}, C_{o2} and C_s

The voltage and current waveforms of the switched capacitor over the grid period are presented in Figure 15. As described in the converter's operating stages, there is no discharge of the switched capacitor during the positive half-cycle, and the charge transfer from capacitor C_{o1} to capacitor C_s is minimal, because the voltage difference between the capacitors is only the direct voltage drop of the diode D_{c1}. Consequently, this current is neglected in the converter design methodology.

Figure 16 presents the waveforms of the switched capacitor C_s during the switching frequency period within the negative half-cycle. Analyzing the positive portion of the current waveform, it can be observed that the charging of the switched capacitor occurs in partial charge mode, validating the capacitor design methodology developed in this work. The capacitor discharge follows the waveform of the current through the boost inductor, as expected. However, a negative current spike is observed, originating from the reverse recovery of diode D_{c2}. This non-ideal characteristic of the converter must be considered when selecting semiconductors to ensure it does not adversely impact efficiency.

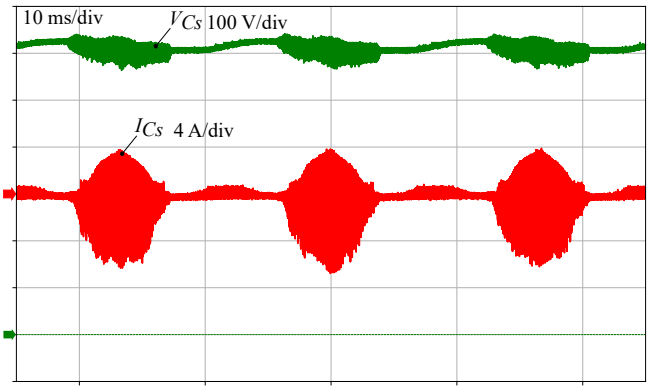

FIGURE 15. Switching Capacitor C_s Waveforms - grid period

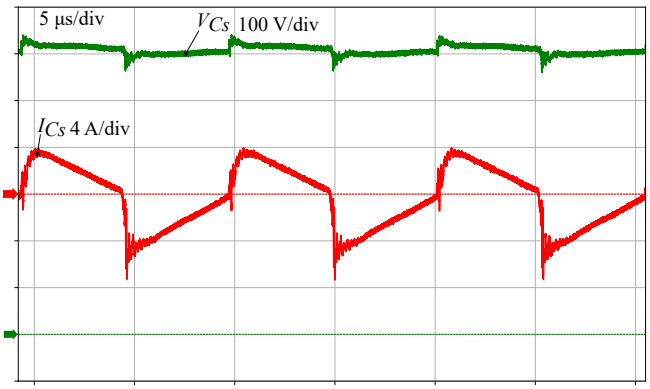

FIGURE 16. Switching Capacitor C_s Waveforms - switching period

Finally, Figure 17 illustrates the voltage and current waveforms of the boost inductor during the grid period, which demonstrate that the converter operates in the discontinuous conduction mode, validating the proposed design methodology.

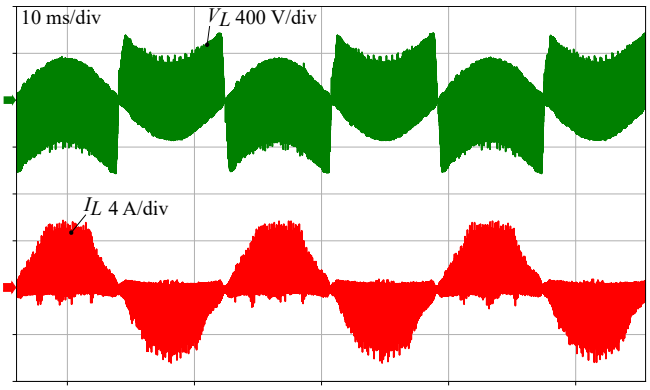

FIGURE 17. Boost Inductor L_b Waveforms - switching period

VI. CONCLUSION

The aim of this article was to develop a design methodology for operating a converter recently proposed in the literature, the single phase bridgeless PFC rectifier with hybrid switched capacitor cell, in discontinuous conduction mode. The proposed converter successfully achieved an output voltage of 1200 V from a 220 V input at rated power with a power factor of 0.99. It demonstrated high efficiency of 97.3% and compliance with IEC61000-3-2 harmonic limits, confirming suitability for Class A electronic equipment.

The design reduces voltage stress on semiconductors, enabling the use of lower-rated components and enhancing reliability. These features highlight the converter's potential for modern applications, such as electroporation, requiring compact, efficient, and low-harmonic solutions.

Future work will focus on integrating active control to further improve performance by THD reduction methods.

ACKNOWLEDGMENT

This work was partially supported by the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), Brazil, under grants 402175/2022-0 and 200163/2022-1.

AUTHOR'S CONTRIBUTIONS

C.MUMIC: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Writing – Original Draft. **M.V.SOARES:** Writing – Review & Editing. **Y.R.NOVAES:** Project Administration, Resources, Supervision, Writing – Review & Editing. **A.J.WATSON:** Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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