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Single-Phase Rectifier with Cascaded-Transformer to Supply a Three-Phase Induction Motor with Open-End Windings

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ABSTRACT This paper presents a single-phase to three-phase AC-DC-AC step-down converter with a symmetrical DC-link voltage ratio. The proposed converter architecture is well-suited for rural distribution grid applications, where a high-voltage single-phase grid is required to transmit energy over long distances while minimizing conduction losses. The converter consists of two cascaded H-bridge converters connected via transformers and two three-phase inverters supplying an open-end winding induction motor (OEWIM). The level-shifted pulse-width modulation (LSPWM) strategy is employed to synthesize the converter voltages. A proportional-integral (PI) controller regulates the overall DC-link voltages, while a hysteresis controller maintains the balance of the individual DC-link voltages. Additionally, a resonant PI controller ensures a sinusoidal grid current, and a Phase-Locked Loop (PLL) is used to achieve a high power factor in the grid. Compared to a conventional two-level leg topology, the proposed configuration reduces harmonic distortion and semiconductor power losses while ensuring a high power factor. Simulation and experimental results validate the effectiveness of the PWM and control strategies.

KEYWORDS AC-DC-AC multilevel converters, cascaded-transformers converter, open-end winding induction motor, single-phase to three-phase.

I. INTRODUCTION

Most electrical grids in the countryside are not three-phase but single-phase, which requires power electronic devices to supply three-phase loads. Three-phase loads are widely used in farms and industrial plants. They present better dynamic performance and can achieve high power levels. On the other hand, single-phase to three-phase converters appear as a possibility to overcome the lack of a three-phase grid. Hence, AC-DC-AC conversion has been the object of study for several years in applications such as three-phase motor drive [1]–[4], uninterrupted power supply (UPS) [5], distributed generation system [6] and power quality conditioner [7] and [8]. The conventional single-phase to three-phase AC-DC-AC converter is presented in Fig. 1.

In high-power medium-voltage drives, the AC-DC-AC multilevel converters have been widely applied as a viable solution to overcome current and voltage limitations of power switches. These converters can generate output voltage waveforms with a large number of levels by using multiple power sources and employing switching devices with lower voltage ratings. In addition, the harmonic distortion, the rate of change of voltage over time (dv/dt), which affects the stress on power switches, the electromagnetic interference (EMI), and the switching losses are reduced [9]. Overall, multilevel converters seek better energy quality from the grid to the loads. In this context, topologies derived from basic module series connections are optimal solutions for high-voltage applications. Among these, the most popular topology is the series H-bridge, implemented with cascaded transformers [10]–[12] and without cascaded transformers [13]–[15]. Additionally, the open-end winding (OEW) concept also appears as an option to achieve multilevel features through series-connection of three-phase converters [16], [17].

Modern applications are increasingly using power electronics devices with stricter requirements regarding the performance of electrical machines. The open-end winding induction machine (OEWIM) is increasingly becoming an interesting alternative due to its advantages over the conventional single-inverter induction motor: 1) multilevel

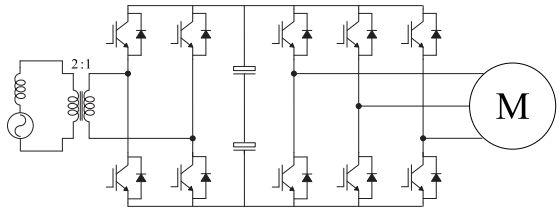

FIGURE 1. Conventional single-phase to three-phase converter.

voltage, enabling a more effective current control, and consequently less torque ripple; 2) greater reliability, since it is capable to operate in the occurrence of faults [18], [19]. The OEWIM can be classified into three types based on the DC power supply configuration of the inverters. The first type uses a single power source supplying both inverters, offering a simple and cost-effective solution. However, this configuration allows zero-sequence current circulation, which does not contribute to torque production and results in additional losses. The second type employs a hybrid approach, where one inverter is powered by a dedicated DC source while the other operates with a floating capacitor. This solution eliminates zero-sequence current but introduces low-frequency harmonic components. The third type utilizes isolated DC sources for each inverter, effectively eliminating zero-sequence current and enhancing system reliability in case of inverter failure. However, this approach increases system costs due to the need for an additional DC source, which can be a limiting factor [20].

This paper proposes an AC-DC-AC topology that resolves the aforementioned issues by incorporating multilevel features while supplying a three-phase open-ended load from a single-phase grid. The rectifier side comprises two series-connected transformers on the primary side, supplying two H-bridge converters through a single-phase grid. On the other hand, the inverter side is composed of two three-phase VSI converters supplying an OEWIM, as shown in Fig. 2. Although the proposed converter has a higher number of power switches compared to conventional converters, it offers a suitable solution for applications where only a single-phase grid is available, such as in rural areas. Since the voltage rating of the switches is reduced, conduction and switching losses can also be minimized.

Overall, the proposed converter provides multilevel features on both the rectifier and inverter sides with galvanic isolation, thereby avoiding circulating current. Despite the presence of a common-mode voltage, zero-sequence current cannot flow because the inverters are supplied by isolated DC sources. This configuration effectively eliminates the common-mode voltage from the actual voltage applied to the motor windings [21], [22]. Additionally, this topology ensures a high power factor close to unity, DC-link voltage control, and controlled output voltages.

The low-frequency transformers (LFTs) may be used to step down the voltage level and provide galvanic isolation between the converters, enabling multilevel voltage operation at both the input and output of the system. The topology can be modified by removing one of the transformers while still maintaining insulation between the DC links. However, to achieve the high input voltage, additional series-connected converters may be necessary. For this reason, in remote rural areas where size and weight are less critical, the version of the converter using two LFT is considered the most suitable solution. However, if the voltage level is compatible with the converter's ratings and galvanic isolation is not required, one transformer can be safely removed, as illustrated in Fig. 2(b). This configuration allows H-bridge converters to interface with a single-phase grid. On the output side, the system includes two three-phase voltage source inverters (VSIs), which supply an open-end winding induction motor (OEWIM), as depicted in Fig. 2. This arrangement can contribute to improved overall system efficiency.

The contributions of the proposed solution include improved power quality on both the grid and load sides. On the grid side, multilevel voltage is utilized to maintain Total Harmonic Distortion (THD) within standard limits while ensuring a high power factor. On the load side, the OEWIM motor drive benefits from reduced torque ripple, elimination of common-mode voltage in the motor windings, and the use of multilevel voltage. Furthermore, an efficient and straightforward DC-link balancing control is implemented, enhancing overall system performance.

The first version of this paper was presented in [23]. This current version includes all content from the original, with the following additions:

1) New analysis and results, including a novel Level-shift PWM (LSPWM) approach and its correlation with single-carrier-based PWM.
2) A DC-link balance control method based on the selection of switching states.
3) A comparative analysis of harmonic distortion and semiconductor losses, demonstrating reduced harmonic distortions and power losses.
4) New simulation and experimental results.

In this way, this paper is organized as follows the proposed structure and its main equations are presented in Section II; the LSPWM strategy for grid and load sides is presented in Section III; a suitable control strategy is presented in Section IV to balance the DC-link voltage by choosing proper switching states, and to ensure sinusoidal grid current, high power factor, and controlled output voltages; analysis in terms of harmonic distortion and semiconductor losses are discussed in Section V; simulation and experimental results under same conditions are presented in Section VI and VII, respectively. Finally, overall conclusions are summarized in Section VIII.

II. SYSTEM MODEL

The proposed topology, illustrated in Fig. 2, is composed of two cascaded H-bridge rectifiers (Converters A and

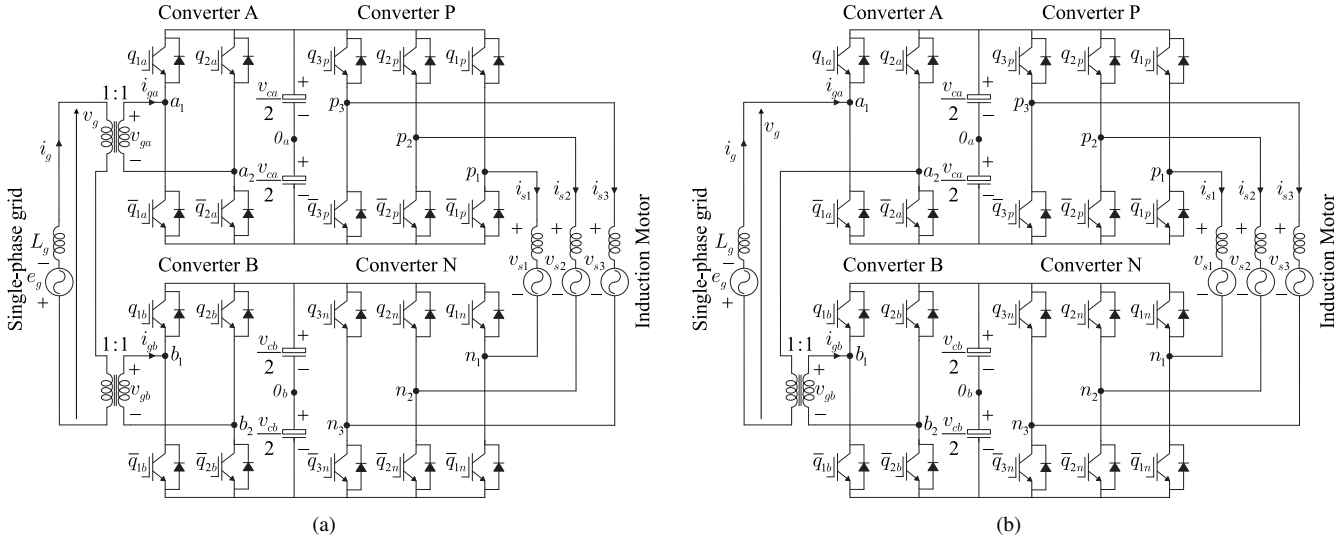

FIGURE 2. Proposed single-phase to three-phase converter with two DC links. (a) With two cascaded transformers. (b) With one cascaded transformer.

B), isolated by two transformers (T_a and T_b), and two three-phase inverters feeding an OEWIM. The transformers ensure galvanic isolation between the grid and power converter, which is required in high-voltage applications, allowing connections of many motor drive systems at the secondary as needed. The system model equations of the input side, referred to the transformer's primary side, are

$$e_g = r_g i_g + l'_g \frac{di_g}{dt} + v_g \tag{1}$$

$$l'_g = l_g + 2l_t \tag{2}$$

$$i_{gk} = n i_g \tag{3}$$

$$v_g = n(v_{ga} + v_{gb}) \tag{4}$$

$$v_{gk} = v_{k10_k} - v_{k20_k} \tag{5}$$

where $k = a, b$ denotes the two converters on the rectifier side; e_g is the grid voltage; i_g is the grid current; i_{gk} are the rectifier currents; and n is the transformer turns ratio (with $n = 1$). The variables v_{gk} represent the rectifier output voltages, while v_{k10_k} and v_{k20_k} are the rectifier pole voltages. The impedance L_g comprises the resistance r_g and the inductance l'_g, which includes the leakage inductance l_t of each transformer (referred to the grid side) and the equivalent input inductance l_g.

The converters P and N are feeding an OEWIM. As shown in Fig. 3, the voltages applied to the machine terminals are denoted as v_{sj}, with $j = 1, 2, 3$. Thus, the converter output voltages can be written as:

$$v_{sj} = v_{pj0_a} - v_{nj0_b} - v_{0_a0_b} \tag{6}$$

where v_{pj0_a} and v_{nj0_b} are the pole voltages of converters P and N, respectively.

$$v_{0_a0_b} = \frac{1}{3}\sum_{j=1}^{3}(v_{pj0_a} - v_{nj0_b}) \tag{7}$$

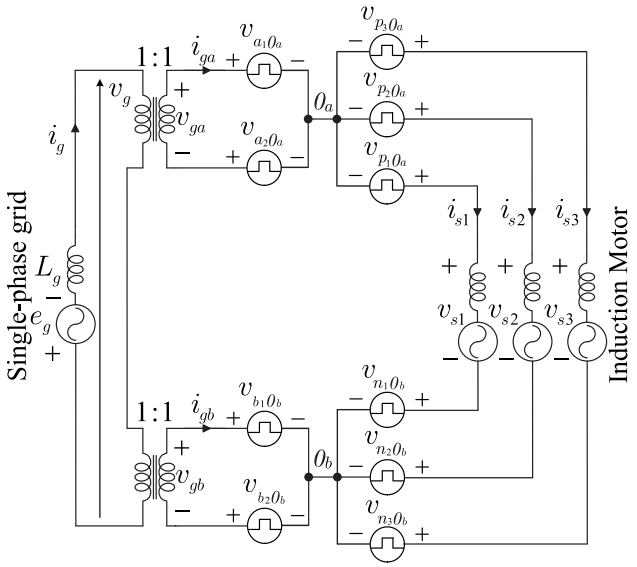

FIGURE 3. Equivalent circuit of the proposed converter.

where $v_{0_a0_b}$ is the voltage between the DC-link midpoints 0_a and 0_b.

III. PWM STRATEGY

A. PWM Strategy of Converters A and B

A level-shifted PWM (LSPWM) strategy is used to define the switching states of the rectifiers (converters A and B) in the proposed converter. The grid-side converter voltage, v_g^*, is modulated to be synthesized by the two rectifiers. The number of synthesized voltage levels and the required carrier signals depend on the DC-link voltage ratio. In this paper, the DC-link voltage ratio is 1:1, so the proposed converter can synthesize up to five voltage levels. These levels are v_g = $[-v_{cT}^*, -v_{cT}^*/2, 0, v_{cT}^*/2$ and $v_{cT}^*]$, where $v_{cT} = v_{ca} + v_{cb}$. Table 1 summarizes all the possible switching states and

TABLE 1. Generated grid voltage, switching states, and their effect on the DC-link voltages depending on the polarity of the current i_g.

Voltage	$q_{1a}q_{2a}q_{1b}q_{2b}$	$i_g \geq 0$		$i_g < 0$	
		v_{ca}	v_{cb}	v_{ca}	v_{cb}
v_{cT}	1010	↑	↑	↓	↓
$\frac{v_{cT}}{2}$	0010	–	↑	–	↓
	1000	↑	–	↓	–
	1011	↑	–	↓	–
	1110	–	↑		↓
0	0000	–	–	–	–
	0011	–	–	–	–
	0110	↓	↑	↑	↓
	1001	↑	↓	↓	↑
	1100	–	–	–	–
	1111	–	–	–	–
$-\frac{v_{cT}}{2}$	0001	–	↓	–	↑
	0100	↓	–	↑	–
	0111	↓	–	↑	–
	1101	–	↓	–	↑
$-v_{cT}$	0101	↑	↑	↓	↓

their output voltages. In addition, to generate v_g with the maximum number of levels, four triangular carriers are required, as shown in Fig. 4. Each carrier is placed between two nearest voltage levels, forming a region known as a sector.

Generally, to generate N levels, N-1 triangular carriers are required. However, most microcontrollers do not support multiple level-shifted carriers. As an alternative, an emulated single-carrier PWM strategy is proposed in [24]. This approach utilizes a single-carrier PWM operating between the limits v_{sup} and v_{inf}, where normally $v_{\text{sup}} = v^*_{cT}/2$ and $v_{\text{inf}} = 0$. The modulating waveform (v^*_g) is modified ($v^*_{g\text{mod}}$) according to the sector, i.e.:

$$v^*_{gmod} = |v^*_g| - V_{off-set} \tag{8}$$

where $V_{off-set}$ is a constant offset. For instance, if $v^*_{cT}/2 < v^*_g \leq v^*_{cT}$ (see Fig. 4), the $V_{off-set} = v^*_{cT}/2$ and if $v^*_{cT}/2 \leq v^*_g < 0$, the $V_{off-set} = 0$ and so on. Then, a single carrier is compared with the modified modulating waveform $v^*_{g\text{mod}}$ to select the proper switching states. All possible switching states are shown in Table 1. These states are shown following the sequence $[q_{1a}q_{2a}q_{1b}q_{2b}]$.

B. PWM Strategy of Converters P and N

The LSPWM is also applied to converters at the load side. Given the three-phase reference output voltages v^*_{sj}, $j = 1, 2, 3$, an auxiliary voltage is introduced as common mode reference v^*_h, Thus obtaining the new reference voltage v^*_{sjh}

$$v^*_{sjh} = v^*_{sj} + v^*_h \tag{9}$$

The auxiliary voltage (v^*_h) is normalized in function of (μ) between its maximum v^*_{hmax} and minimum v^*_{hmin} possible

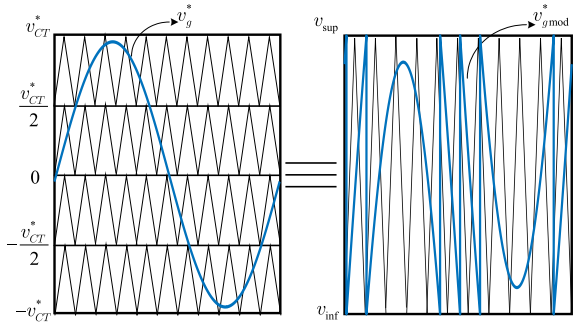

FIGURE 4. Grid side level-shifted PWM Strategy and its equivalent single-carrier modulation.

values, as presented in [25],

$$v^*_h = \mu v_{hmax} + (1-\mu)v_{hmin} \tag{10}$$

$$v_{hmax} = \frac{v_{cT}}{2} - \max(v^*_{s1}, v^*_{s2}, v^*_{s3}) \tag{11}$$

$$v_{hmin} = -\frac{v_{cT}}{2} - \min(v^*_{s1}, v^*_{s2}, v^*_{s3}) \tag{12}$$

The reference voltages (v^*_{sjh}) are applied in the LSPWM strategy to define the switching states of converters P and N. The output converter's voltages generate up to three voltage levels using this technique, which would mean two triangular carriers per phase, as shown in Fig. 5. The modulating approach can be emulated using a single-carrier per phase, as implemented for the grid side. The switching states for each level are also shown in these figures.

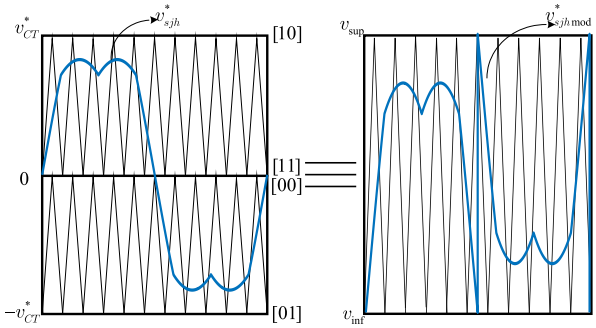

FIGURE 5. Load side level-shifted PWM Strategy and its equivalent single-carrier modulation.

IV. CONTROL STRATEGIES

Fig. 6 presents the control block diagram of the proposed configuration. Initially, the two DC-link voltages are controlled through the average DC-link voltage [$v_c = (v_{ca} + v_{cb})/2$]. The voltage v_c is adjusted to its reference value v^*_c using a proportional-integral (PI) controller. This controller determines the amplitude of the reference grid current (I^*_g), located on the primary side of the transformer. The reference current (i^*_g) is synchronized with the grid voltage (e_g) using a Phase Locked-Loop (PLL). This ensures a high power factor on the grid side. In addition, a resonant PI controller (R_i) [26] is used to control the grid current. The output of

this controller is the reference voltage v_g^*, which is used in the PWM strategy.

Once the average DC-link voltage is controlled, an individual control is applied to one of the DC links to ensure that both are properly regulated. Since different switching states can generate the same voltage vector, each with a distinct effect on the DC-link currents, these redundancies can be utilized to balance the DC-link voltages effectively. This can be observed by the DC-link currents, which are given by

$$i_{ca} = q_{1a}i_{ga} - q_{2a}i_{ga} - q_{3p}i_{s3} - q_{2p}i_{s2} - q_{1p}i_{s1} \quad (13)$$

$$i_{cb} = q_{1b}i_{gb} - q_{2b}i_{gb} + q_{3n}i_{s3} + q_{2n}i_{s2} + q_{1n}i_{s1} \quad (14)$$

Each switching state of converters A and B can increase or decrease the energy transferred from the grid to the load. When the energy transferred from the grid is bigger than the load energy, the capacitor voltage rises (i.e., $i_{ck} > 0$ with $k = a, b$); otherwise, the capacitor voltage decreases. The effect of each switching state on the DC-link voltage is summarized in Table 1. The hysteresis control continuously monitors one of the DC-link voltages and adjusts it when it reaches the specified upper or lower limit. When the lower limit is reached, specific switching states are applied during the PWM period to charge the DC-link; otherwise, when the upper limit is reached, switching states are selected to discharge the DC-link. The specified limits form the hysteresis band, ensuring that the controlled voltage fluctuates within the allowed range, Δv_{cb}.

To maintain v_{cb} between the hysteresis band, the voltage vectors are chosen as follows:

1) if $v_{cb} - v_{cb}^* > \Delta_{vcb}$ – a voltage vector is selected to decrease v_{cb} or to increase v_{ca}.
2) if $v_{cb} - v_{cb}^* < -\Delta_{vcb}$ – a voltage vector is selected to increase v_{cb} or to decrease v_{ca}.

For example, if $0 < v_g^* < \frac{v_{cT}}{2}$ and the grid current is positive. In this case, the voltage vectors 0010 and 1110 increase the voltage v_{cb}, while the vectors 1000 and 1011 increase the voltage v_{ca}.

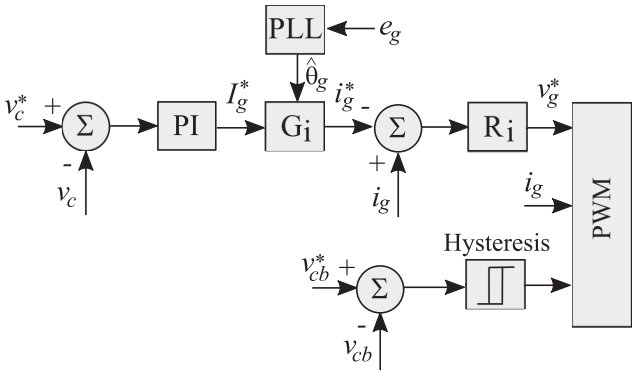

FIGURE 6. System block control diagram of proposed configuration.

V. COMPARATIVE ANALYSIS

The conventional and proposed topologies are analyzed and compared regarding harmonic distortions and semiconductor losses. All analyses are performed under steady-state open-loop simulations considering the same operation conditions, as detailed in Table 2.

Two voltage levels are investigated while keeping the same power in both cases. In the first scenario (lower voltage), the grid voltage is 220 V and the output voltage is 110 V. In the second scenario (higher voltage), the grid voltage is 440 V and the output voltage is 220 V. In addition, the topologies are investigated: (i) operating with the same carrier frequency (f_c), and (ii) with different carrier frequencies to achieve the same grid current THD.

TABLE 2. Simulation parameters for comparative analysis.

Parameter		Value
Grid voltage	e_g	220 V and 440 V (RMS)
Grid impedance	Z_g	5%
Load voltage	v_l	110 V and 220 V (RMS)
Grid frequency	f_g	60 Hz
Carrier frequency	f_c	10 kHz
3ϕ load	P_l	5 kW
PF load	PF	0.8

A. Number of Components and Voltage Levels

A comparison of different single-phase to three-phase topologies with the proposed topology, in terms of power devices and generated voltage levels, is presented in Table 3. All the analyzed topologies have the same number of power switches.

TABLE 3. Comparison of different single-phase to three-phase topologies.

	Proposed	Single-carrier/ Double-carrier [27]	Neutral-Point Clamped (NPC)
Diodes	-	-	10
Inductors	1	4	1
Switches	20	20	20
DC links	2	2	1
Low-frequency transformers	2*	1	1
Input voltage levels	5	3	5
Output voltage levels	9	5 / 7	9

* can be reduced to one.

The topology presented in [27] has a transformer with its secondary side powering the rectifiers in parallel, which allows current circulation and requires four filter inductors. Moreover, this topology generates multilevel output voltages with fewer and unevenly distributed levels. Another topology that can be considered is an NPC topology

with a configuration identical to the one shown in Fig. 1. This topology would generate the same number of voltage levels as the proposed one. However, this topology has ten clamping diodes, and the transformer processes 100 % of the total power. On the other hand, the proposed converter uses two transformers, each processing only half of the total power (see Fig. 2(a)). Alternatively, a single transformer with a center tap on the secondary can be used to supply the rectifiers in isolation. In addition, as shown in Fig. 2(b), one transformer can be removed if the grid voltage level is compatible with the converter's voltage.

The following comparison is done between the proposed topology (see Fig. 2(a)) and the conventional topology (see Fig. 1).

B. Harmonic Distortions

The total harmonic distortion (THD) and weighted total harmonic distortion (WTHD) are used to evaluate the quality of the grid current and load voltage waveforms, respectively. The results were obtained using the equations presented in [28] and are summarized in Table 4.

The simulated waveforms of the proposed and conventional configurations operating with the same carrier frequency ($f_c = 10$ kHz) and in the first scenario (lower voltage) are shown in Fig. 7. The topologies present a THD of 5% and 2.68%, for conventional and proposed topologies, respectively. In addition, the output voltage WTHD values are 0.28% and 0.12%, respectively. Thus, the proposed topology achieves a 46.4% reduction in THD and a 57% reduction in WTHD compared to the conventional one. Similar results were observed in the second scenario (higher voltage).

TABLE 4. Harmonic distortion analysis.

	Conventional	Proposed
THD (f_c = 10 kHz)	5 %	2.68 %
WTHD (f_c = 10 kHz)	0.28 %	0.12 %
f_c (THD = 5%)	10 kHz	5.5 kHz

The results of the proposed configuration can be attributed to the higher number of voltage levels on both the grid and load sides (see Fig. 7). The proposed topology generates five levels on the grid side and nine on the load side, whereas the conventional topology generates three levels on the grid side and five levels on the load side. In this way, the proposed topology can be designed with smaller passive filters or can operate with a lower carrier frequency to achieve the same performance as the conventional topology. The first option may result in a reduction in manufacturing costs, while the second option leads to reduced power losses, which can translate to a longer lifespan for the power switches and energy savings. Table 4 shows the carrier frequencies for each topology operating with 5% of THD. It is noteworthy that the proposed converter can reduce the switching frequency, resulting in a frequency 45% lower than that of the conventional topology.

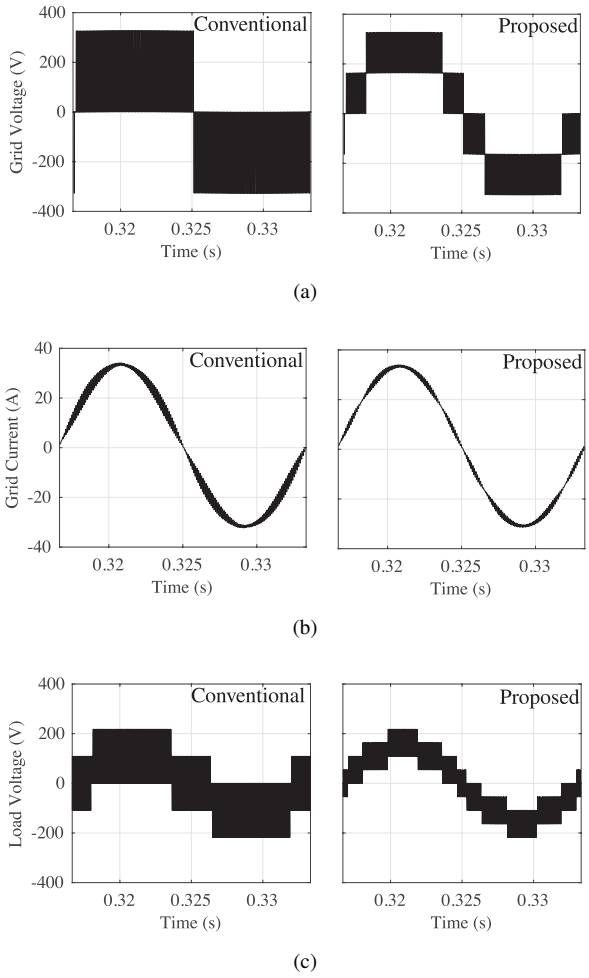

FIGURE 7. Simulated waveforms comparing the conventional and proposed converters. (a) Grid voltage. (b) Grid current. (c) Load voltage.

At last, the THD of grid current is evaluated over a range of load power, as shown in Fig. 8. For this analysis, the grid impedance is kept constant. As can be seen, the proposed topology demonstrates better performance across the entire power range.

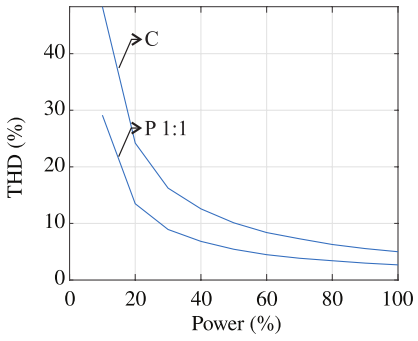

FIGURE 8. THD of grid current vs load power.

C. Semiconductor losses analysis

The semiconductor losses include both conduction and switching losses of the transistor and its anti-parallel diode. The results were obtained using PSIM, with the switch model developed based on the Littelfuse MG0675S-BN4MM datasheet [29]. This device was chosen to support the analyzed voltage and current levels, with a maximum rating of 600 V and 75 A.

Conduction and switching losses on the switches can be found by applying (15) and (16), respectively [30].

$$P_{COND} = V_{CEO} I_{AVG} + R_c I_{RMS}^2 \tag{15}$$

$$P_{SW} = \frac{1}{2\pi} \int_0^{2\pi} W(\omega t) d(\omega t) \tag{16}$$

where V_{CEO} is the IGBT on-state zero current collector-emitter voltage drop, R_c is the collector-emitter on-state resistance, W is the switching loss energy shown in (17).

$$W(\omega t) = k_0 + k_1 i(\omega t) + k_2 i(\omega t)^2 \tag{17}$$

where k_0, k_1 and k_2 are coefficients that represent the contributions of energy loss by switching (turn on and turn off). These coefficients can be obtained with linear regression through a second-order polynomial from the datasheet energy curves provided by the manufacturer.

Fig. 9 presents the semiconductor losses for the conventional (C) and proposed (P 1:1) topologies. The losses are categorized into conduction and switching losses for both the rectifier and inverter, as indicated by the labels. As mentioned earlier, two sets of voltages levels were investigated, the first with lower voltage, as shown Figs. 9(a) and 9(b), and the second for higher voltage, as shown in Figs. 9(c) and 9(d). The losses are normalized based on conventional losses, representing 285 W for the first case and 160 W for the second case.

Two scenarios are investigated for the two sets of voltages:

- Scenario i – topologies operating with the same carrier frequency, i.e., $f_c = 10$kHz. This scenario is presented in Figs. 9(a) and 9(c);
- Scenario ii – topologies operating with the same THD = 5%, which means different carrier frequencies per topology. These frequencies are shown in Table 4. This scenario is presented in Figs. 9(b) and 9(d).

In both scenarios, the proposed topology presents lower losses than the conventional one, with its efficiency being maximized in scenario ii. For lower voltage applications, the P 1:1 reaches 25% lower losses compared to the C topology, considering the same THD (i.e., 5% of THD) (see Fig. 9(b)). On the other hand, for higher the voltage applications, the proposed topology becomes even more efficient, as shown in Fig. 9(d), achieving 30% lower losses than the C topology. As already mentioned, the THD advantage of the proposed topology can be leveraged to reduce switching losses by operating at a lower switching frequency. Furthermore, the proposed topology becomes even more attractive for higher voltages and lower current applications.

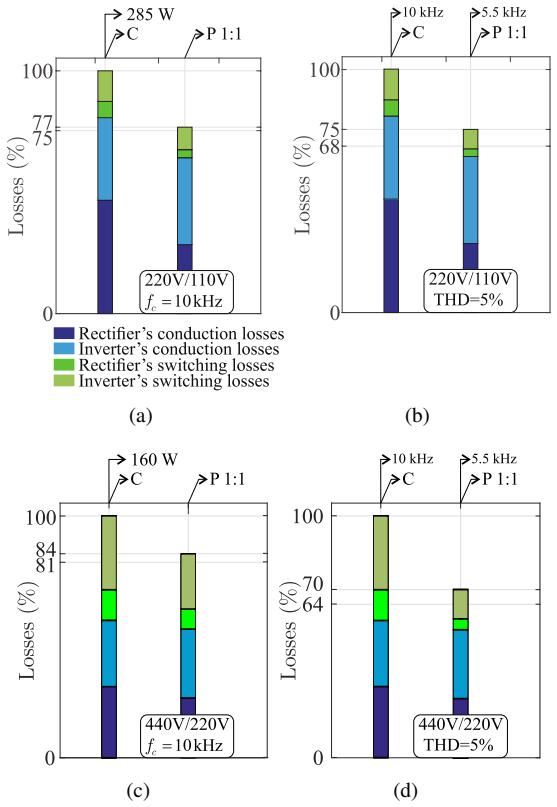

FIGURE 9. Semiconductor losses analysis. (a) and (b) V_g and V_l equal to 220V and 110V, respectively. (c) and (d) V_g and V_l equal to 440V and 220V. (a) and (c) Topologies operating with the same carrier frequency $f_c = 10$ kHz (scenario i). (b) and (d) Topologies operating with the same THD = 5% (scenario ii).

Semiconductor power losses are illustrated in Fig. 10 for a power range of 10% to 100% of nominal load power (5 kW). The results indicate that the proposed topology is consistently more efficient than the conventional one at all power levels, with an efficiency advantage for higher power. For this analysis, the carrier frequency was maintained at 10 kHz to ensure optimal THD performance, as shown in Fig. 8.

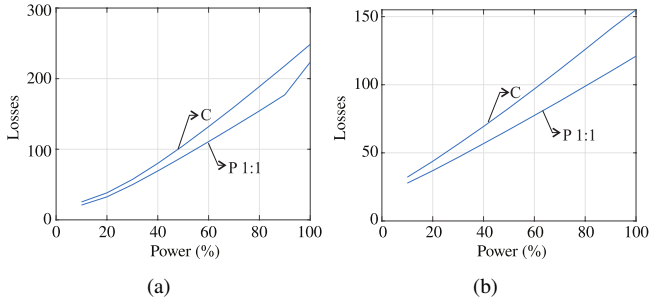

FIGURE 10. Semiconductor losses for different load power. (a) For 220/110 V. (b) For 440/220 V.

VI. SIMULATION RESULTS

Computer simulations were carried out using PSIM software. The circuit parameters are detailed in Table 5. The system supplies an RL load rated at 460 W with a power factor of 0.8, connected with open terminals.

TABLE 5. Parameters used in the simulated and experimental results.

Parameter		Value
Grid voltage	e_g	127 V (RMS)
Grid inductance	l_g	6.7 mH
Grid resistance	r_g	0.1 Ω
Grid frequency	f_g	60 Hz
Transformers turn ratio	n	1:1
Load voltage	v_l	77.7 V (RMS)
Load frequency	f_l	60 Hz
DC-link capacitance	C	2200 μF
Carrier frequency	f_c	10 kHz
DC-link Voltage	v_c	210 V

The simulation results are presented in Fig. 11 for the proposed topology. Fig. 11(a) shows waveforms of the grid voltage (e_g) and current (i_g), which are in phase, resulting in a power factor close to unity. The grid voltage is 127 V and the grid current is 3.62 A. The current THD achieved 3.18 %, thus demonstrating the current control's correct operation. The results indicate that the grid current THD was lower than that specified by the standard. Fig. 11(b) shows the converter input voltage waveforms, which have five voltage levels. The DC-link voltages v_{ca} and v_{cb} are well regulated to 105 V (see Fig. 11(c)).

Fig. 11(d) shows the output converter voltages (v_{s1}, v_{s2} and v_{s3}). These voltages present nine levels, as expected. Fig 11(e) shows the output converter currents (i_{s1} and i_{s2}) with 2.3 A and their corresponding average output voltage. The output currents THD was 0.45 %. The average switching frequencies f_{sw} per leg can be obtained from pole voltages. Fig 11(f) shows them (v_{a10a}, v_{a20a}, v_{b10b} and v_{b20b}), all power switches operate during half circle which means $f_{\text{sw}} =$ 5kHz.

Figs. 11(g) and 11(h) illustrate the simulated waveforms during a load transient. To evaluate the dynamical performance of the system, a step change was applied in the load, varying from 50 Ω to 37.5 Ω, and vice versa. As can be seen, the voltages v_{ca} and v_{cb} were well regulated, remaining at half of the DC-link voltage, i.e, 105 V. These results demonstrate the proper operation of the implemented control strategy.

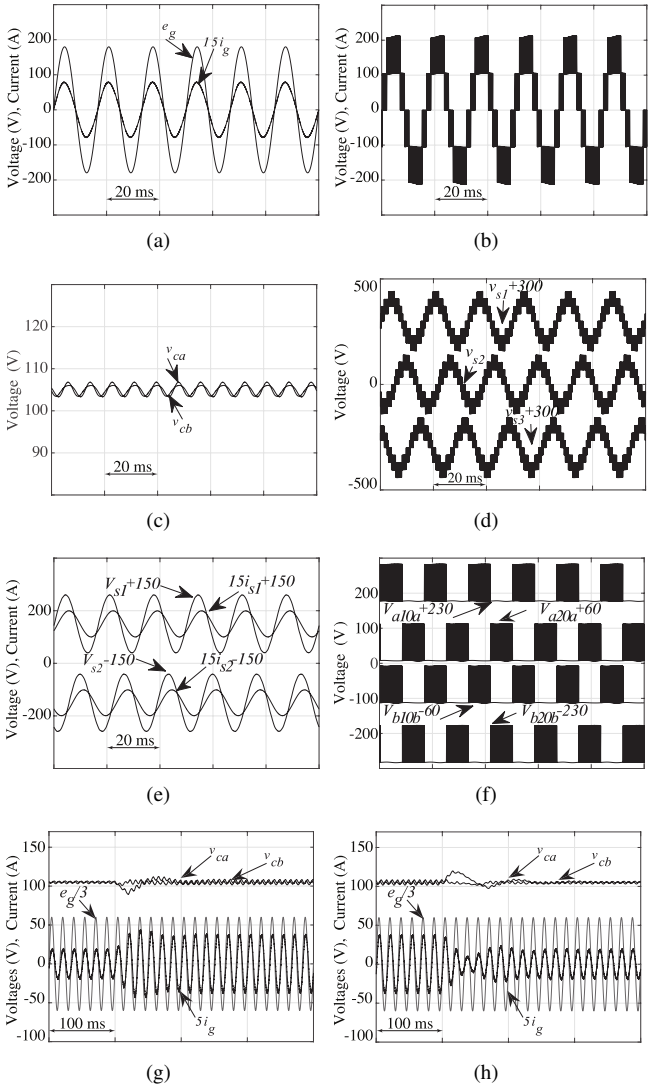

FIGURE 11. Simulation results. (a) Grid's voltage (e_g) and current (i_g). (b) Input voltage (v_g). (c) Voltages v_{ca} and v_{cb}. (d) Load voltages (v_{s1} and v_{s2}). (e) Average load voltages (v_{s1} and v_{s2}) and currents (i_{s1} and i_{s2}). (f) Rectifier pole voltages (v_{a10a}, v_{a20a}, v_{b10b} and v_{b20b}). (g) Transient response of v_{ca} and v_{cb}, e_g and i_g, for load increasing. (h) Transient response of v_{ca} and v_{cb}, e_g and i_g, for load decreasing.

VII. EXPERIMENTAL RESULTS

The proposed topology was implemented in the laboratory using the same simulation parameters to validate the results. Due to equipment and component limitations, the experiments were conducted at reduced voltage and current levels. The experimental setup was based on a digital signal processor (DSP), model TMS320F28379D, with a microcomputer equipped with plug-in boards and sensors. The converters use power switches model SKM50GB123D with drivers SKHI-23. The loads resistance and inductance were 50 Ω and 7 mH. The experimental waveforms for the proposed topology are shown in Fig. 12.

Fig. 12(a) shows the grid voltage (e_g) and current (i_g). As can be observed, the current is sinusoidal and in phase with e_g, ensuring a unity power factor. Fig. 12(b) shows the converter voltage at the grid side (v_g), which generates five voltage levels. Fig. 12(c) illustrates the DC-link voltages v_{ca} and v_{cb}. The two DC-link voltages are regulated and balanced to their reference values, i.e, both voltages are around 105 V. These voltages present a low-frequency

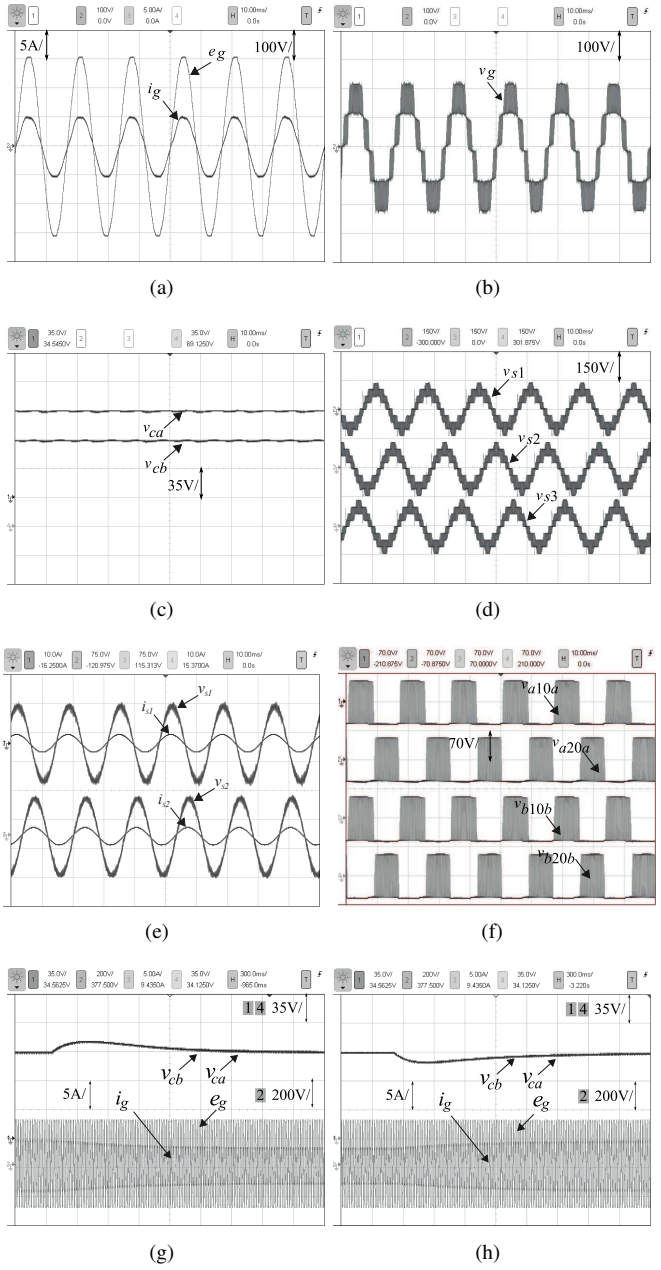

FIGURE 12. Experimental results. (a) Grid voltage (e_g) and current (i_g). (b) Input voltage (v_g). (c) Voltages v_{ca} and v_{cb}. (d) Load voltages (v_{s1} and v_{s2}). (e) Average load voltages (v_{s1} and v_{s2}) and currents (i_{s1} and i_{s2}). (f) Rectifiers' pole voltages (v_{a10a}, v_{a20a}, v_{b10b} and v_{b20b}). (g) Transient response of v_{ca}, v_{cb}, e_g, and i_g, for load decreasing. (h) Transient response of v_{ca}, v_{cb}, e_g, and i_g, for load increasing.

component (twice grid frequency), an intrinsic condition of single-phase systems.

The converter output voltages (v_{s1}, v_{s2} and v_{s3}) that supply the three-phase open-ended load are shown in Fig. 12(d). These voltages have nine levels. Their average values and load currents (i_{s1} and i_{s2}) are shown in Fig. 12(e). Fig. 12(e) shows the rectifiers' pole voltages on the grid-side converters, which alternate between $-v_{ca}/2$ and $v_{ca}/2$.

To test the control response to load variations, the resistive part of the load is changed from 37.5 Ω to 50 Ω for Fig. 12(f) and the opposite in Fig. 12(g). These results show the dynamical response of the DC-link voltages (v_{ca} and v_{cb}), the grid voltage (e_g) and the grid current (i_g). It can be observed that the voltages and currents remain stable in both load variations. These results show the proper functioning of the applied controls. Therefore, experimental results are entirely consistent with the simulation results.

VIII. CONCLUSIONS

This paper has proposed a new topology for step-down applications, where converters on the grid side are cascaded connected, and the three-phase load is open-ended connected. The system's symmetric operation has been investigated, and the corresponding system model, LSPWM strategy, and control approach have been described. The proposed topology was compared with the conventional one in terms of THD (for grid current), WTHD (for load voltage), and semiconductor losses under two specific scenarios: (i) all topologies operating at the same carrier frequency and (ii) all topologies operating at the same THD, which implies different carrier frequencies. Regarding the semiconductor losses, in both scenarios, the proposed topology demonstrated better performance, achieving up to 30% lower losses.

The proposed topology provides multilevel voltages at both the grid and load sides, resulting in improved waveform quality compared to the conventional topology. This led to reductions of 46.4% in THD and 57% in WTHD. These enhancements can be leveraged to reduce either the size of passive filters or the switching frequency. A reduction in passive filters means lower manufacturing costs, while a lower switching frequency leads to reduced semiconductor losses and improved energy efficiency. Simulation and experimental results under steady-state and transient-state have shown the effectiveness of the PWM strategy and control algorithm. The proposed topology appears to be a good option for applications where only a single-phase grid is available, such as in rural areas.

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AUTHOR'S CONTRIBUTIONS

A.D.D.ALMEIDA: Formal Analysis, Investigation, Validation, Writing – Original Draft. **B.S.GEHRKE:** Investigation, Validation, Writing – Review & Editing. **N.ROCHA:** Conceptualization, Formal Analysis, Supervision. **E.L.L.FABRICIO:** Conceptualization, Investigation, Supervision. **C.A.CALDEIRA:** Writing

– Review & Editing. **G.M.S.RODRIGUES:** Writing – Review & Editing. **I.S.FREITAS:** Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

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