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Validation of controllers for photovoltaic inverters using automated tests and hardware-in-the-loop

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ABSTRACT

The ABNT NBR-16149 and NBR-16150 standards and INMETRO Ordinance No. 140 establish requirements for connecting PV inverters to the Brazilian electrical grid. To meet these requirements, the firmware of these devices needs to be properly designed and validated. Additionally, it is important to perform tests to verify whether the inverter and its control systems comply with the standards. In this context, this paper presents a methodology for the validation of controllers for PV inverters using Hardware-in-the-loop (HIL). To validate the proposed methodology, a two-level three-phase PV inverter with Finite Control Set Model Predictive Control (FCS-MPC) for current control and additional control and grid connection functionalities was evaluated. The compliance of the controller with relevant standards was assessed through automated HIL testing. This approach allows control designers to identify potential issues in advance, refine algorithms, and enhance controller performance before the complete hardware certification process of the inverter.

KEYWORDS Finite Control Set Model Predictive Control, Automated Tests, Hardware-in-the-loop, Photovoltaic Inverter, Power Electronics

I. INTRODUCTION

In the last few years, there has been a significant increase in photovoltaic (PV) electric power generation in Brazil. According to the International Renewable Energy Agency (IRENA) [1], Brazil ranks as the sixth-largest country in PV generation in May 2024. Therefore, PV have gained great attention in industry and academia, as they are responsible for interfacing the PV systems with the grid.

For PV inverters to be commercialized, they must first undergo a certification process. In Brazil, the certification of a PV inverter consists of 26 test procedures performed in accredited laboratories and specified by NBR-16149 [2], NBR-16150 [3] ABNT norms, and INMETRO Ordinance 140 [4]. Inverter controllers and grid connection algorithms must be designed to comply with these requirements. The validation of the inverter firmware is typically performed after its implementation in hardware, for this reason, in [5], [6], automated test platforms for the certification of PV inverters were presented, with [5] for the Brazilian standards NBR-16149 [2] and NBR-16150 [3] using LabVIEW (LEN Test Software) to evaluate the conformity of PV grid-connected inverters and [6] for the Chinese grid connection standards using Kingview software. However, validation tests using HIL are a less costly and time-consuming alternative compared to tests performed in laboratories.

Hardware-in-the-loop (HIL) has been used in various industrial applications such as aerospace [7], communications [8], robotics [9], battery chargers [10], [11], electric machines [12], [13], energy storage [14], [15], and especially microgrids as noted in [16], [17]. In [18], a wind generator control system was implemented in HIL. In [19], the performance of a controller implemented in a high power three-phase active filter was tested using Controller Hardware-in-the-Loop (C-HIL). In addition, [20] proposed a C-HIL framework for the real-time validation of microgrid controllers, where C-HIL combines simulation with real controller [20], [21]. In this approach, the control algorithm is implemented in a microcontroller, while the power circuit elements are emulated in HIL.Some papers on inverter testing using HIL can be found in the literature, such as [22], which presents C-HIL results obtained in compliance with European technical standards. In addition, [23] outlines the core principles of Controller-Hardware-in-the-Loop (C-HIL) and Power-Hardware-in-the-Loop (P-HIL) testing within the context of renewable energy integration. In P-HIL, real hardware operates within a simulated environment, allowing actual power exchange between physical

and virtual components [24], [25], thereby enabling more accurate performance assessments under realistic operating conditions. In [26], a P-HIL platform is presented to test advanced functionalities of inverters connected to the power distribution system.

As a result, it can be concluded that HIL is an effective solution for validating inverter firmware. considering this, a platform for automated testing and certification of PV inverter firmware based on the Brazilian standards NBR 16149 [2], NBR 16150 [3], and INMETRO Ordinance 140 [4] was developed by [21], [27]. In [28], the HIL validation strategy is presented with a focus on Low Voltage Fault Ride Through tests (LVRT). Additionally in [21], [28] the test setup and the logical sequence the test script follows to carry out a test are explained. Also in the field of power electronics, [29] presents a stability assessment for grid-connected electronic equipment applying a HIL testing concept. The advantage of this method is the faster development process without the risk of damaging equipment. In [30], the automated test platform was validated by comparing results from HIL simulations with those obtained in real laboratory experiments, using statistical analysis to evaluate the accuracy and consistency between both approaches. This comparison highlights the accuracy and reliability of the HIL-based automated tests.

In this context, this paper aims to demonstrate that the HIL strategy is a viable solution for validating controllers and grid connection functionalities for PV inverters. In order to do so, a case study will be presented considering a two-level three-phase inverter connected to the grid with an LCL filter. The inverter firmware includes functionalities such as current control, power control, DC bus voltage control, Maximum Power Point Tracking (MPPT) algorithm, and grid connection features that the inverter must comply with to meet Brazilian standards [2], [3], and [4]. For this case study, the automated HIL pre-certification testing platform developed in [21], [30], [31] will be used.

The main contributions of this paper are:

- Demonstrate that automated HIL testing is a viable solution for validating the firmware of photovoltaic inverters;
- Prove the effectiveness of HIL automated testing as well as how it enables rapid analysis and correction of firmware errors;
- Demonstrate that the automated HIL testing is a viable solution for validating the firmware of medium-power systems;
- Demonstrate the feasibility of assessing the inverter's behavior under a range of operating conditions, especially those defined by Brazilian standards.
- Implement a FCS-MPC with grid-connection functionalities, which, to the best of our knowledge, has not been previously reported in the literature.

this paper is an extension of [32], and the main differences with respect to [32]] are:

- An extended literature review is included;
- Results and analysis of additional automated tests in HIL are included;
- A more detailed theoretical development of the control functions;
- Enhancement of DC-link voltage control with the addition of anti-windup.

The remainder of this paper is divided as follows: Section II describes the controllers implemented for the inverter; Section III describes the specifications of the Brazilian standards; Section IV describes the operation of the automated HIL tests; Section V presents the results of the automated HIL tests; Section VI concludes the paper.

II. CONTROL FUNCTIONALITIES

In this section, the controllers implemented for the considered three-phase two-level inverter with LCL filter will be presented. Figure 1 shows the schematic of the inverter with the block diagram of the control system.

Figure 1 illustrates the system, where the control system consists of four loops. The outermost loop is the MPPT algorithm, which identifies the maximum power point and establishes the reference for the DC bus voltage. The DC bus control loop generates the active power reference, followed by the power control loop, which provides the current reference. This reference is used by the FCS-MPC current control to minimize the cost function error, as detailed later. Also in Figure 1, the grid-connection functionalities are designed to guarantee compliance of the inverter with regulatory standards.

The system was modeled in the $\alpha\beta$ reference frame, as this approach enables decoupling between the axes, thereby allowing independent control of the alpha and beta components.

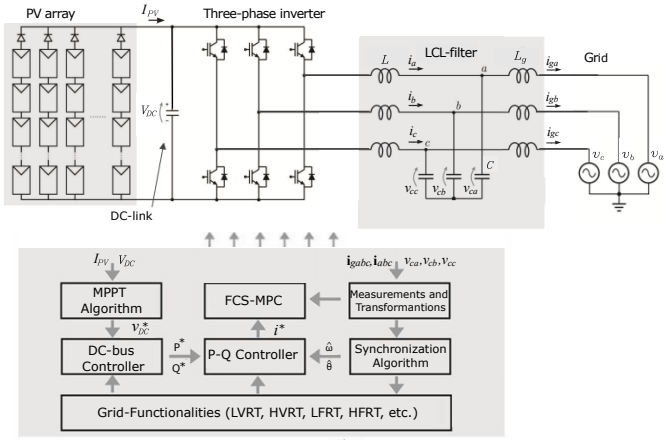

FIGURE 1. Schematic of the three-phase two-level inverter considered in this paper. Adapted from [33].

A. Synchronization algorithm

The literature presents a variety of grid synchronization methods. In this paper, the simplest approach was adopted, in which the angle θ is obtained from the grid voltages v_α and v_β. The most simple method was chosen because the main objective of this paper is to demonstrate that automated testing is a viable tool for validating photovoltaic inverter controllers.

The angle θ is calculated from the grid voltages $\mathbf{v}_{\alpha\beta}$ according to (1).

$$\theta(k) = \arctan \frac{v_\beta(k)}{v_\alpha(k)} \tag{1}$$

From θ the angular frequency $\omega(k)$ is calculated by (2);

$$\omega(k) = \frac{\theta(k) - \theta(k-1)}{T_s} \tag{2}$$

After that, the frequency $f(k)$ is calculated by (3).

$$f(k) = \frac{\omega(k)}{2\pi} \tag{3}$$

B. Current control

In this paper, the FCS-MPC strategy was selected for the inverter current control, offering an effective alternative to classical power converter controllers [34]. The idea of this strategy is the prediction of the future states of the converter for all its switching vectors [34], [35], [36]. Through a cost function, the switching vector that minimizes the error between the current references and the predicted inverter currents is chosen and implemented by the inverter [37]. In [38], the FCS-MPC control strategy is analyzed for various power electronics applications, demonstrating superior transient performance and greater robustness to parameter variations compared to classical control methods. The equation of the inverter-side current in alpha-beta coordinates is given by (4):

$$\mathbf{i}_{\alpha\beta}(k+1) = \mathbf{i}_{\alpha\beta}(k) + \frac{T_s}{L}\mathbf{u}_{\alpha\beta}(k) - \frac{T_s}{L}\mathbf{v}_{c\alpha\beta}(k) \tag{4}$$

Where $\mathbf{i}_{\alpha\beta}(k+1)$ e $\mathbf{i}_{\alpha\beta}(k)$ are the inverter-side currents, $\mathbf{v}_{c\alpha\beta}(k)$ are the voltages of the filter capacitors, $\mathbf{u}_{\alpha\beta}(k)$ are the inverter voltages, T_s is the sampling time, L is the inverter-side inductance. In addition, the implementation delay of the processor must also be included in the formulation of the FCS-MPC [39].

$$\mathbf{i}_{\alpha\beta}(k+2) = \mathbf{i}_{\alpha\beta}(k+1) + \frac{T_s}{L}\mathbf{u}_{\alpha\beta}(k+1) - \frac{T_s}{L}\mathbf{v}_{c\alpha\beta}(k+1) \tag{5}$$

In FCS-MPC, the cost function is calculated at each sampling instant for all inverter voltage vectors $\mathbf{u}_{\alpha\beta}$, and the vector with the lowest cost is selected to be implemented. Equation (6) defines the cost function of the MPC, where $\mathbf{i}^*_{\alpha\beta}$ is the reference current and J is the cost function that will be calculated. The definition of the reference current will be detailed in Section D.

$$J = |\mathbf{i}_{\alpha\beta}(k+2)^* - \mathbf{i}_{\alpha\beta}(k+2)|_2^2 \tag{6}$$

The matrix notation is:

$$J = \|\mathbf{H}\mathbf{u} + \mathbf{h}\|_2^2 \tag{7}$$

where, $\mathbf{u}$ are the input voltage of the inverter, $\mathbf{h}$ are the system variables and $\mathbf{H}$ is the matrix of fixed parameters of the inverter.

$$\mathbf{u} = \begin{bmatrix} u_\alpha(k+1) \\ u_\beta(k+1) \end{bmatrix}$$

$$\mathbf{h} = \begin{bmatrix} i^*_\alpha(k+2) \\ i^*_\beta(k+2) \end{bmatrix} - \begin{bmatrix} i_\alpha(k+1) \\ i_\beta(k+1) \end{bmatrix} + \frac{T_s}{L}\begin{bmatrix} v_{c\alpha}(k+1) \\ v_{c\beta}(k+1) \end{bmatrix} \tag{8}$$

$$\mathbf{H} = -\frac{T_\mathrm{s}}{L}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}.$$

The optimization problem of the FCS-MPC can be formulated as:

$$\min_{u \in S} J(\mathbf{u}) \tag{9}$$

where $\mathbf{S} = \{\mathbf{u}^0, \mathbf{u}^1, \mathbf{u}^2, \mathbf{u}^3, \mathbf{u}^4, \mathbf{u}^5, \mathbf{u}^6\}$.

The inverter voltage vectors can be seen in Table 1. After selecting the optimal vector in $\alpha\beta$ coordinates the vector is converted back to abc coordinates.

TABLE 1. Inverter voltage vector.

Vector	Switching states in $\alpha\beta$	Switching states in abc
$\mathbf{u}^0$	$[0 \quad 0]^T$	$[0 \quad 0 \quad 0]^T$
$\mathbf{u}^1$	$\left[\sqrt{\frac{2}{3}} \quad 0\right]^T$	$[1 \quad 0 \quad 0]^T$
$\mathbf{u}^2$	$\left[\frac{1}{\sqrt{6}} \quad \frac{1}{\sqrt{2}}\right]^T$	$[1 \quad 1 \quad 0]^T$
$\mathbf{u}^3$	$\left[-\frac{1}{\sqrt{6}} \quad \frac{1}{\sqrt{2}}\right]^T$	$[0 \quad 1 \quad 0]^T$
$\mathbf{u}^4$	$\left[-\sqrt{\frac{2}{3}} \quad 0\right]^T$	$[0 \quad 1 \quad 1]^T$
$\mathbf{u}^5$	$\left[-\frac{1}{\sqrt{6}} \quad -\frac{1}{\sqrt{2}}\right]^T$	$[0 \quad 0 \quad 1]^T$
$\mathbf{u}^6$	$\left[\frac{1}{\sqrt{6}} \quad -\frac{1}{\sqrt{2}}\right]^T$	$[1 \quad 0 \quad 1]^T$
$\mathbf{u}^7$	$[0 \quad 0]^T$	$[1 \quad 1 \quad 1]^T$

C. Active and reactive power control

The inverter active and reactive powers will be controlled in the dq reference frame by two independent PI controllers [40], designed using the frequency-response method [40], [41]. In this method, it is necessary to convert the voltages and grid-side currents from $\alpha\beta$ to dq coordinates [42]. The variables on the d and q axes refer to active and reactive powers, respectively. This project was based on [33], [43]. Thus, two grid-side reference currents i_{gd} and i_{gq} will be generated and converted back to the $\alpha\beta$ coordinates for the FCS-MPC for current control. The PI gains kp_{dq} and ki_{dq} are calculated as:

$$kp_{dq} = \frac{\cos PM - 180^\circ}{b} \tag{10}$$

$$ki_{dq} = \omega_{bw} \cdot \sqrt{\frac{1 + 2bkp_{dq} - b^2 kp_{dq}^2}{b^2}} \tag{11}$$

Where the $\cos PM$ denotes the phase margin, $\omega_{\text{BW}} = 2\pi 10$ rad/s is the controller bandwidth, and b is the maximum magnitude of the voltage vector that the inverter can apply in the $\alpha\beta$ plane, calculated based on the RMS phase voltage calculated by $b = \frac{3}{2}220\sqrt{2}$.

The grid-side reference currents $i_{gd}(k)$ and $i_{gq}(k)$ are:

$$i_{gd}(k) = kp_{dq}e_d(k) + ki_{dq}T_s x_d(k) \tag{12}$$

$$i_{gq}(k) = -(kp_{dq}e_q(k) + ki_{dq}T_s x_q(k)) \tag{13}$$

Where e_d and e_q are the errors, ans x_d and x_q are the states of the PI controller. where $x_d(k) = e_d(k) + x_d(k-1)$ and $x_q(k) = e_q(k) + x_q(k-1)$.

After obtaining the grid-side current references in dq $\mathbf{i}_{gdq}$, the conversion to $\alpha\beta$ reference frame is performed according to the equation below, where the angle θ was obtained from the synchronization algorithm.

$$\begin{bmatrix} i_{g\alpha}(k) \\ i_{g\beta}(k) \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{gd}(k) \\ i_{gq}(k) \end{bmatrix} \tag{14}$$

The grid-side current reference is calculated by equation (14), as $\mathbf{i}g\alpha\beta(k)$ represents the current flowing through the inductor on the grid side. However, in this controller, the current flowing through the inductor on the inverter side, $\mathbf{i}\alpha\beta$, is controlled. The inverter-side current references can be found by compensating the reactive power of the filter capacitor.

$$i^*_\alpha(k) = i_{g\alpha}(k) - \omega C v_{c\beta}(k) \tag{15}$$

$$i^*_\beta(k) = ig_{g\beta}(k) + \omega C v_{c\alpha}(k) \tag{16}$$

The reference currents will be used in the cost function J calculated by (6) and $\omega = 2\pi f(k)$. The following equations present the reference values. These references are estimated at time step (k+2) to account for the transport delay. The estimations were performed using the phasor rotation matrix [44].

$$\begin{bmatrix} i^*_\alpha(k+1) \\ i^*_\beta(k+1) \end{bmatrix} = \begin{bmatrix} \cos(\omega T_s) & -\sin(\omega T_s) \\ \sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix} \begin{bmatrix} i^*_\alpha(k) \\ i^*_\beta(k) \end{bmatrix} \tag{17}$$

$$\begin{bmatrix} i^*_\alpha(k+2) \\ i^*_\beta(k+2) \end{bmatrix} = \begin{bmatrix} \cos(\omega T_s) & -\sin(\omega T_s) \\ \sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix} \begin{bmatrix} i^*_\alpha(k+1) \\ i^*_\beta(k+1) \end{bmatrix} \tag{18}$$

D. DC-link voltage control

In this section, the design of the DC-link voltage controller will be presented. In this loop, the voltage reference is provided by the MPPT, and the control variable is proportional to the energy rather than the voltage itself. The control will be performed by a PI controller [33], [40].

$$G(z) = \frac{2k_p(z^{-1}) + 2k_i T_s}{(z^{-1})^2 C_{in} + 2k_p T_s(z^{-1}) + 2k_i T_s^2} \tag{19}$$

The transfer function $G(z)$ is implemented in discrete-time, where k_p and k_i correspond to the proportional and integral gains and C_{in} corresponds to the DC bus capacitance. The proportional and integral gains are given by:

$$k_p = \omega_n C_{in} \qquad k_i = \frac{\omega_n^2 C_{in}}{2} \tag{20}$$

Where ω_n is the undamped natural frequency, given by $\omega_n = \omega_{BW}\sqrt{\sqrt{10} - 3}$ with ω_{BW} defined as $\omega_{BW} = 2\pi 3$ rad/s.

The DC bus voltage error can be calculated as:

$$e(k) = \|v^*_{dc}(k) - v_{dc}(k)\|^2 \tag{21}$$

where $v^*_{dc}(k)$ is the reference and $v_{dc}(k)$ is the voltage measured on the DC bus. The active power reference P^* generated by the PI is calculated by:

$$P^* = e(k)k_p + x(k)k_i T_S \tag{22}$$

where $x(k)$ corresponds to the current state of the PI controller, which is calculated by $x(k) = e(k) + x(k-1)$.

E. MPPT

The MPPT algorithm tracks the photovoltaic panel's maximum power point based on temperature and irradiance, accounting for the (VxI) and (PxV) nonlinearities. This work employs the perturb and observe method for its simplicity and effectiveness [45], [46].

The conventional perturb & observe algorithm adjusts the DC bus voltage in small steps and monitors the resulting power variation [45]. If power increases, the step direction is maintained; otherwise, it is reversed to track the maximum power point, as shown in Figure 2.

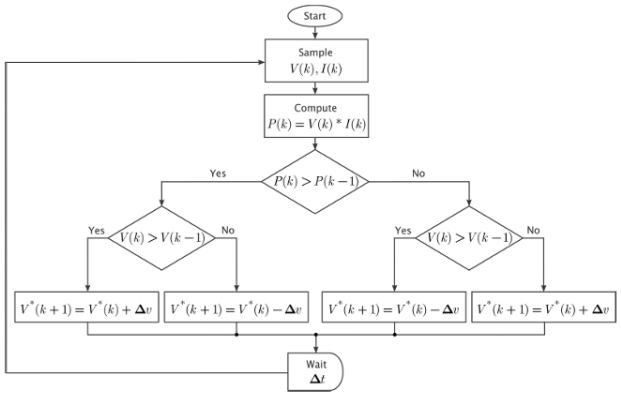

FIGURE 2. Perturb & Observe MPPT Algoritm. Adapted from [33].

III. TESTS FOR CONTROLLER VALIDATION

For the validation of the controllers and the grid connection functionalities in this case study, automated tests will be performed using a HIL platform. The INMETRO ordinance N° 140 [4] describes 26 test procedures that must be performed to guarantee the certification of the PV inverter. In this paper, the following tests will be considered:

- Phase change: In this test, the inverter must be able to withstand an out-of-phase automatic reconnection at the

AC ports. Two tests are performed, for 90° and 180° phase changes;
- Total Harmonic Distortion (THD) test: the test procedure evaluates the Total Harmonic Distortion (THD) at power levels of 10%, 20%, 30%, 50%, 75%, and 100% of the nominal power. The acceptance criterion requires that the THD remains below 5% when the inverter operates at power levels above 30% of the nominal power;
- Overfrequency disconnection level: The test requires the power injection to stop above 62.6 Hz;
- Overfrequency disconnection time: The test, mandating inverter shutdown within 10.2 s after the inverter reaches the overfrequency disconnection level;
- Underfrequency disconnection level value: The test, requiring power injection to stop above 57.4 Hz;
- Underfrequency disconnection time: The test, requiring inverter shutdown within 5.2 s after the inverter reaches the underfrequency disconnection level value;
- Overvoltage disconnection level: The test, which states that the grid voltage is raised in steps, where the approval criterion is that the inverter must not exceed a voltage 110% of the nominal value;
- Overvoltage disconnection time: The test, requiring inverter shutdown within 1.2 s after the inverter reaches the overvoltage disconnection level value;
- Undervoltage disconnection level: The test states that the grid voltage is raised in steps, where the aprroval criterion is that the inverter must not be less a voltage 80% of the nominal value;
- Undervoltage disconnection time: the test mandates inverter shutdown within 2.7 s after the inverter reaches the undervoltage disconnection level value.
- Fixed power factor test: The inverter is configured to operate with a power factor equal to 1.0 and 0.9 (inductive and capacitive). The power factor is measured in the power ranges described in the standard, with a tolerance of $\pm$ 0.025.
- Power factor curve test: The inverter is configured to generate an active power factor x curve, as shown in Figure 1 of [4]. As an approval criterion, the power factor must follow the behavior of Figure 1 [4] with a $\pm$ 0.025 tolerance.
- Reactive power injection and consumpion test: The inverter is configured to operate in resistive mode (Q = 0 Var), inductive mode (Q = 48.43%) and capacitive mode (Q = 48.43%), Q is equivalent to the reactive power of the inverter. To pass, the inverter must maintain the reactive power that was configured before the test.
- Active power variation test at overfrequency: During the test the inverter must behave according to the curve shown in Figure 2 of [4].
- Overfrequency and Underfrequency variation immunity test: The inverter must operate in the frequency bands shown in Figures 4 and 5 of [4].
- Overvoltage and Undervoltage variation immunity test: The inverter must operate in the frequency bands shown in Figures 6 and 7 of [4].

IV. AUTOMATIC TEST PROCEDURE

The automated HIL tests are performed in five main steps [30], [31], where the step-by-step procedure can be seen in Figure 4. The details on the operation of the automated tes platform is out of the scope of this paper. Detalied information on the platform can de found in [21], [30], [31]. The platform was created based on the Typhoon Hil Simulator [47]. The first step is to create the inverter schematic in Typhoon HIL Schematic Editor software [47], considering the topology and real inverter parameters. The inverter firmware was programmed in a C block within the schematic. The second step is to run a Python test routine that executes the step-by-step procedure of the test parameters specified in the previous subsections. The platform runs the inverter simulation in real time while performing the automatic tests.

The next part deals with the validation procedure. The Python routine controls each test step described in the standard, such as opening and closing switches, changing values in the real-time HIL simulation. These actions are performed in real-time while the HIL simulation is running. At the end of each test, the performance of the converter is analyzed to determine if it failed or passed the test. The last step is the automatic generation of the test report, showing the captured waveforms, the results of data post-processing, other relevant information, and, most importantly, whether the inverter passed or not the tests.

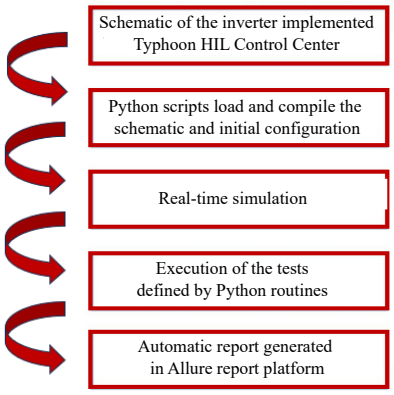

FIGURE 3. Test procedure flowchart. Adapted from [32].

V. HARDWARE-IN-THE-LOOP RESULTS

This section presents the results of the validation tests for the inverter considered in this case study. The schematic model is shown in Figure 1. The model was implemented

in a Typhoon HIL 402. The specifications and values of the model are shown in Table 2.

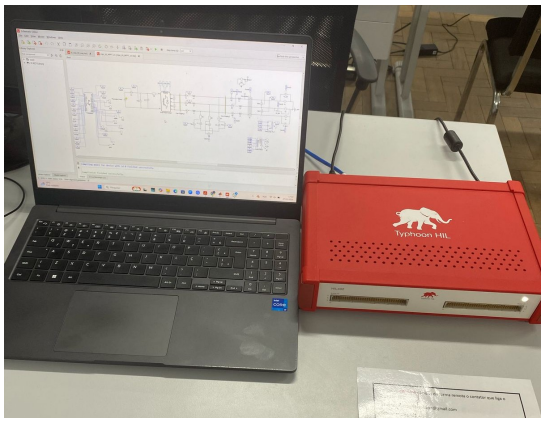

FIGURE 4. Hardware-in-the-Loop test bench.

TABLE 2. System parameters.

Parameter	Value
Nominal Active Power P_{nom}	100 kW
RMS grid voltage V_{grid}	220 V
Sampling time T_s	$50\mu s$
Dc bus voltage V_{DC}	800 V
Grid Frequency f	60 Hz
inverter-side filter inductance L	$1mH$
grid-side filter inductance L_g	$100\mu H$
Filter capacitance C	$200\mu F$
DC bus capacitance C_{in}	$20mF$

A. Phase change

The results of the phase change test are presented in Figures in 5 and 6 It is possible to conclude that the inverter passed this test, as it was able to perform automatic reconnection during the phase change and remain stable, both for 90° and 180°.

B. Total Harmonic Distortion test

The results of the Total Harmonic Distortion (THD) test are found in Table 3, where it is possible to observe the total THD percentage for different voltage values, showing that the total THD for the power levels 50%, 75% and 100% of the nominal power is below 5%.

TABLE 3. Total Harmonic Distortion (THD) for different EUT power levels

EUT Power (%)	Total THD (%)
50	3.46
75	2.21
100	1.70

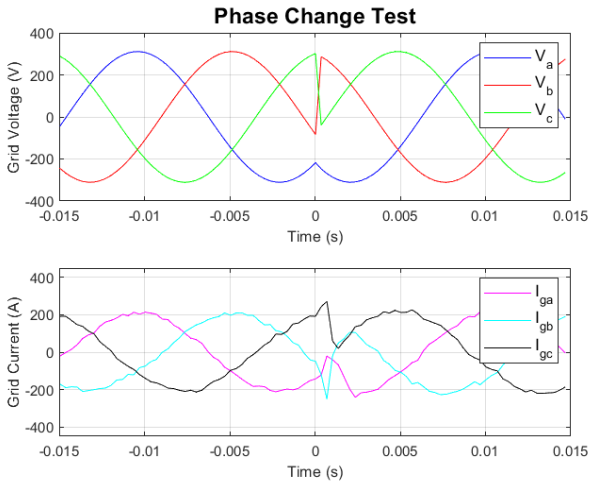

FIGURE 5. Test result for a phase change of 90°.

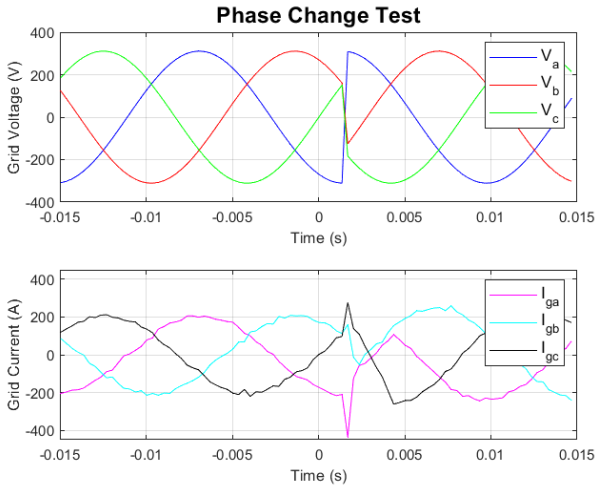

FIGURE 6. Test result for a phase change of 180°.

C. Overfrequency disconnection level

The results of the overfrequency disconnection level test are presented in Figure 7. The acceptance criterion states that the converter must stop supplying power at 62.6 Hz. The inverter successfully interrupts the power supply at 62.6 Hz, confirming that it passed the test.

D. Overfrequency disconnection time

The results of the overfrequency disconnection time test are presented in Figure 8. The acceptance criterion states that the converter must stop supplying power at 10.2 s. The inverter successfully interrupts the power supply at 0.39 s.

E. Underfrequency disconnection level

The results of the underfrequency disconnection level test are presented in Figure 9. The acceptance criterion states that the converter must stop supplying power at 57.4 Hz. The inverter successfully interrupts the power supply at 57.4 Hz.

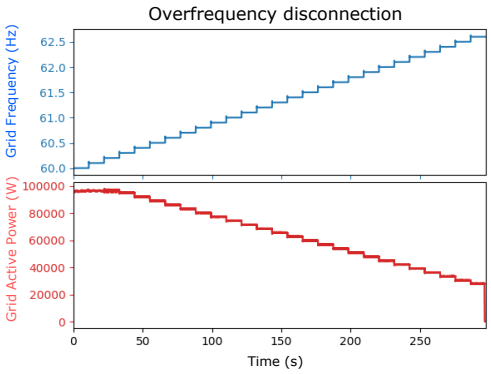

FIGURE 7. Interruption of power supply at maximum frequency.

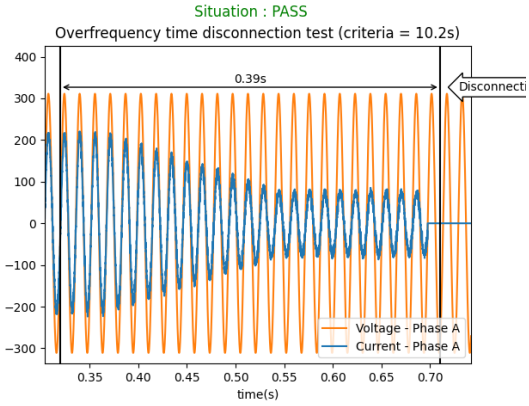

FIGURE 8. Interruption time at maximum frequency.

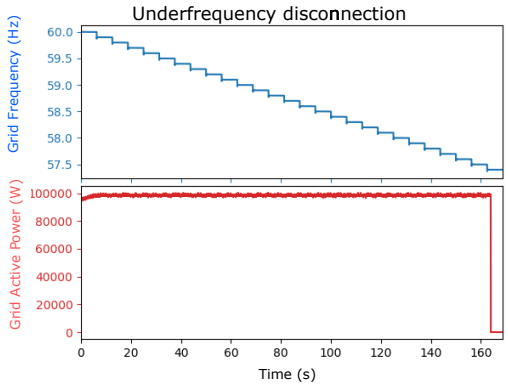

FIGURE 9. Interruption of power supply at minimum frequency.

F. Underfrequency disconnection time

The results of the underfrequency disconnection time test are presented in Figure 10. The acceptance criterion states that the converter must stop supplying power at 5.2 s. The inverter successfully interrupts the power supply at 0.39 s.

G. Overvoltage disconnection level

The results of the overvoltage disconnection level test are presented in Figure 11. The acceptance criterion states that

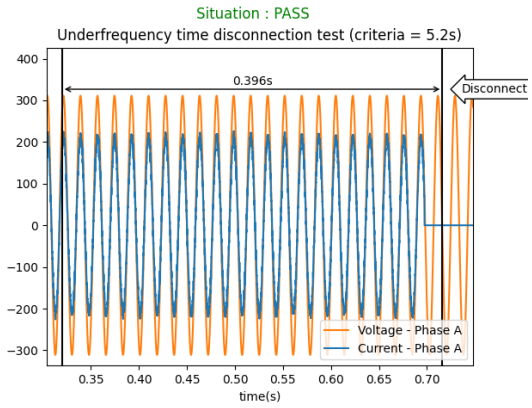

FIGURE 10. Interruption time at minimum frequency.

the converter must stop supplying power at 246.4 V. The inverter successfully interrupts the power supply at 246.4 V. The inverter was approved in this test.

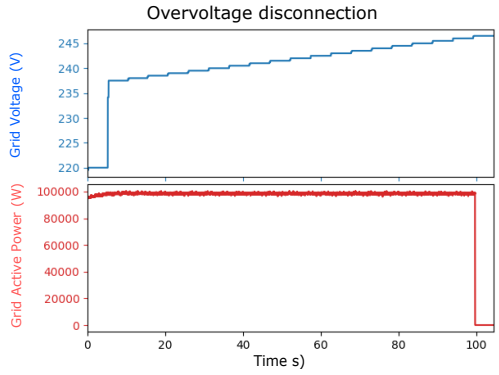

FIGURE 11. Interruption of power supply at maximum voltage.

H. Overvoltage disconnection time

The results of the overvoltage disconnection time test are presented in Figure 12. The acceptance criterion states that the converter must stop supplying power at 1.2 s. The inverter successfully interrupts the power supply at 1.009 s.

I. Undervoltage disconnection level

The results of the undervoltage disconnection level test are presented in Figure 13. The acceptance criterion states that the converter must stop supplying power at 176.0 V. The inverter successfully interrupts the power supply at 176.0 V.

J. Undervoltage disconnection time

The results of the undervoltage disconnection time test are presented in Figure 14. The acceptance criterion states that the converter must stop supplying power at 2.9 s. The inverter successfully interrupts the power supply at 2.508 s.

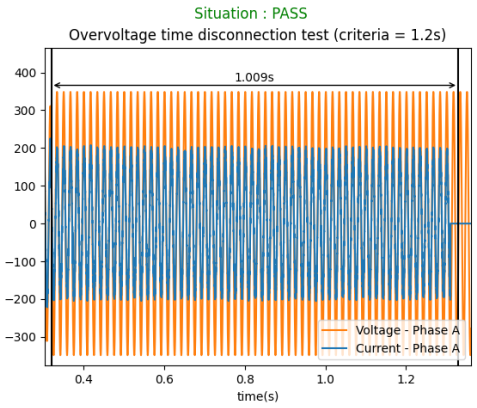

FIGURE 12. Interruption time at maximum voltage.

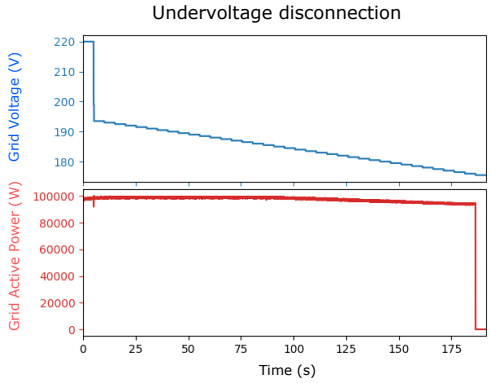

FIGURE 13. Interruption of power supply at minimum voltage.

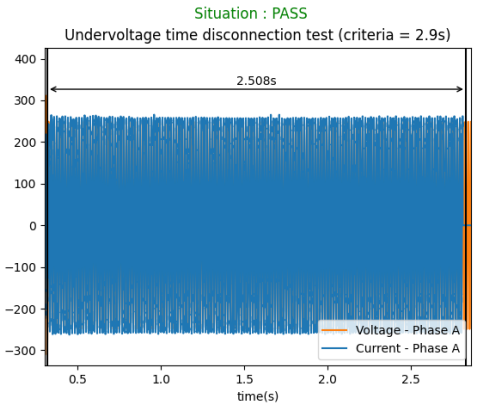

FIGURE 14. Interruption time at minimum voltage.

K. Fixed Power Factor Test

Table 4 presents the results of the fixed power factor test. Power levels at 10% and 20% of rated power were excluded, as per INMETRO Ordinance 140 [4]. From Table 4, it can be seen that the inverter operated at power factors of 1.0 and 0.9, within the 0.025 tolerance limit.

TABLE 4. Fixed power factor test.

EUT Power (%)	PF = 1.0	PF = 0.9	PF = -0.9
30	0.99	0.89	0.89
50	0.99	0.90	0.90
75	1.00	0.90	0.90
100	1.00	0.90	0.90

L. Power Factor Curve Test

Table 5 shows that the inverter met the requirements for power levels above 30%, but failed at 10% and 20% of rated power, where a power factor of 1.0 ± 0.025 is required.

The cause of this issue is that FCS-MPC has a higher current ripple compared to other control methodologies. A viable solution to this problem is to redesign the LCL filter to ensure proper filtering of harmonic components. In addition to redesigning the filter, another alternative would be to enhance the FCS-MPC by implementing a fixed switching frequency MPC, which provides better results results regarding the harmonic content injected into the power grid, as stated in [48]–[51].

TABLE 5. Power Factor Curve Test Results

EUT Power (%)	Measure PF
10	0.89
20	0.97
30	0.98
50	0.99
75	0.94
100	0.89

After redesigning the LCL filter, the values of the passive components are shown in Table 6. The inverter was again subjected to the power factor curve test and passed, meeting the regulatory requirements as demonstrated in Table 7.

TABLE 6. Redesigned LCL Filter Component Values.

Parameter	Value
L	2mH
L_g	$200\mu H$
C	$400\mu F$

TABLE 7. Power Factor Curve Test Results from the modified LCL filter.

EUT Power (%)	Measure PF
10	0.98
20	0.99
30	0.99
50	0.99
75	0.95
100	0.90

M. Reactive power consumption and injection test

The results of the power factor curve test are presented in Table 8. In this test, the power ranges equivalent to 10% and 20% of the rated power are not considered in all operations. The inverter passes the test in the power ranges equivalent to 50%, 75%, and 100% in capacitive and inductive operation. However, in all power ranges in resistive operation and at 30% in capacitive and inductive operations, the inverter does not pass the test. As mentioned in the previous section, a viable solution is to adjust the LCL filter, enabling the inverter to eliminate harmonic components.

TABLE 8. Injection and Consumption of Reactive Power Test Results

EUT Power (%)	Resistive	Capacitive	Inductive
30	17.20%	51.38%	51.38%
50	10.66%	49.61%	49.47%
75	7.10%	48.95%	48.92%
100	5.31%	48.75%	48.71%

After the redesign in the LCL filter shown in Table 6, there was a significant improvement in the results. However, the inverter failed in the power ranges of 30% and 50% of the rated power in resistive operation as shown in Table 9. Moreover, there was a significant improvement in the results of the THD test that can be shown in Table 10.

TABLE 9. Injection and Consumption of Reactive Power Test Results

EUT Power (%)	Resistive	Capacitive	Inductive
30	5.63%	48.72%	48.71%
50	3.30%	48.56%	48.53%
75	2.22%	48.5%	48.48%
100	1.70%	48.47%	48.46%

TABLE 10. Total Harmonic Distortion (THD) for Different EUT Power Levels from the modified LCL filter

EUT Power (%)	Total THD (%)
50	1.36
75	0.89
100	0.66

N. Active power variation test at overfrequency

Based on the result shown in Figure 15, it is noted that the inverter passed the test, as the power behaved according to the specification in Ordinance No. 140 of INMETRO [4].

O. Overfrequency and Underfrequency variation immunity test

The results of the overfrequency and underfrequency tests are presented in Figures 16 and 17. The standard requires that the inverter must remain connected to the grid and inject active power during the events specified in Figures 4 and 5 of [4]. It can be concluded that the inverter performed as expected during the frequency transients and passed the tests.

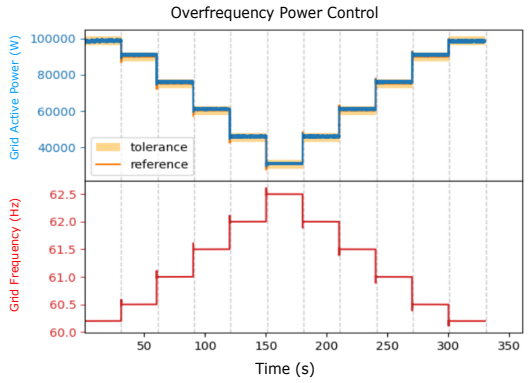

FIGURE 15. Overfrequency active power contro test.

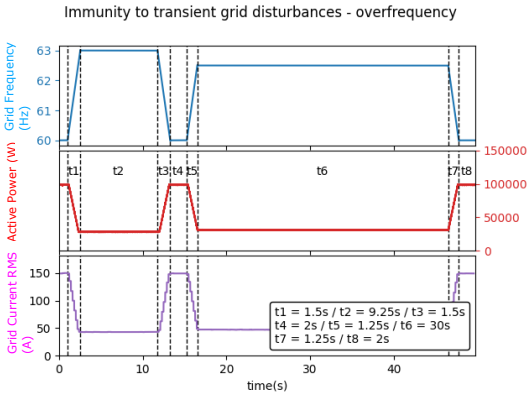

FIGURE 16. Overfrequency variation immunity test curve.

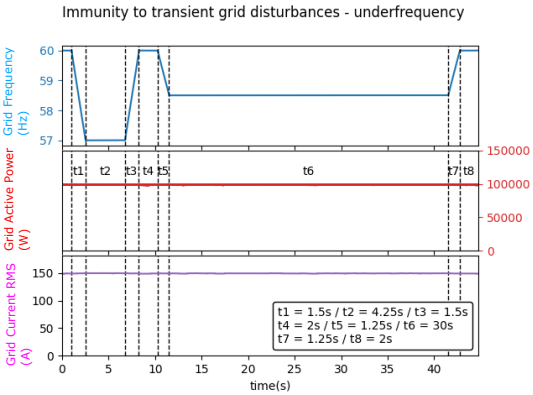

FIGURE 17. Underfrequency variation immunity test curve.

P. Overvoltage and Undervoltage variation immunity test

The results of the overvoltage and undervoltage tests are presented in Figures 18 and 19. The standard requires that the inverter remain connected to the grid and inject active power during the events specified in Figures 6 and 7 of [4]. Figure 18 shows that the inverter remained connected to the grid while operating under overvoltage conditions, from which it can be concluded that the inverter passed the test.

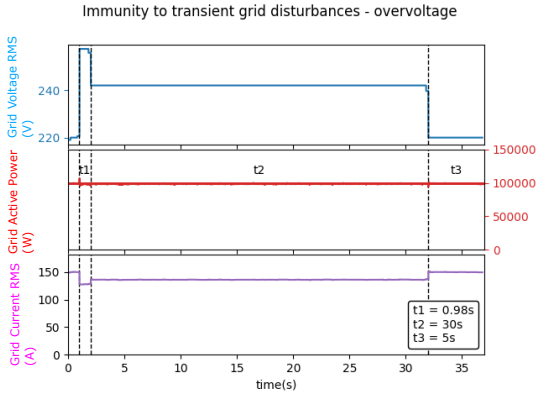

FIGURE 18. Overvoltage variation immunity test curve.

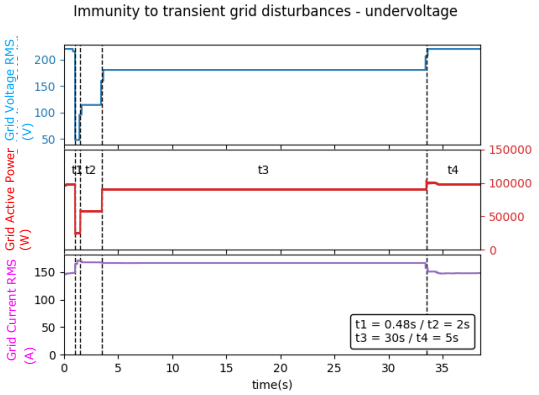

FIGURE 20. Undervoltage variation immunity test curve with the anti-windup.

However, during the undervoltage test, the inverter did not remain connected, as shown in Figure 19, and thus failed the test. The cause of the inverter failure in this test is the saturation of the control action of the DC bus control. This problem occurs in situations where the active power decreases and the DC bus voltage increases, contributing to the increase in the quadratic error.

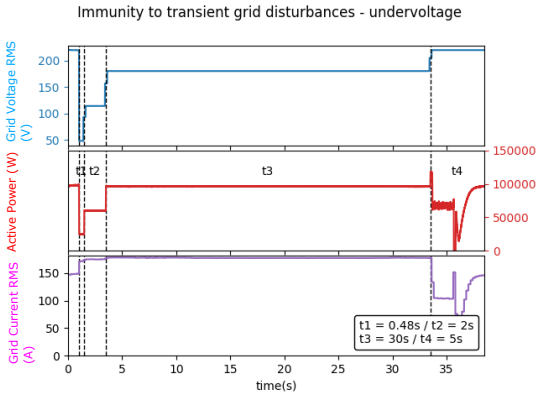

FIGURE 19. Undervoltage variation immunity test curve.

To solve the problem of control action saturation, an anti-windup functionality was implemented, which is presented by $A_p = -(P_{ref} - P^*) \cdot k_{atw}$.

Where $k_{atw} = 0.8$ is the empirically adjusted anti-windup gain, A_p is the calculated anti-windup control action, P^* is the active power reference without limitation given in (22), and P_{ref} is the power reference with a maximum value of 100 kW.

$$x(k+1) = (e(k) + A_p) \cdot T_s + x(k) \tag{23}$$

Equation (23) presents the future state of the PI $x(k+1)$, considering the anti-windup variable. It can be noted that the equation has been modified compared to what was presented in Section C. At the end of the algorithm, the current state of the PI is updated to $x(k) = x(k+1)$.

As shown in Figure 20, the implementation of the anti-windup functionality enabled the inverter to pass the undervoltage immunity test. Thus, automated HIL tests provide a means for rapidly validating firmware and applying necessary adjustments to ensure proper inverter performance.

VI. CONCLUSION AND FUTURE WORKS

This paper demonstrated the contribution that automated HIL testing offers a reliable and effective means of validating converter firmware before proceeding to hardware-level inverter tests. The system considered for the case study underwent 18 compliance tests with Brazilian standards [2]–[4], initially passing 15. After the redesign of the LCL filter and the implementation of the anti-windup functionality, the inverter passed 17 tests. Automated HIL tests proved to be an effective tool for identifying and correcting firmware errors.

Another interesting advantage of automated HIL tests is the ability to validate the firmware of medium-power systems, which would be extremely difficult in real laboratories. Automated HIL testing serves as a tool that allows quick validation of firmware, enabling necessary adjustments based on the results to achieve proper inverter operation. The FCS-MPC with grid-connected functionalities was implemented and showed good performance, especially in transient response tests. For future work, implementing a fixed-frequency FCS-MPC controller would be interesting to test and analyze its performance. Another relevant topic would be subjecting the inverter to new automated tests specified in [2]–[4], such as anti-islanding, flicker, reconnection tests, and frequency power control.

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AUTHOR'S CONTRIBUTIONS

J.V.L.ROSA: Data Curation, Formal Analysis, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **L.F.R.MENEGAZZO:** Data Curation, Su-

pervision, Validation. **L.V.BELINASO:** Formal Analysis, Writing – Review & Editing. **F.M.CARNIELUTTI:** Conceptualization, Methodology, Project Administration, Resources, Software, Supervision, Writing – Review & Editing. **H.PINHEIRO:** Resources, Software, Supervision, Visualization, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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