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Study and Design of a Non-Isolated Bidirectional DC-DC Converter Based on a Switched Inductor and Voltage Multiplier Cell for Renewable Energy Applications

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ABSTRACT In this paper, a bidirectional converter with low voltage stress is evaluated. The converter is based on a switched inductor technique combined with a switched capacitor in a voltage multiplier structure, enabling a higher voltage gain while maintaining reduced stress on the switching components. Both dynamic and static modeling are developed to provide a comprehensive understanding of the converter behavior and a control strategy is proposed to ensure stable operation under varying load and input conditions. To validate the theoretical analyses, a hardware prototype was designed and implemented, operating at 80-500 W with an input to output voltage range of 72-400 V. Experimental tests were conducted under different operating conditions, confirming the effectiveness of the proposed converter. A peak efficiency of 98.4% was achieved at 250 W, demonstrating the high performance of the converter. Additionally, the ability to reverse power flow online without requiring shutdown enhances its applicability in renewable energy systems and energy storage interfaces.

KEYWORDS bidirectional DC-DC converter, non-isolated, switched inductor, voltage multiplier

I. INTRODUCTION

With the excessive use of fossil fuels and the intensification of the greenhouse effect, developed countries have increasingly engaged in discussions regarding the ban on the manufacturing of vehicles based on internal combustion engine in the next decades [1-3]. In response, there has been an interest for renewable energy solutions, such as solar, wind, and fuel cell technologies [4-6]. These alternatives are being integrated into various energy systems, including microgrids, hybrid electric vehicles, uninterruptible power supplies (UPS) and battery chargers [7-9]. Such applications share a high-voltage bus (V_H) and a low-voltage bus (V_L) with different level of voltage. Therefore, a bidirectional converter is required to interconnect the buses, thereby facilitating the bidirectional power flow.

A variety of converter topologies have been explored in the literature to meet the diverse requirements of these kind of systems. The standard structures [10-13] are the simplest, with fewer components and operational simplicity. However, they cannot achieve the high voltage gains required for renewable energy applications. Based on standard structures, some multilevel bidirectional converters have been developed [14-15], but, in general, maintain the same static gain as the standard topologies from which they were derived. Nevertheless, they improve system efficiency by distributing losses in a more effectively way across their components and, consequently, achieve relatively higher voltage gains compared to standard topologies.

Another possible approach to increasing voltage gain is the use of a cascaded converter system [16-17], which results in a quadratic input-to-output gain relationship. Nonetheless, this configuration doubles the number of semiconductors and capacitors required for each additional stage, leading to a relatively high implementation cost.

To maintain a relatively low number of devices while achieving high voltage gain, converters based on coupled inductors [18-19] have been developed. This technique relies on a magnetic circuit capable of storing energy in the secondary side through the switching of the primary side. The voltage gain is determined by the turns ratio between the primary and secondary windings of the magnetic element, allowing for either high or low gain. However, this approach is typically associated with high current and voltage stress on the semiconductor devices.

To mitigate both current and voltage stresses on semiconductor devices, a switched-inductor [20] approach can be employed. Due to its parallel-input configuration, this technique magnetizes two or more inductors in parallel and demagnetizes them in series. On the other hand, the voltage gain of this approach remains close to the necessary limit

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when compared to the stringent requirements of renewable energy applications.

So, to improve the voltage gain and stresses in the switches devices, the switched-capacitor techniques have been used in the last years. Switched-capacitor circuits operate by periodically reconfiguring capacitors, alternating between parallel and series connections, in order to transfer energy between different voltage levels [21-22]. A particular kind of switched capacitor is the voltage multiplier cell, which has two capacitors that can be charged in parallel with the inductors and discharged in series with the output capacitor [23-26]. The main advantage of this approach is the high voltage gain, low voltage stresses and low values of inductances.

In this sense, this paper introduces a non-isolated bidirectional DC-DC converter design that offers high voltage gain while minimizing component stress, complexity, and cost. The proposed converter can be seen in the Fig. 1 and combines elements from the switched inductor with voltage multiplier cell, keeping a simplified approach that results in a more efficient and reliable system. It is composed of five switches (S_{in1}, S_{in2}, S_{out1}, S_{out2} and S_{out3}), two inductors (L_1 and L_2), and four capacitors (C_L, C_1, C_2 and C_4), enabling step-up and step-down operations with reduced current ripple. Since the grounding of all switches is distinct, dedicated isolated gate drivers for each switch must be used. Since there is no common grounding between input and output, the impact of electromagnetic interference (EMI) is minimal since the operating power is 500 W and the switching frequency is low. However, if this presents a problem, any residual EMI is effectively mitigated using common-mode chokes, Y-capacitors, and/or shielded inducers [27].

The structure of the paper is as follows: Section II and III describe the operational principles, including both step-up/step-down modes in continuous conduction mode (CCM), voltage gains, and stresses. Section IV presents the analysis of the input current waveform ripple. Section V outlines the design guidelines, while Section VI details the modeling and control system of the proposed converter. In Section VII, the methodology for estimating the overall efficiency of the converter is presented, while Section VIII provides a comparison among converters with similar technologies. Finally, Sections IX and X present the experimental results and the main conclusions, respectively.

II. STEP-UP OPERATION

To explain the operation of the proposed converter during a single switching cycle, the following assumptions are considered: in both step-up/step-down operations, the converter works in continuous conduction mode (CCM); all components are ideal; the capacitors are sufficiently large, allowing voltage to be treated as constant; and the components shaded in gray are off.

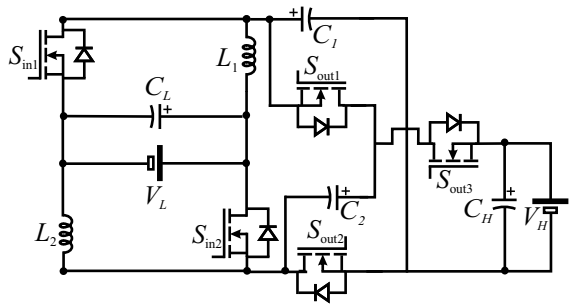

FIGURE 1. Proposed converter.

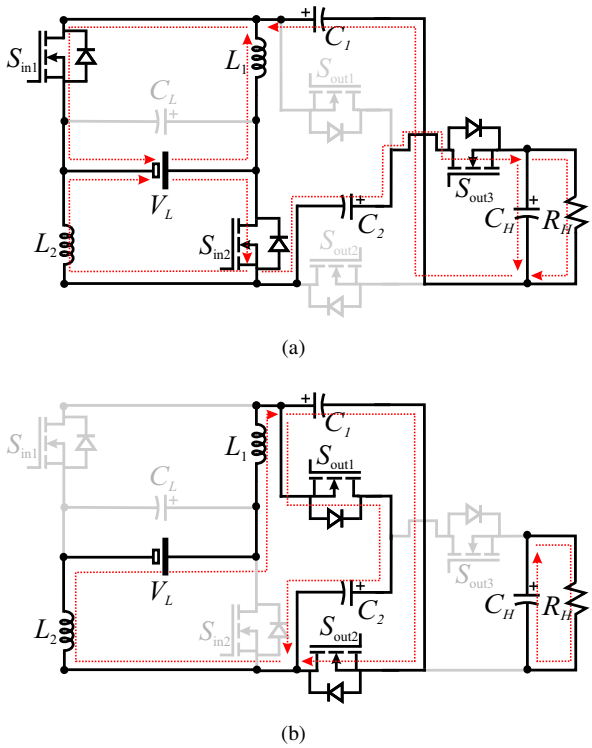

FIGURE 2. Topological stages for step-up operation. (a) Stage I. (b) Stage II.

In step-up mode, switches S_{in1}, S_{in2} act as active switches, while S_{out1}, S_{out2} and S_{out3} function as synchronous rectifier, besides that, D_H is used to represent the step-up duty cicle. The stages of operation can be seen in Fig. 2, while the main theoretical waveforms are shown in Fig. 3(a)

Stage I [Fig. 2(a), $t_o - t_1$]: During this stage, switches S_{in1}, S_{in2} and S_{out3} are active (ON), while S_{out1} and S_{out2} are inactive (OFF). Inductors L_1 and L_2 are magnetizing by the input voltage V_L, and the current through the inductors can be described as:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_L}{L_i}t + I_L(t_0), \tag{1}$$

where $L_i = L_1 = L_2$.

Stage II [Fig. 2(b), $t_1 - T_s$]: In this phase, switches S_{in1}, S_{in2} and S_{out3} are deactivated (OFF), while S_{out1} and S_{out2} are turned (ON). The inductors L_1 and L_2 demagnetizing by

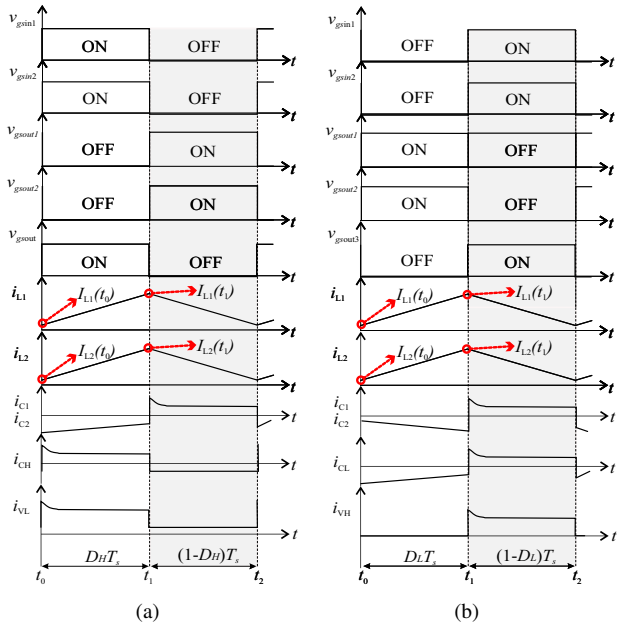

FIGURE 3. The main waveforms for (a) step-up and (b) step-down.

rate of $V_L - V_{Ci}$, and the current in the inductors is given by:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_L - V_{C_i}}{L_1 + L_2} t + I_L(t_1). \tag{2}$$

where $V_{C_i} = V_{C_1} = V_{C_2}$.

A. Step-Up Voltage Gain Calculation

The voltage gain must be calculated in two steps. First, it must be considered that the inductors demagnetize through the capacitors C_1 and C_2 of the voltage multiplier, thus the voltage gain must initially be applied to these capacitors.

By applying the volt-second balance principle to the inductors (L_1 and L_2), the voltage gain can be derived as shown below:

$$\int_0^{D_H Ts} V_L dt + \int_{D_H Ts}^{Ts} V_L - V_{C_1} dt = 0. \tag{3}$$

Based on the operational stages, the voltage gain is expressed as:

$$\frac{V_{C_1}}{V_L} = \frac{V_{C_2}}{V_L} = \frac{1 + D_H}{1 - D_H}. \tag{4}$$

In the second stage of calculating the voltage gain, it must be considered that the capacitors C_1, C_2 and the voltage source V_L are aligned in series and discharged in the capacitor C_H. Thus, the voltage gain presented in Eq. (4) is multiplied and applied to the high-voltage capacitor, as follows:

$$\frac{V_H}{V_L} = 1 + \frac{2 + 2D_H}{1 - D_H}. \tag{5}$$

B. Voltage and Current Stress on Semiconductors

The voltage across the switches S_{in1} and S_{in2} can be described in the second stage of operation, as follows:

$$V_{S_i} = \frac{V_L + V_{C_1}}{2} = \frac{V_L}{1 - D_H} \tag{6}$$

The voltage across the switches S_{out1}, S_{out2} and S_{out3} can be defined as:

$$V_{S_i} = V_H - V_{C1} = \frac{2V_L}{1 - D_H} \tag{7}$$

The current stress on switches S_{in1} and S_{in2} are given by:

$$I_{S(rms)} = I_L \sqrt{D_H}. \tag{8}$$

In relation to the switches S_{out1} and S_{out2}, their current stress are given by:

$$I_{S(rms)} = I_L \sqrt{1 - D_H}. \tag{9}$$

Following the methodology described in 30, the current through the switch S_{out3} can be approximated by a trapezoidal waveform. Accordingly, its RMS current can be expressed as:

$$I_{S(rms)} = \frac{I_1^2 + I_1 I_2 + I_2^2}{3} \tag{10}$$

where:

$$I_1 = \frac{V_L + 2V_{C1} + \Delta_{VC1} - V_H + \frac{\Delta_{VH}}{2}}{3R_{DS}} \tag{11}$$

$$I_2 = \frac{V_L + 2V_{C1} - \Delta_{VC1} - V_H - \frac{\Delta_{VH}}{2}}{3R_{DS}} \tag{12}$$

III. STEP DOWN OPERATION

In step-down mode, switches S_{in1} and S_{in2} act as synchronous rectifiers, while S_{out1}, S_{out2} S_{out3} function active switch, besides that, D_L is used to represent the step-up duty cicle.

The stages of operation can be seen in Fig. 4, while the main theoretical waveforms are shown in Fig. 3(b).

Stage I [Fig. 4(a), $t_0 - t_1$]: In this phase, switches S_{in1}, S_{in2} and S_{out3} are turned OFF, while S_{out1} and S_{out2} are ON. The inductors L_1 and L_2 are magnetizing, as described:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_{C_i} - V_L}{L_1 + L_2} t + I_L(t_o). \tag{13}$$

where $C_i = C_1 = C_2$.

Stage II [Fig. 4(b), $t_1 - t_2$]: At this stage, switches S_{in1}, S_{in2} and S_{out3} are turned ON, while S_{out1} and S_{out2} are OFF. The inductors L_1 and L_2 are demagnetizing and their currents are expressed as:

$$\mathrm{i}_{L1}(t) = i_{L2}(t) = \frac{V_L}{L_i} t - I_L(t_1), \tag{14}$$ where $L_i = L_1 = L_2$.

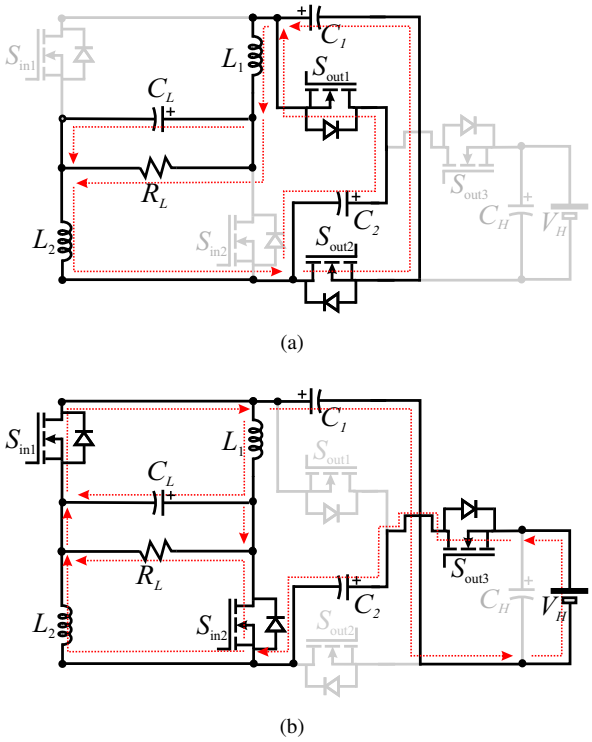

FIGURE 4. Topological stages for step-down operation. (a) Stage I. (b) Stage II.

A. Step-Down Voltage Gain Calculation

Since in step-down mode the power supply V_H is fixed, each capacitor in the voltage multiplier must receive half of the high-voltage bus, as characterized:

$$\frac{V_{C_1}}{V_L} = \frac{V_{C_2}}{V_L} = \frac{D_L}{2 - D_L} \tag{15}$$

To find the voltage gain in step-down mode, the volt-second balance, which was presented in Eq. 3,must be taken into account. Thus, the static voltage gain is resolved and found in Eq. 16.

$$\frac{V_L}{V_H} = -\frac{4}{D_L - 4} - 1 \tag{16}$$

IV. INPUT CURRENT RIPPLE OF THE PROPOSED CONVERTER

The input current at low voltage side (i_{VL}) proposed converter can be seen in Fig. 3. This current is the sum of the switched inductor cell and switched capacitor currents. In the first stage of converter operation, this current can be described as:

$$i_L(t) = i_{L_1}(t) + i_{L_2}(t) + i_{C_1}(t) + i_{C_2}(t) \tag{17}$$

While in the second stage of operation, this current is given by:

$$i_L(t) = i_{L_1}(t) \tag{18}$$

where:

$$i_L(t) = i_{L_1}(t) = i_{L_2}(t) = i_{C_1}(t) = i_{C_2}(t) \tag{19}$$

Knowing the operation operation stage, the input current ripple at low voltage side (iVL) can be rewritten as:

$$\Delta I_{VL} = \frac{2V_L D_H T_s}{L} + 2I_{C(\max)} \tag{20}$$

where $L = L_1 + L_2$, $IC_{(max)}$ is the peak current of capacitor C_1 and C_2. The behavior of this waveform can be seen in Fig. 3. Note that the sum of the switched inductor and switched capacitor cell currents causes a high ripple current. Therefore, the capacitor CL was included in the converter.

V. DESIGN GUIDELINES

A. Inductors

The inductors are designed based on the current ripple criterion. Since both inductors have the same inductance value, designing one will suffice. The voltage across the inductor during the active portion of the duty cycle in step-up operation is:

$$V_{L1} = L\frac{d_{I_{L1}}}{dt} = L\frac{\Delta_{I_{L1}}}{\Delta t} = V_L. \tag{21}$$

The Δt corresponds to the active phase of the duty cycle,

$$L\frac{\Delta_{I_{L1}}}{DT_s} = V_L. \tag{22}$$

Solving to find the inductance value as a function of the desired current ripple:

$$L_1 = L_2 = \frac{V_L D_H T_s}{\Delta_{I_{L1}}} = \frac{V_L D_H}{\Delta_{I_{L1}} f_s}. \tag{23}$$

B. Capacitors

The equation for the capacitor C_H can be derived from the second stage of operation in step-up mode, during which the capacitor is discharging, based on the concept of charge stored in the capacitor, as expressed in Eq. (24).

$$Q_H = C_H V_H \tag{24}$$

By regrouping the terms in (24) and adapting for ΔV_H, Eq. (25) is obtained.

$$\Delta Q_H = C_H \Delta V_H = \frac{V_H(1 - D_H)T_S}{R_H} \tag{25}$$

By reorganizing the terms in (25) and applying (5) in V_H, the value of the capacitor C_H is obtained in Eq. (26).

$$C_H = \frac{D_H + 3}{\Delta V_H R_H F_S} \tag{26}$$

To determine C_L, it is necessary to evaluate the current variation through the capacitor during the first stage of operation. This variation corresponds to the current variation of the inductor during the same period, as expressed in Eq. (27).

$$\Delta I_{L1} = D_L T_s \frac{V_{C1} - V_L}{2L_1} \tag{27}$$

Knowing that the voltage variation across the capacitor depends on the instantaneous current through it, Eq. (29) is obtained.

$$C\frac{dV_C}{dt} = D_L T_s \frac{V_{C1} - V_L}{2L_1} \tag{28}$$

By rearranging the terms, the mathematical expression for the capacitance C_L is obtained in Eq. (29).

$$C_L = \frac{(V_{C1} - V_L)(D_L T_S)^2}{2L_1 \Delta V_L} \tag{29}$$

VI. MODELING AND CONTROL SYSTEM

A. Dynamic Model

To guarantee that the converter operates effectively in the specified applications, this section will present the modeling and control of the proposed converter. In converters that use switched capacitors, the dynamic model can be simplified by eliminating the voltage-multiplier cell and considering it as a gain with dynamics adjusted by its equivalent capacitances and resistances, this technique is widely used and has been shown to preserve the original converter dynamic characteristics [28-29]. In this sense, aiming to simplify the order of the model without losing accuracy, the state-space model is presented in Eq. (30).

$$\begin{bmatrix} \dot{v}_H \\ \dot{i}_{L1} \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{eq}C_{eq}} & -\frac{D_H - 1}{C_{eq}} \\ \frac{D_H - 1}{2L_1} & 0 \end{bmatrix} \begin{bmatrix} v_H \\ i_{L1} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{D_H + 1}{2L_1} \end{bmatrix} V_L \tag{30}$$

The equivalent capacitance (C_{eq}) regulares the oscillation/resonance frequency, while the equivalent resistance (R_{eq}) determines the damping of the system. These parameters can be adjusted in simulation by comparing the system response with the converter response [29] and are used exclusively for tuning the dynamic model, with no regard to the order of magnitude of their values. The process begins with the building of state-space equations in simulation software, enabling comparison with the response of the converter. The inductance value of the model can be kept equal to that of the converter. In contrast, the capacitance (C_{eq}) and resistance (R_{eq}) values may initially be assigned arbitrarily. During the iterative procedure, C_{eq} is adjusted until the frequency of the model response matches that of the converter. From this point onward, R_{eq} is varied so that the damping of the model corresponds to the damping of the converter. Once both parameters are aligned, the model is considered to be properly tuned to the converter response.

To better demonstrate the effectiveness of the technique, Fig. 5 shows a comparison between the obtained model and the simulated converter. It is notable, therefore, that the time response of both the model and the converter overlap, thus demonstrating the model effectiveness. Additionally, the Fast Fourier Transform (FFT) is shown, elucidating that the oscillation frequencies and gains of the model and the converter are converging to the same point. The parameters used for this demonstration are presented in Table 1.

Since the state-space technique exhibits nonlinear characteristics, a linearization process is necessary to obtain linear transfer functions. This process, referred to as perturb and linearize. [30-31], involves expressing each state-space variable $x(t)$ as a sum of static components (X, U, and D) with a small time-variant disturbance ($\hat{x}(t)$, $\hat{u}(t)$, and $\hat{d}(t)$), as shown in Eq. (31-33). After this perturb and linearize

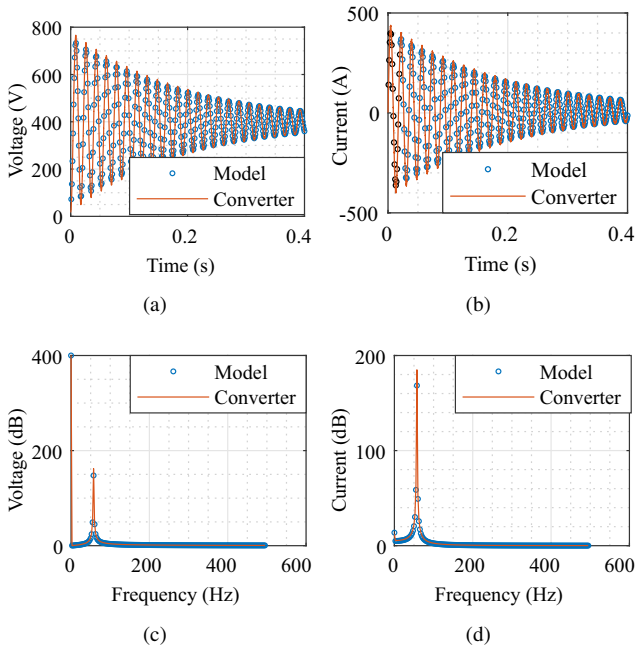

FIGURE 5. Model validation from (a) Time response of V_H voltage. (b) Time response of inductor current. (c) FFT of inductor current. (d) FFT of V_H voltage.

procedure, the nonlinear terms can be neglected, and the Laplace transform is applied to obtain the linear transfer functions.

$$x(t) = X + \hat{x}(t) \tag{31}$$

$$u(t) = U + \hat{u}(t) \tag{32}$$

$$d(t) = D + \hat{d}(t) \tag{33}$$

The transfer functions of high-side voltage by duty cycle and of inductor current by duty cycle are given by:

$$\frac{\hat{v}_H(s)}{\hat{d}(s)} = \frac{2\lambda\left(\beta - 2\alpha\beta - \gamma s + \alpha^2\beta - \alpha\gamma s\right)}{(\alpha-1)^2\left(\beta\alpha^2 - 2\beta\alpha + 2\theta\gamma\beta s^2 + 2\gamma s + \beta\right)} \tag{34}$$

$$\frac{\hat{i}_{L1}(s)}{\hat{d}(s)} = \frac{\lambda\left(\alpha + 2\theta\beta s + 3\right)}{(\alpha-1)^2\left(\beta\alpha^2 - 2\beta\alpha + 2\theta\gamma\beta s^2 + 2\gamma s + \beta\right)} \tag{35}$$

where: $\alpha = D_H$, $\beta = R_{eq}$, $\theta = C_{eq}$, $\gamma = L_1$, $\lambda = V_L$.

In Eq. (34), it is possible to identify the presence of a non-minimum phase zero, positioned as expressed in Eq. (36). It is noteworthy that the location of this zero depends on the relationship between R_{eq} and L_1, since these parameters can be more flexibly adjusted, whereas D_H is directly related to the converter's operating point, thus limiting its variation. Furthermore, this zero will always be located in the right half-plane, given that the denominator invariably yields a negative value. Regarding the numerator, its sign depends on D_H. However, it is always non-positive (strictly negative

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TABLE 1. Parameters.

Parameter	Value
Output Power	80-500 W
High Side Voltage V_H	400V
Low Side Voltage V_L	72 V
Switching frequency F_s	50 kHz
Proposed Converter Inductor L_1 and L_2	270 μH (597700 Magnetics 0.4 Ω)
Proposed Converter Capacitor C_L, C_H, C_1 and C_2	470 μF (EPCOS B43503-S5477)
Semiconductor devices	NTHL060N065SC1 (EliteSiC, 44 mohm, 650 V)
Equivalent resistance of the dynamic model R_{eq}	35 Ω
Equivalent capacitance of the dynamic model C_{eq}	2.82 mF

for $D_H \neq 1$). Consequently, the sign configuration ensures that the zero remains positive, thereby characterizing a non-minimum phase behavior.

$$Z_0 = \frac{R_{eq}(2D_H - D_H^2 - 1)}{L_1(-D_H - 1)} \tag{36}$$

B. Control System Design

The control strategy of the system is illustrated in Fig. 6. Both compensators are PI (Proportional-Integral) controllers, where the high-voltage side voltage V_H and the current through inductor L_1 are monitored and regulated. Thus, the proposed control enables operation in step-up and step-down modes. The dual-loop control system enhances the stability and reliability of the system, especially when energy is regenerated on the V_H side and power flow changes occur.

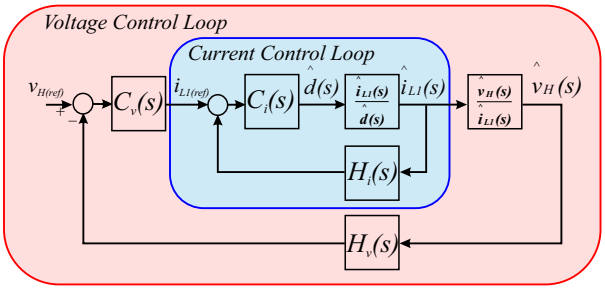


FIGURE 6. Control system.

The proportional-integral (PI) controller was designed using MATLAB Sisotool and Bode diagram analysis. The PI controllers are given by:

$$C_v(s) = \frac{1109(5.7 \times 10^{-3}s + 1)}{s} \tag{37}$$

$$C_i(s) = \frac{104.3(3.18 \times 10^{-4}s + 1)}{s} \tag{38}$$

Fig. 7 shows the Bode diagram of the uncompensated and compensated systems for voltage V_H. By applying the PI controller, the compensated system achieves a phase margin of 70° at 75 Hz. A phase margin of 70° was adopted as an appropriate value to ensure that, even if a sensor introduces some angular lag, the controller can continue to operate reliably, thus maintaining system robustness. The crossover frequency of 75 Hz was selected to provide a fast dynamic response and to function as a low-pass filter, with a cutoff frequency approximately two decades below the switching frequency (50 kHz), thereby preventing possible interference from switching signals.The PI controller attains the desired outcomes, as demonstrated in the experimental results section.

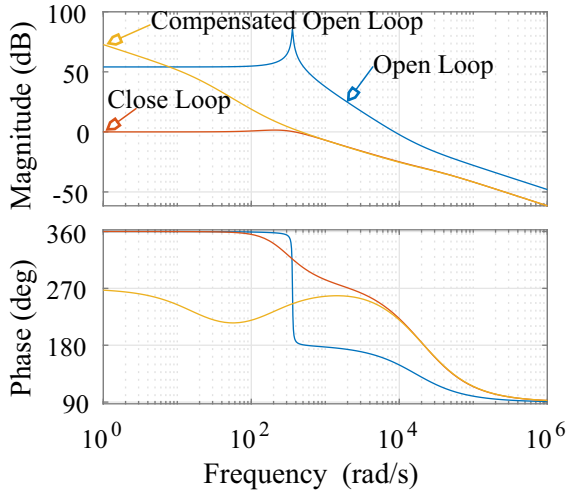


FIGURE 7. Bode plot from V_H.

VII. ESTIMATED EFFICIENCY

The methodology employed to calculate the efficiency and the distribution of losses is outlined in [30], and it involves using a mathematical model to derive the power losses in the components. Moreover, the parameters employed for the estimation are presented in Table I and the nominal power was used to estimate the power losses.

The semiconductor devices use SiC technology, which exhibit negligible losses related to the reverse recovery of intrinsic diodes. Therefore, this type of loss was disregarded in the estimated loss calculations. So, the switches experience two types of losses: resistive and switching losses. The resistive losses are calculated using the parasitic ON resistance ($R_{DS}(on)$), while the switching losses are dependent on the rise (t_{on}) and fall (t_{off}) times. The full derivation of the power losses from the switches is presented in Eq. (39).

$$P_S = \underbrace{I_{S(RMS)}^2 R_{DS(on)}}_{Resistive} + \underbrace{0.5F_s V_{DS} I_S(t_{on} + t_{off})}_{Switching} \tag{39}$$

where V_{DS}, $I_{S(RMS)}$, $R_{DS(on)}$, t_{on}, and t_{off} represent the voltage across the switches, the RMS value of the current through the switch, the resistance between drain and source, the turn-on time, and the turn-off time, respectively, all of which can be found in the MOSFET datasheet.

The inductors exhibit resistive and magnetic losses, which are described in Eq. 40.

$$P_L = \underbrace{r_L I_{L(rms)}{}^2}_{Resistive} + \underbrace{\left(aB_{pk}{}^b f_s{}^c\right) A_e l_e}_{Magnetic} \tag{40}$$

where $I_{L(rms)}$ is the RMS current of the inductor; r_L is the copper resistance; B_{pk} is the magnetic flux density of the magnetic core; a, b, and c are constants obtained from the curve fitting of the core; l_e is the core's medium path length (MPL), and A_e is the core sectional area, provided in the core datasheet.

Capacitors experience only resistive losses, as shown in Eq. 41.

$$P_C = I_{C(rms)} ESR \tag{41}$$

where ESR is the equivalent series resistance of the capacitors, and $I_{C(rms)}$ is the RMS value of the current passing through the capacitor.

The efficiency (η) of the converter is determined as follows:

$$\eta = \frac{P_{output}}{P_{losses} + P_{output}} \tag{42}$$

where P_{losses} is the total power loss in the components, and P_{output} is the nominal output power.

Therefore, applying the presented methodology, a theoretical result of 96.35% was obtained, with the theoretical distribution of losses illustrated in Fig. 8.

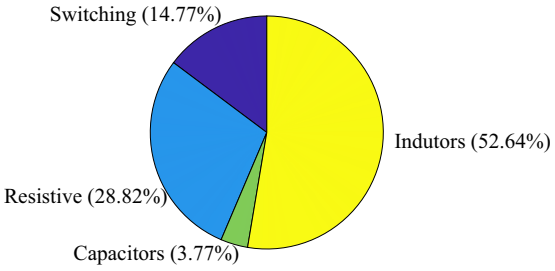
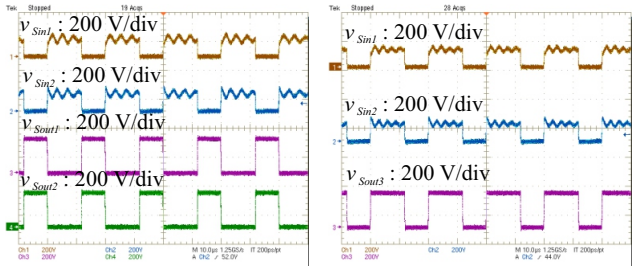


FIGURE 8. Losses Distribution.

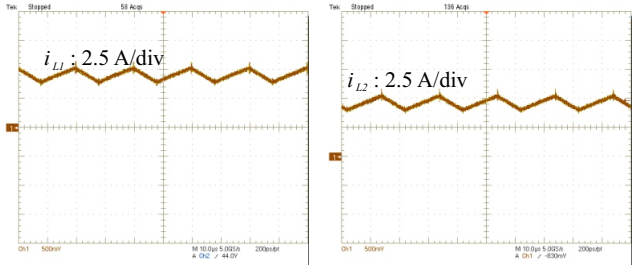
VIII. PERFORMANCE COMPARISON

To present the advantages and limitations of the proposed converter, the converters in Table 2 are compared. In terms of total number of components, the proposed converter has the highest number of components, followed in order by [20], [25], [22], [26], and [13]. Additionally, the proposed converter exhibits one of the lowest voltage stresses on its switches, followed by [22], [20], [25], and [13]. In terms of voltage gain, the converter [25] shows the highest gain, followed by the proposed converter, [20], [26], [13] and [22].



(a) (b)

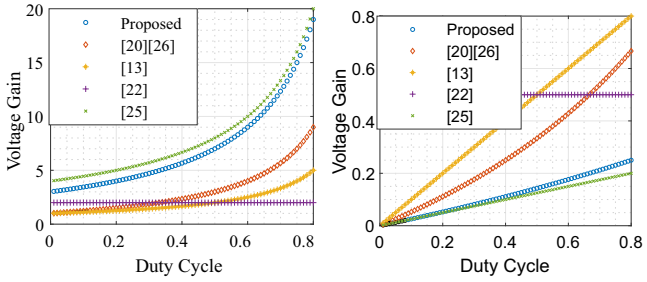
FIGURE 9. Voltage across semiconductor devices for step-down mode.



(a) (b)

FIGURE 10. Current through the inductors (a) L_1 and (b) L_2 for step-down mode.

For better understanding about the voltage gain, it is plotted in Fig. 11 for all of the converters in Table II. In this sense, the proposed converter has a disadvantage in the number of components, but it is superior in voltage stress and presents the second highest voltage gain, even when compared to converters with the same operating technology.



(a) (b)

FIGURE 11. Voltage gain for (a) step-up mode. (b) Step-down mode.

IX. EXPERIMENTAL RESULTS

To validate the theoretical analysis, experimental results were performed in laboratory in order to compare the results with the theoretical equations. The practical results considered 72 V / 400 V and 500 W, additionally, the others parameters used can be seen in Table 1. To define the low and high voltage sources (V_L and V_H), a Keysight N8762A DC power supply was employed in the experimental setup. An STM32F411 Digital Signal Processor was utilized

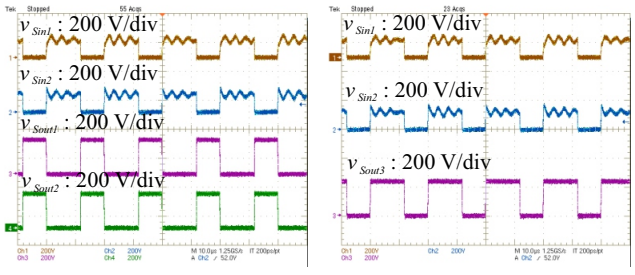
TABLE 2. Converters Comparative Table

Converter	Step-up Gain	Step-down Gain	Maximum Voltage Stress on Switches S_{in}	Maximum Voltage Stress on Switches S_{out}	Switches Count	Inductor Count	Capacitor Count	Step-up technique
Proposed	$1+\frac{2+2D_H}{1-D_H}$	$-\frac{4}{D_L-4}-1$	$\frac{V_L+V_{C_1}}{2}$	V_H-V_{C1}	5	2	4	Voltage multiplier cell
Converter [13]	$\frac{1}{1-D}$	D	V_H	V_H	2	1	2	Classical boost converter
Converter [20]	$\frac{1+D}{1-D}$	$\frac{D}{2-D}$	$\frac{V_H+V_L}{2}$	$\frac{V_H+V_L}{2}$	4	2	4	Switched inductor
Converter [25]	$\frac{4}{1-D}$	$\frac{D}{4}$	$\frac{V_H}{4}$	$\frac{V_H}{2}$	3	2	5	Voltage multiplier cell
Converter [22]	2	$\frac{1}{2}$	V_L	V_L	5	0	4	Simple switched capacitor
Converter [26]	$\frac{1+D}{1-D}$	$\frac{D}{2-D}$	$\frac{V_L+V_H}{2}$	$\frac{V_L+V_H}{2}$	3	2	4	Voltage multiplier cell

to generate the PWM signal and control routine. Lastly, a Yokogawa WT1800 power analyzer was used to assess efficiency. The control results were obtained in closed-loop, with the compensators presented in Eq. (37-38).

A. Voltage results

The voltage across the semiconductor devices is presented in Fig. 12 and Fig. 9 for step-up and step-down modes, respectively. Additionally, the voltage across the switches is within the calculated parameters, reaching approximately 180 V for semiconductors S_{in1} and S_{in2}. Furthermore, semiconductors S_{out1}, S_{out2}, and S_{out3} showed around 235 V between their terminals.



(a) (b)

FIGURE 12. Voltage across semiconductor devices for step-up mode.

Owing to the natural clamping effect inherent to the semiconductors S_{out1}, S_{out2}, and S_{out3} in the proposed topology, the measured voltage stresses across these devices were in close agreement with the theoretical predictions. In contrast, the switches S_{in1} and S_{in2} are not subject to such natural clamping. Due to the presence of parasitic inductances, combined with the inductance mismatch between L_1 and L_2, the peak current at the end of the energy storage interval becomes unequal in the two inductors. When these inductors are subsequently connected in series during the transfer stage, the arrangement effectively corresponds to two current sources with different instantaneous values. This mismatch gives rise to overvoltages, as the surplus current is abruptly discharged into the switch capacitances. As a result, the semiconductors S_{in1} and S_{in2} experienced a voltage stress of 180 V, diverging from the 120 V predicted by the theoretical analysis.

B. Current results

The current passing through the magnetic devices (L_1 and L_2) is presented in Fig. 13 and Fig. 10 for step-up and step-down modes, respectively, these current achieves an average value of 4.1 A.

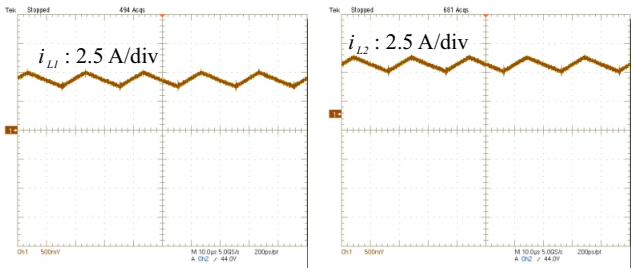


FIGURE 13. Current through the inductors (a) L_1 and (b) L_2 for step-up mode.

C. Control results

To demonstrate the effectiveness of the control system from the proposed converter, Fig. 14(a) shows the control system acting first in a step change from minimum load to full load, and then from full load to half load. In both tests, it is notable that the control system quickly regulated the voltage V_H to prevent fluctuations and deviations from the reference values.

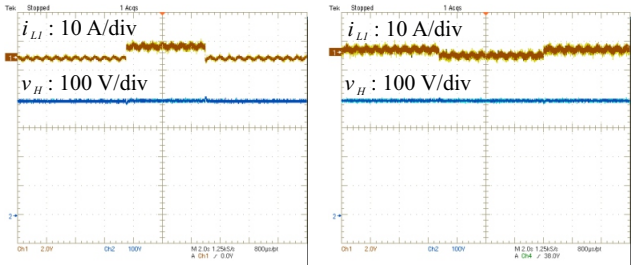


FIGURE 14. Experimental results of control under (a) step load and (b) power flux reversion.

To verify the bidirectionality and proof the online power flux reversion, Fig. 14(b) shows the online reversal of power flow, where the inductor current shifts from +2A, passing through zero, and reaches -2A, indicating a flux reversion from step-up to step-down mode. Additionally, in the second phase, the reversion occurs from step-down to step-up mode, moving from -2A, passing through zero, and reaching +2A. Due to the zero-crossing of the inductor current, this test can be considered the most unstable test for bidirectional converters, which definitively proves that the control system was still able to reverse the power flow and keep the voltage V_H regulated without the need to restart the converter.

D. Efficiency results

The Fig. 15 presents the efficiency curve within the evaluated power range for the converter, where positive power indicates operation in step-up mode, while negative power corresponds to step-down mode.

In step-up mode, the converter starts operating at 80 W with an efficiency of 96.1%. The curve follows an increasing

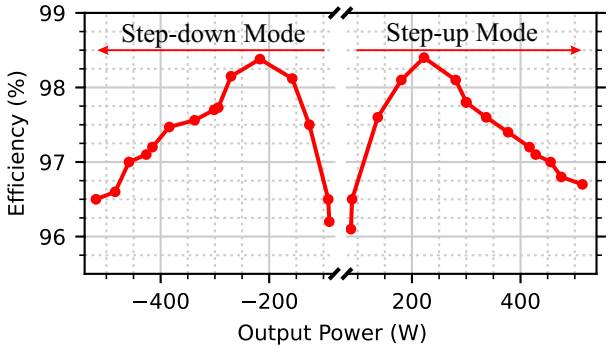


FIGURE 15. Experimental results of efficiency.

trend, reaching a peak efficiency of approximately 98.4% at 250 W. Beyond this point, efficiency begins to decline, reaching 96.7% at 500 W. The efficiency curve in step-up mode is quite similar to that in step-down mode, with minor variations that may be attributed to the resonance process of switches S_{in1} and S_{in2}.

Additionally, the efficiency curve exhibits three distinct phases: an initial increase, followed by a peak, and subsequently a decline. This behavior can be explained by the fact that, at low power levels, switching losses are more significant relative to the operating power. At the efficiency peak, the converter operates at its optimal point. The subsequent decline in efficiency is primarily due to the ohmic losses of the semiconductor devices.

X. CONCLUSION

This paper presents an analysis of a bidirectional converter for interfacing different voltage levels in renewable energy applications. The converter was based on a switched inductor with a voltage multiplier cell. This approach enables an increase in voltage gain compared to the conventional technique of using only a switched inductor.

The analyzed converter was tested under various operating conditions within its operational range, achieving a peak efficiency of 98.4% while operating at 250 W. Furthermore, the proposed converter was compared with other converters employing similar technologies, demonstrating advantages in terms of voltage gain and voltage stress on the switches.

Moreover, with a simple control strategy, the converter can be assessed under different dynamic operating conditions, confirming that the proposed topology can reverse the power flow online without requiring shutdown and restart to invert the direction of power flux. Additionally, the experimental results exhibited strong agreement with the theoretical analysis.

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AUTHOR'S CONTRIBUTIONS

F.G.NIMITTI: Conceptualization, Data Curation, Formal Analysis, Investigation, Project Administration, Resources, Supervision, Validation, Visualization, Writing – Original Draft. **A.M.S.S.ANDRADE:** Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Project Administration, Resources, Supervision, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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