Original Paper

Eletrônica de Potência
Open Journal of Power Electronics

Received September 18, 2025; Received in revised form November 10, 2025; Accepted November 25, 2025; Date of publication January 09, 2025.
The review of this paper was arranged by Associate Editor Montiê A. Vitorino and Editor-in-Chief Allan F. Cupertino.
Digital Object Identifier http://doi.org/10.18618/REP.e202603

Analysis and Design of a Half-Bridge Converter with Current Doubler for Auxiliary Power Modules in Electric Vehicles

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ABSTRACT Electric vehicles (EVs) demand highly efficient power management systems to enhance reliability and extend operational autonomy. Unlike traditional internal combustion engine (ICE) vehicles, which use alternators to supply low-voltage systems, EVs rely on DC-DC converters, commonly referred to as Auxiliary Power Modules (APMs). This paper presents the analysis, design, and experimental validation of a half-bridge converter with a current-doubler (HB-CD) topology tailored for APM applications. A generalized structure is proposed to support the parallel operation of multiple modules, aiming to mitigate current stress and reduce output ripple. A 3 kW laboratory prototype was implemented using two 1.5 kW modules operating in parallel, enabling interleaved operation and effective current sharing. Experimental results demonstrate the converter's ability to maintain high efficiency, reaching up to 94.6% under nominal conditions and 95.9% under minimum input voltage operation, confirming the feasibility of the proposed topology for high-current automotive applications.

KEYWORDS Auxiliary Power Module, DC-DC converter, electric vehicles.

I. INTRODUCTION

EVs have been extensively researched to improve their appeal and competitiveness in the global automotive market. The transition from ICE vehicles to EVs aims to reduce greenhouse gas emissions and dependence on fossil fuels [1]. In this context, recent advances in power conversion and energy storage can reduce EV cost and weight, an important factor for driving range [2].

Conventional ICE vehicles use a low-voltage (LV) system powered by a belt-driven alternator, supplying a 12 V battery and loads such as headlights, multimedia systems, alarm and Electronic Control Unit (ECU). In EVs, two distinct systems exist: a high-voltage (HV) system for traction and a LV system for auxiliary loads. The latter typically operates at 14 V (12 V nominal), while the HV system operates at 400 V or 800 V. A DC-DC converter, known as the auxiliary power module (APM), is used to interface both systems [3].

The APM has several vital specifications, such as galvanic isolation [4], which avoids a ground loop formation between the HV network and the LV network in EVs, a condition that can also pose a fatal risk to humans [5]. Other essential requirements of the converter are high reliability, high power density, and high efficiency, which directly affect the vehicle autonomy. An essential aspect of the APM is ensuring the quality of its output voltage. Electronic loads, including control units, radios, and media systems, are particularly sensitive to the ripple content in the voltage supplied by the APM. Therefore, it is crucial to maintain a low output voltage ripple [6].

In ICE vehicles, the current supplied by the alternator for a typical compact car usually ranges from 75 to 150 A. In contrast, EVs present a higher power demand on the LV system because loads that were previously mechanically driven by the engine, such as the air conditioning compressor, are now powered by the APM. Furthermore, in many EVs, the batteries, traction inverters, and the APM are water-cooled, which requires electric pumps and fans. As a result, the current on the 12 V side can reach up to 250 A, leading to significant conduction losses in the LV side of the converter [7].

Several studies in the literature offer innovative approaches for APM implementation. For instance, [8] compares the full-bridge LLC resonant converter and the phase-shifted full-bridge converter, highlighting their differences and applications. In [9], a novel reconfigurable current-fed converter is proposed, capable of operating across a wide input (180 V to 900 V) and output (6 V to 16 V) voltage ranges, providing versatility for different applications. In [10], the dual active bridge (DAB) converter is used, with an input voltage range from 240 V to 450 V and an output volt-

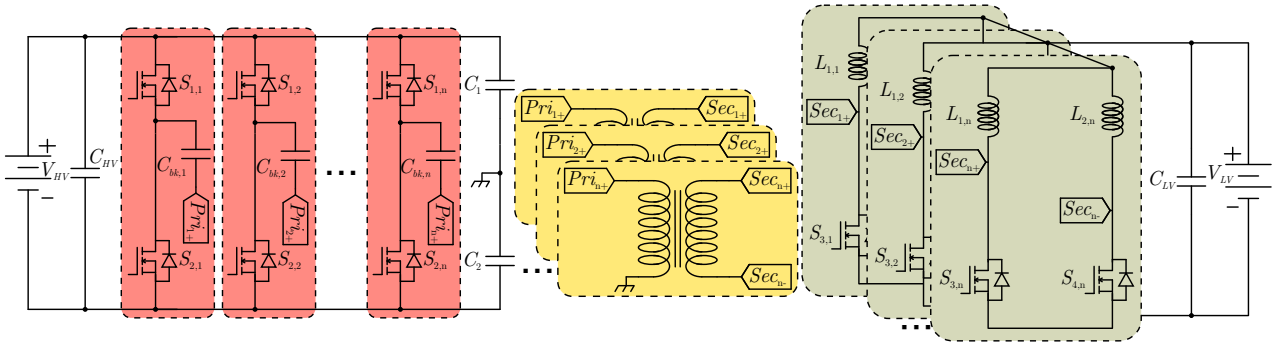


FIGURE 1. Generalized configuration with parallel input half-bridge converters and parallel output current doubler cells.

age range from 11 V to 16 V. In [11], a 1.5 kW half-bridge converter employing an isolated current doubler rectifier was presented. The authors did not implement parallel operation, and the analysis was carried out at a single operating point, corresponding to 400 V on the HV side and 12 V on the LV side. In [12], a converter with two distinct operating modes is proposed. For low input voltage range (350 V to 590 V), it operates as a three-switch forward converter with a double-ended active clamp. On the other hand, for high input voltage range (590 V to 800 V), it operates as an asymmetric half-bridge converter. In [13], an LLC half-bridge topology is used on the primary side of the DC-DC converter, while on the secondary side, a novel synchronous rectification control (SRC) strategy was developed using the full-bridge topology.

These studies consistently highlight that high output currents negatively impact both efficiency and power density in APM. In response to this challenge, this paper proposes a generalized isolated half-bridge converter topology with a current doubler on the secondary side. The generalized structure considers the parallel operation of multiple identical modules, all employing the same transformer turn ratio connected through a shared high-frequency transformer interface. This configuration enables the distribution of current among modules, thereby reducing conduction losses and minimizing output current ripple through interleaved operation.

In this article, a generalized modular half-bridge converter with a current-doubler rectifier (HB-CD) is proposed for EV APM. The proposed architecture enables the parallel connection of multiple converter modules through a shared transformer interface, providing natural current sharing and reducing conduction losses, which are the dominant loss component in this type of application. An interleaving strategy with a 90° phase shift between modules is proposed and experimentally validated, demonstrating effective ripple cancellation and balanced current distribution. The converter employs SiC Cascode on the primary side featuring four-pin packages which allows cleaner switching transitions and lower switching losses. On the secondary side, low-voltage, high-current Si MOSFETs in SMD packages connected in parallel are used, providing high efficiency. Planar transformers and inductors further enhance power density and enable compact construction suitable for high-current automotive environments. The inherent modularity of the proposed topology allows scalability of output power by adding modules in parallel while maintaining proper current balance. A 3 kW prototype, composed of two 1.5 kW modules, was designed and experimentally tested, achieving up to 95.9% efficiency and confirming the feasibility and effectiveness of the proposed approach.

This paper is organized as follows: Section II presents the half-bridge topology with the current doubler and its operating stages for one module. Section III describes the parallel connection of modules on both sides, evaluating the interleaving operation among the modules. Section IV presents and discusses the experimental results for an 3 kW module. Finally, Section V presents the main conclusion of the article.

II. DESCRIPTION OF THE TOPOLOGY

The topology under evaluation as an APM in this article is the PWM half-bridge converter on the primary side with a current doubler on the secondary side (HB-CD), connected through a high-frequency isolation transformer. This topology can be further generalized by connecting multiple half-bridge cells on the primary side with a single capacitive bus and a parallel connection of current doubler converters on the low voltage side, as shown in Figure 1.

This topology is interesting for several reasons, such as: (i) for a given current doubler cell, each inductor conducts half of the output current; (ii) the secondary switches operate in Zero Voltage Switching (ZVS); (iii) the half-bridge topology on the primary side applies only half of the bus voltage, allowing for a lower turns ratio to step down the voltage; (iv) there is no current in the transformer and primary switches during the secondary freewheeling stages, while in the secondary, the switches share the current; (v) PWM with a fixed frequency leads to low control complexity, easy filter design, and simple synchronous rectification strategy; (vi) current doubler configuration on the secondary side results in natural inductor current interleaving at the cell level, multiplying the effective ripple frequency at the output capacitor compared to the switching frequency, which allows for a reduction in

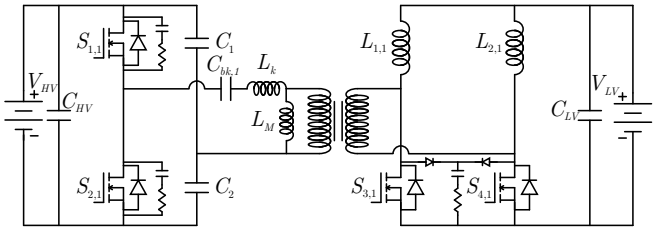


FIGURE 2. Isolated half-bridge converter with ouput current doubler.

filter volume; (vii) on the primary side of the converter, due to the leakage inductance of the transformer in series with the semiconductors, the current through the switches increases with a limited slope, reducing the overlap between current and voltage in these switches, which in turn decreases the switching losses on the primary side.

A simplified structure using only one module is shown in Figure 2, which has two switches on the HV primary side, two switches on the LV secondary side, a high-frequency isolation transformer, a split capacitive bus, and two inductors at the output. In addition, snubber circuits are required in the converter. These circuits are recommended by semiconductor manufacturers due to the high current derivatives (di/dt) present during switching transitions. Particularly on the secondary side, snubbers play a crucial role in suppressing voltage spikes caused by the parasitic inductances of the layout and transformer windings, thereby improving switching reliability and reducing voltage stress across the devices.

The PWM strategy of the converter is simple, with the two switches on the primary side symmetrically switching with a 180-degree phase shift. The switches on the secondary side are complementary to their respective primary switches (S_3 is complementary to S_1 and S_4 is complementary to S_2). The converter operates according to the following stages.

The converter operates in eight stages, four during each symmetrical half-cycle. Therefore, stages five to eight exhibit the same behavior as stages one to four and, for this reason, are not described in detail. The first four operating stages are summarized below:

First Stage [t_0–t_1]: Switch S_1 is turned on while S_2 remains off. On the secondary side, switches S_3 and S_4 initially share the output current. As the leakage inductance L_k charges, the current through S_3 decreases to zero, causing S_4 to conduct the full load current. The stage ends when the transformer secondary current equals the current through inductor L_1.

Second Stage [t_1–t_2]: Switches S_1 and S_4 conduct simultaneously, applying $V_{HV}/2$ to the transformer primary. During this interval, the current through S_4 equals the output current.

Third Stage [t_2–t_3]: When S_1 turns off, the leakage inductance current naturally flows through the body diode of S_2, clamping the voltage across S_1 to V_{bus}. On the secondary side, the currents through S_3 and S_4 converge to $I_{LV}/2$. This stage ends when the energy stored in L_k is completely discharged.

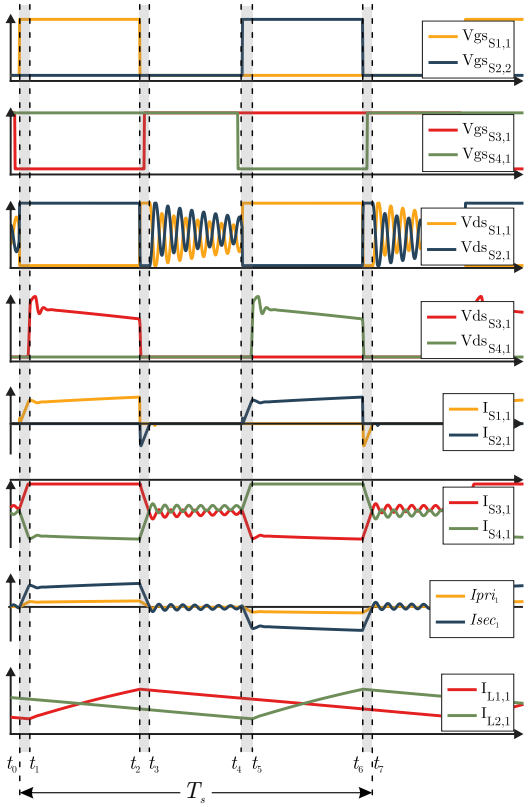


FIGURE 3. Main waveforms.

Fourth Stage [t_3–t_4]: After the current in L_k reaches zero, a resonant transition occurs among the switches output capacitances (C_{oss}), the snubber network, and L_k. The resulting oscillation is centered around $V_{HV}/2$. Both S_3 and S_4 then share the output current equally.

Figure 3 shows the main waveforms of the power module presented in Figure 2.

A. Design Methodology and Component Sizing

The proposed converter was designed for a rated power of 3 kW, defined as the requirement to supply a complete set of LV loads in an EV.

According to the EV architecture, the converter must interface the HV traction bus and the LV auxiliary network. Therefore, the design was constrained to an input voltage range of 250–400 V and an output voltage range of 10–14 V, covering typical battery conditions and transient variations in the auxiliary system. The switching frequency was set to 100 kHz, representing a compromise between magnetic component size, switching losses, and control simplicity.

The transformer turns ratio (n) was defined based on the maximum duty cycle that the converter can operate ($D_{max} = 0.5$) and on the required input and output voltage ranges. The duty cycle of the converter is given by

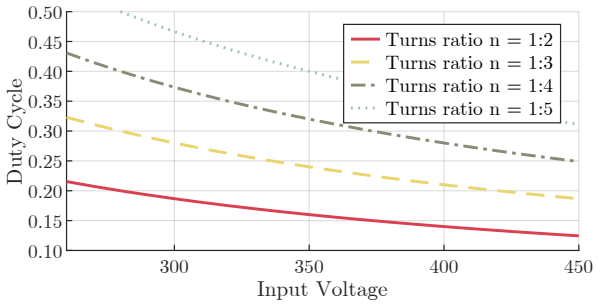


FIGURE 4. Duty cycle as a function of input voltage for different n, considering $V_{LV} = 14$ V.

$$D = \frac{2nV_{LV}}{V_{HV}}, \tag{1}$$

where n is the transformer turns ratio, V_{LV} is the LV output, and V_{HV} is the HV input. Considering the maximum required output voltage of 14 V, the duty cycle variation as a function of input voltage was obtained and is shown in Figure. 4

As observed, turns ratios of $n = 2$, $n = 3$, and $n = 4$ are capable of covering the entire operating range. However, lower n result in higher secondary voltages, which require MOSFETs with higher voltage ratings and, consequently, higher on-state resistances ($R_{DS(on)}$), increasing conduction losses. Therefore, the turns ratio $n = 4$ was selected to allow operation over the full input voltage range while keeping the secondary voltage low enough to employ devices with lower breakdown voltage and reduced channel resistance, thus improving overall efficiency.

Once the transformer design parameters were established, the sizing of the output inductors was carried out to complement the magnetic design, ensuring proper current filtering and minimized output ripple. In the current-doubler stage, each output inductor carries half of the total module current. The design targeted a peak-to-peak current ripple of approximately 20% of each inductor's average current (i.e., 20% of $I_{LV}/2$), which ensures reduced voltage ripple at the output and proper current sharing between the modules. The inductance value was calculated using:

$$L = \frac{(V_{sec} - V_{LV})D}{\Delta i_L f_s}, \tag{2}$$

where V_{sec} is the secondary transformer voltage, Δi_L is the peak-to-peak inductor current ripple, and f_s is the switching frequency. Considering nominal conditions ($V_{sec} = 50$ V, $V_{LV} = 12$ V, $D = 0.24$, $\Delta i_L = 0.2 I_{LV}/2$, and $f_s = 100$ kHz), the resulting inductance is approximately 3.3 µH. This value provides an effective compromise between magnetic volume, transient response, and current ripple attenuation.

Following the magnetic design, the switching performance of the converter was analyzed. In high-speed converters employing SiC devices with low gate resistance, the resulting high dv/dt rates can cause voltage overshoot and electromagnetic interference (EMI). To mitigate these effects, several device manufacturers recommend the use of RC snubber networks connected in parallel with the power switches [14]–[16]. These circuits limit the V_{DS} peak voltage, suppress ringing caused by parasitic inductances and capacitances, and reduce EMI without introducing additional gate delay. Typical snubber parameters (R_S, C_S) for the selected primary-side switches are recommended in the manufacturer's datasheet, ensuring an optimized balance among voltage suppression, switching losses, and dynamic performance.

On the secondary side, the synchronous rectifiers experience voltage transients caused by leakage inductance and reverse-recovery interactions between the transformer and the rectifier devices. In this case, the snubbers were specifically designed to suppress these experimentally observed spikes. The sizing process was guided by the classical methodology proposed in [15], [17], [18], where analytical estimations provide the initial component sizing, later refined through simulation and experimental adjustment.

The snubber resistor is first determined to define the desired clamping voltage and dissipate the energy stored in the leakage inductance

$$R_S = \frac{V_{SN}^2}{\frac{1}{2} L_k I_{\text{peak}}^2 f_s} \frac{(V_{SN} - nV_O)}{V_{SN}} \tag{3}$$

where L_k is the leakage inductance referred to the secondary side ($L_k = 0.206$ µH, obtained from $L_{LK,pri} = 3.3$ µH and $n = 4$), I_{peak} is the peak current associated with the leakage energy ($I_{\text{peak}} = 15$ A), f_s is the switching frequency ($f_S = 100$ kHz), nV_O represents the reflected output voltage across the switch ($nV_O = 50$ V), and V_{SN} is the desired clamping voltage ($V_{SN} = 70$ V).

Once R_S is defined, the snubber capacitance is obtained by imposing a limited voltage ripple across the capacitor

$$C_S = \frac{V_{SN}}{\Delta V_{SN} R_S f_s} \tag{4}$$

where ΔV_{SN} is the allowed voltage variation across the capacitor (here, $\Delta V_{SN} = 0.1 V_{SN} = 7$ V).

For the given parameters, the resulting snubber components were $R_S = 620\ \Omega$ and $C_S = 180$ nF. This analytical approach ensures an adequate damping of the resonant network formed by L_k and C_{oss}, while maintaining the voltage stress in the safe operating limits of the secondary MOSFETs.

III. GENERALIZED PARALLEL OPERATION

The topology introduced in Section II can be extended to a generalized configuration that allows the parallel operation of multiple converter modules. In this structure, the primary sides of the converter are connected in parallel, as well as the secondary sides, as depicted in Figure 1. This arrangement enables modular operation and effective current sharing among the converter units.

In this application, conduction losses dominate due to the high currents on the LV side. Thus, developing strategies to minimize conduction losses becomes crucial. One of the practical solutions is the use of parallel modules, which reduces the current flowing between the components by distributing it among the modules. This strategy not only reduces conduction losses but also has the potential to decrease the output current ripple of the converter.

The current ripple reduction is achieved by interleaving the inductor currents by phase-shifting the PWM carriers. This technique increases the effective frequency of the output components and reduces the ripple magnitude. Specifically, the effective frequency of the summed output current becomes twice the number of parallel-connected modules ($N_{modules}$), as expressed in

$$f_{I_{LV}} = 2 f_s N_{modules}, \tag{5}$$

in which the key factors governing the performance of parallel operation are the number of modules and the phase shift angle ($\Phi_{modules}$) between the carrier signals controlling the switching devices. These parameters are interdependent, as the phase shift angle is determined based on the number of modules, as described in

$$\Phi_{modules} = \frac{180^\circ}{N_{modules}}. \tag{6}$$

Internally, the HB-CD module operates with two complementary PWM carriers, establishing an intrinsic 180° phase displacement between the currents of the two output inductors within each module. Applying the conventional 180° phase shift between the two parallel modules would be counterproductive, as the ripple components of the equivalent inductors would align in phase, resulting in additive ripple. Therefore, a 90° phase displacement is adopted between the PWM carriers of the two distinct modules. This approach properly distributes the four inductor current waveforms over the switching period, leading to effective harmonic cancellation and a significant reduction in the output current ripple.

The design of the output inductors is also influenced by the number of modules in parallel. As the number of modules increases, each inductor carries a proportionally smaller portion of the total output current. To maintain the same relative current ripple in each inductor, the inductance value should scale approximately with the number of modules. In the absence of interleaving, maintaining a constant overall current ripple would require proportionally larger inductance values. However, interleaving operation naturally reduces the net ripple at the converter output, allowing smaller inductors or higher individual ripple levels without compromising the total current quality.

Considering a transformer turns ratio of $n = 4$, a switching frequency of $f_s = 100$ kHz, and output inductors of $L = 3.3$ μH, with an output power of $P_{\text{out}} = 3$ kW, the output current waveforms, shown on Figure 5, were obtained by applying phase shifting according to (6) under different operating conditions.

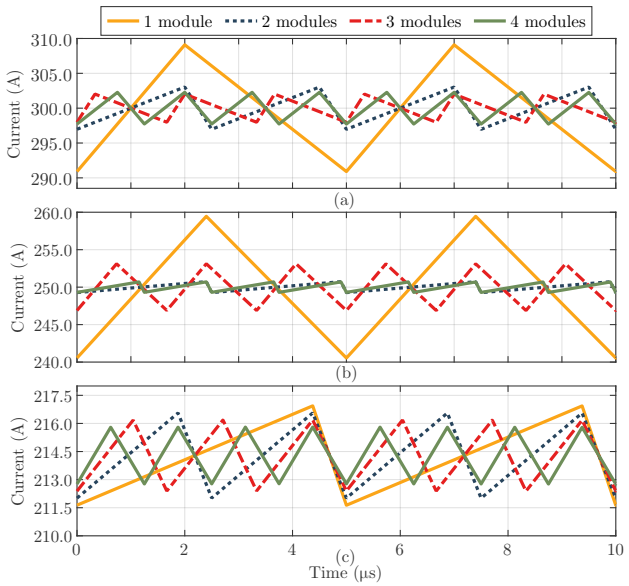


FIGURE 5. Comparison of the output current for different conditions: (a) V_{HV} = 400 V and V_{LV} = 10 V, (b) V_{HV} = 400 V and V_{LV} = 12 V, (c) V_{HV} = 256 V and V_{LV} = 14 V.

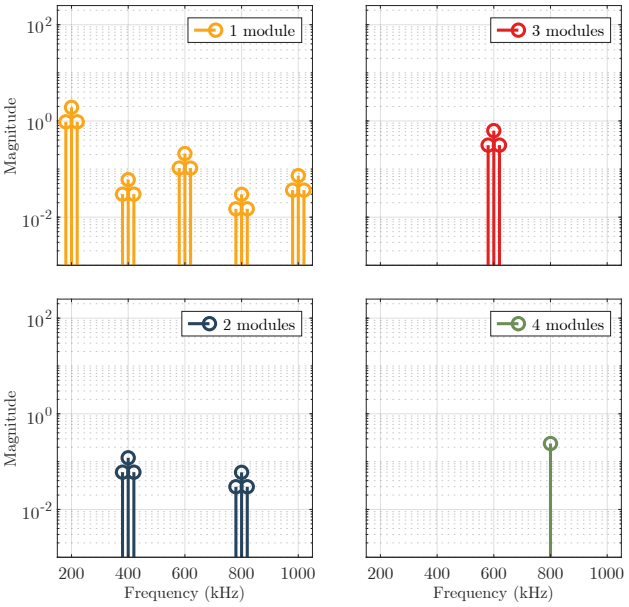


FIGURE 6. Harmonic spectrum of the output current for V_{HV} = 400 V and V_{LV} = 12 V.

Performing the frequency domain analysis, the result is presented in Figure 6. It can be observed that the harmonic content decreases as more modules are connected in parallel, leaving only multiples of the fundamental operating frequency $f_{I_{LV}}$ for each module configuration.

As illustrated in Figure 5 and 6, increasing the number of modules increases the effective frequency of the the output current I_{LV}. Furthermore, reducing the output current ripple is crucial, as high output current ripple degrades and shortens the lifespan of batteries [19].

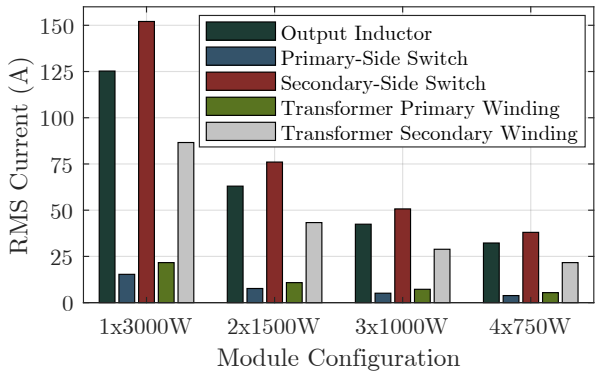


FIGURE 7. RMS current per power component for different numbers of parallel modules. V_{HV} = 400 V and V_{LV} = 12 V.

As shown in Figures 5 and 6, increasing the number of parallel modules not only raises the effective ripple frequency but also reduces the amplitude of the output current ripple. This effect is highly beneficial in automotive systems, where excessive ripple current can degrade the lifetime and efficiency of auxiliary batteries [19]. Furthermore, the ripple reduction directly impacts the required capacitance at the converter output. According to [20], the current-doubler rectifier benefits from inherent ripple cancellation under interleaved operation. Since the required output capacitance is inversely proportional to the square of the ripple frequency, doubling the effective frequency can reduce the necessary capacitance by up to a factor of four. Consequently, the proposed interleaved parallel operation not only improves electrical performance and reliability but also contributes to a more compact and cost-effective converter design.

A. CURRENT STRESS COMPARISON

In addition to output ripple attenuation, parallel module operation enhances current sharing, thereby simplifying the design and physical implementation of each module. Figure 7 presents the RMS current levels observed in key power components for systems employing one to four modules.

A single-module configuration must handle the full output power, resulting in high current stress on the secondary-side devices. As evident in Figure 7, this leads to elevated RMS currents and excessive conduction losses. Additionally, the lack of interleaving prevents any ripple frequency enhancement, requiring larger output capacitors to meet ripple specifications. This increases both the cost and the physical size of the output stage, while also limiting the dynamic performance of the converter.

Although configurations with three or four modules offer marginal improvements in ripple attenuation, they also incur a significant increase in component count and system complexity. The additional modules require more semiconductors devices, gate drivers, current sensors, transformers, and PCB area, while also complicating synchronization. Moreover, the ripple improvement from two to three modules is relatively small, as observed in Figures 5 and 6, rendering the additional cost unjustified in many cases. The use of four modules yields the best ripple performance but results in diminishing returns when weighed against the increased design burden.

TABLE 1. Converter and Component Parameters

Parameter	**Value**
Output power	$P_{out} = 3000$ W
Input voltage	$V_{HV} = [256 - 400]$ V
Output voltage	$V_{LV} = [10 - 14]$ V
Output Current	$I_{LV} = [0 - 250]$ A
Transformer ratio	$n = 4$
Switching frequency	$f_s = 100$ kHz
Inductors	$L_{1,1} = L_{2,1} = L_{1,2} = L_{2,2} = 3.3$ μH
Capacitors	$C_1 = C_2 = 10$ μF
Leakage inductance	$L_k = 3.34$ μH
Magnetizing inductance	$L_m = 731.79$ μH
Primary snubber (RC)	$R_S = 10$ Ω, $C_S = 100$ pF
Secondary snubber (RCD)	$R_S = 680$ Ω, $C_S = 100$ nF, $Diode = STPS10H100SFY$
Component (Part number)	**Main Parameters**
$S_{1,1}$, $S_{2,1}$, $S_{1,2}$, $S_{2,2}$ (UJ4C075060K4S)	SiC, 750 V $R_{DS(on)}$ = 60 mΩ (T_j = 25 °C)
$S_{3,1}$, $S_{4,1}$, $S_{3,2}$, $S_{4,2}$ (IPT017N10NF2S)	Si, 100 V $R_{DS(on)}$ = 1.6 mΩ (T_j = 25 °C)
$L_{1,1}$, $L_{2,1}$, $L_{1,2}$, $L_{2,2}$	3.3 μH, PQ3218-3R3-70-T, (Standex Electronics)
High frequency transformer	T250-16-4, (Payton Planar)

The two-module configuration provides an optimal trade-off between electrical performance and implementation complexity. It enables effective ripple reduction via interleaved operation and provides substantial relief in current stress, particularly in the secondary-side components. Furthermore, the modularity reduces capacitor sizing requirements, and maintains a compact and cost-effective design, making it the most practical choice for the proposed APM converter topology.

IV. EXPERIMENTAL RESULTS

A laboratory prototype of the proposed APM was built using two 1.5 kW converter modules operating in parallel, resulting in a total output power of 3 kW. This configuration enables the evaluation of the converter's performance under interleaved operation with current sharing. Table 1 lists the key parameters and part numbers used in the prototype. A photograph of the implemented hardware is shown in Figure 8.

The operation of the converter under nominal conditions using a single 1.5 kW, module is presented in Figure 9, considering an output voltage of 12 V and an output current of 125 A.

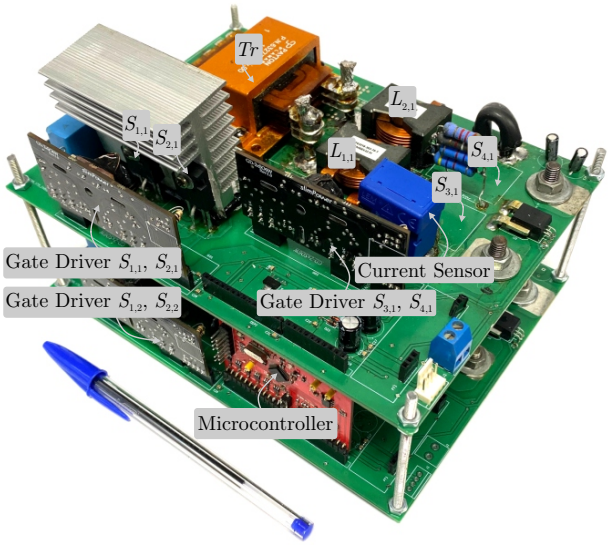


FIGURE 8. Implemented prototype. Measuring: 200 mm x 150 mm x 120 mm.

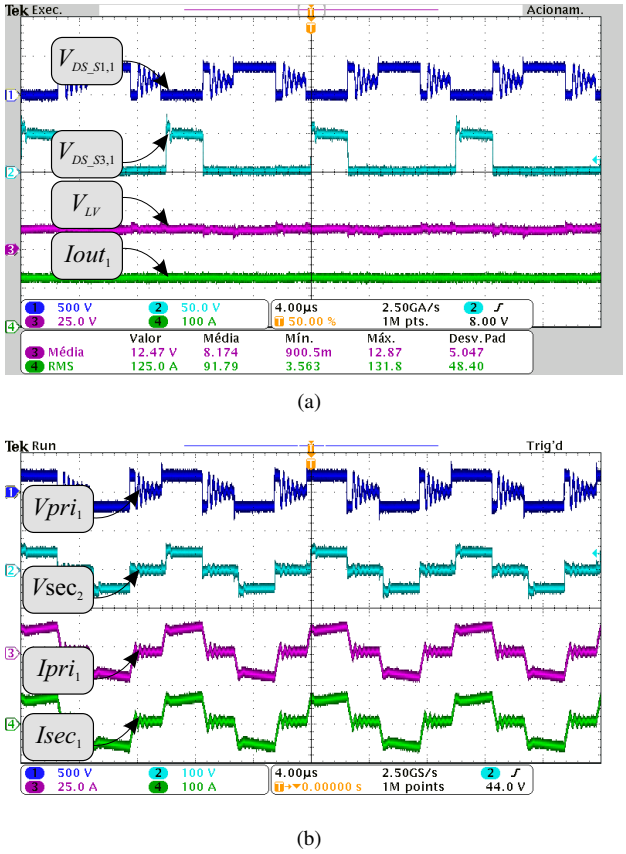


FIGURE 9. Experimental results: (a) Voltage on MOSFETs: $V_{DS\_S1,1}$ (CH1) and $V_{DS\_S3,1}$ (CH2). Output voltage: V_{LV} (CH3) and output current: I_{LV} (CH4); (b) Transformer voltage: V_{pri_1} (CH1) and V_{sec_1} (CH2). Transformer current: I_{pri_1} (CH3) and I_{sec_1} (CH4).

Figure IV shows at the drain-source voltage of the SiC MOSFET $S_{1,1}$. where it can be observed that the maximum voltage across the switch equals the DC bus voltage (400 V). When the two switches on the primary side are off, a resonance occurs due to the energy exchange between the leakage inductance, the snubber circuit and the parasitic capacitances of the $S_{1,1}$ and $S_{2,1}$. The drain-source voltage on the secondary-side MOSFET $S_{3,1}$ is shown in channel CH2. It can be seen that, due to the transformer leakage inductance, there is a voltage spike on the switch, even with the implementation of an RCD snubber.

Figure IV shows the voltages and currents on the high-frequency transformer. One can see that the maximum voltage at the primary side is $V_{HV}/2$ and the minimum value is $-V_{HV}/2$.

A digital closed-loop current control using a proportional–integral (PI) controller was implemented on a TMS320F280037C microcontroller. The control system was designed considering the measurement taken from one of the two inductors in each module, which corresponds to half of the output current of that module. Considering that two modules operate in parallel, each inductor therefore conducts one fourth of the total output current.

The PI controller adjusts the PWM duty cycle of each module, while the PWM carriers are synchronized and interleaved by 90°. This configuration guarantees balanced current distribution and effective ripple cancellation.

Figure IV illustrates the converter operation at a total output power of 3 kW, with an input voltage of $V_{\mathrm{HV}} = 400$ V and an output voltage of $V_{\mathrm{LV}} = 12$ V. The test was conducted using a programmable NHR 4760 DC electronic load emulating the EV 12 V battery system. The figure also shows the output currents of each individual module. Initially, each converter delivers approximately 100 A. After a step in the output current reference, both modules transition to a balanced condition, each supplying approximately 125 A. This behavior confirms proper current sharing between the modules and validates the expected full-load operation at 3 kW. A brief voltage variation in V_{LV} was observed during the transient; however, it did not compromise the converter stability or current balance. This behavior occurred because the electronic load was configured in constant-voltage mode, which has its own dynamic response. When the current reference step was applied, the current momentarily increased the output voltage before the electronic load regulated it back to 12 V. Therefore, the transient deviation in V_{LV} was caused by the load dynamics rather than by the converter operation itself.

Figure IV presents the phase shift between the PWM carriers of the two modules, implemented to achieve output current ripple cancellation. It can be observed that the secondary-side voltages of the transformers and the inductor currents exhibit a 90º phase shift relative to each other, as predicted by (6), representing the optimal interleaving condition for two parallel modules.

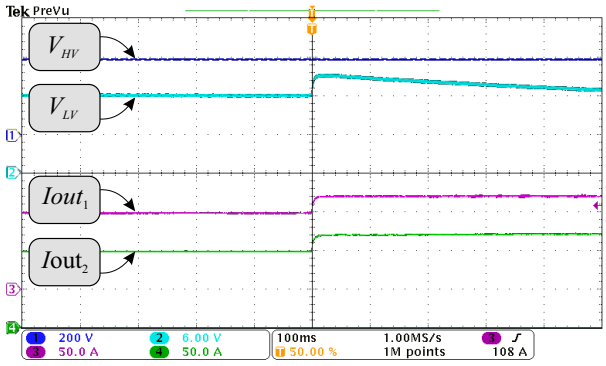
The efficiency curve of the APM for different output voltage levels, with a constant input voltage of 400 V, is shown

TABLE 2. Specifications and performance comparison

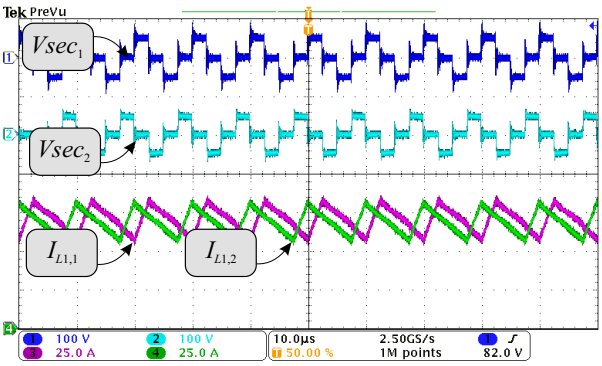
Products / Prototypes	Input range (V)	$SCD_{ct.}$[1]	f_s (kHz)	Power (W)	Peak Efficiency	Full load efficiency	Power density (kW/L)
LLC half-bridge [13]	[220 - 400]	6	[90-200]	2500	93.2%	92.4%	-
Gen5 High Voltage DC-DC [21]	[220 - 800]	-	-	1200	>92%	>92%	0.22†
High voltage DC-DC [22]	[225 - 455]	-	-	3100	>94%	>92%	1.00†
Full-Bridge Center Tap [23]	[240 - 400]	6	500	2700	>94%	>90%	6.00
ISHB zeta converter [24]	[460 - 780]	8	700	1200	93.4%	91.6%	10.20
Two-mode low voltage DC-DC converter [12]	[350 - 800]	6	70	600	>92%	>90%	-
3evo high voltage DC-DC [25]	[250 - 475]	-	-	3600	$\leq$ 95%	$\leq$ 95%	-
This Work	[256 - 400]	12	100	3000	95.9%	92.3%	0.83

Only experimental results. [1] Switches + diodes.

† Power density calculated considering the full external case volume of the sealed converter.



(a)



(b)

FIGURE 10. Experimental results: (a) Input voltage: V_{HV} (CH1) and output voltage: V_{LV} (CH2), output current of modules 1 and 2: *Iout*_1 (CH3) and *Iout*_2 (CH4); (b) Transformer voltage: V_{pri_1} (CH1) and V_{pri_2} (CH2). Inductor current: $I_{L\_1,1}$ (CH3) and $I_{L\_1,2}$ (CH4).

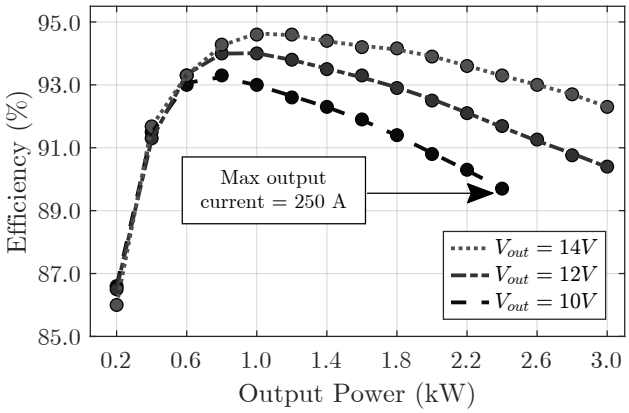


FIGURE 11. Efficiency curve. (V_{HV} = 400 V)

in Figure 11. The measurements were performed using a Yokogawa WT1800 precision power analyzer connected to both the input and output of the converter to accurately capture power losses. Notably, the highest efficiency is achieved when operating at an output voltage of 14 V, as the current through the circuit elements is lower at this voltage level compared to 12 V or 10 V. Under this operating condition, the converter reaches a peak efficiency of 94.6% at 1200 W. Another critical point is that, at 10 V, the converter operates up to an output power of 1250 W, as it is limited to a maximum output current of 125 A.

The converter exhibits its highest performance under partial-load conditions, particularly around 1.25 kW. This behavior occurs because, at this operating point, conduction losses are not yet dominant, as the current through the converter remains moderate compared to full-load operation. At the same time, magnetic and switching losses, represent a smaller percentage of the total power processed. Consequently, in this intermediate power region, the converter achieves its optimal efficiency, confirming the effectiveness of the proposed HB-CD topology for light- and medium-load conditions typically found in EV auxiliary systems.

Figure 12 presents the efficiency results for an output voltage of 14 V and an input voltage of 256 V. The measurements were obtained under the same test setup and instrumentation described previously. This operating point represents a maximum duty cycle condition for the converter. Under these conditions, the converter achieves a maximum

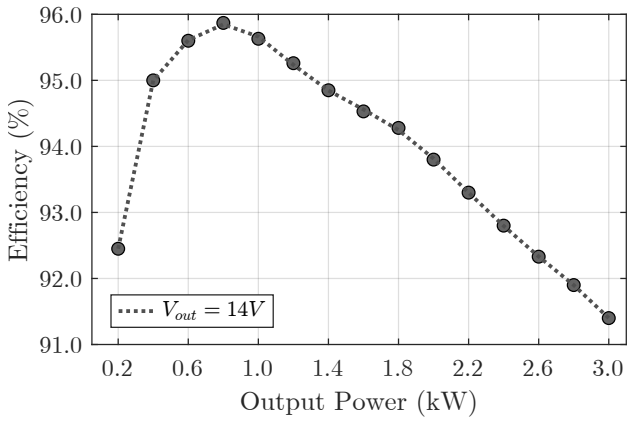


FIGURE 12. Efficiency curve. (V_{HV} = 256 V)

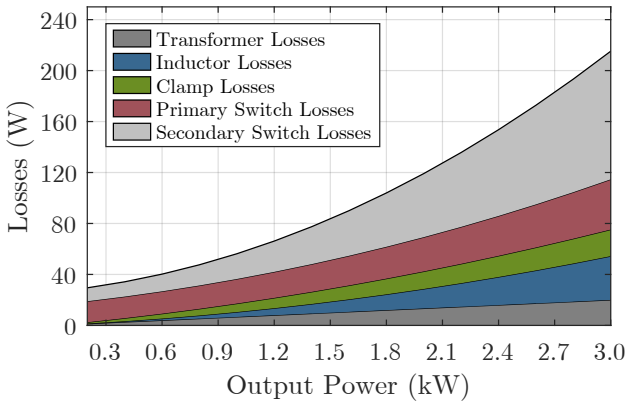


FIGURE 13. Contribution of losses by device. Condition: V_{HV} = 400 V and V_{LV} = 14 V.

efficiency of 95.9% at 800 W, which is higher than in nominal operation. This improvement in peak efficiency is due to the reduced voltage across the primary-side semiconductors when the input voltage is low, which lowers switching losses. Additionally, when reflected to the secondary side, the lower primary-side voltage reduces voltage across the secondary switch, thereby decreasing losses due to parasitic capacitances that would otherwise cause voltage spikes on the switches [26]. This reduction in secondary-side losses further enhances efficiency. However, with increasing output power, the primary and secondary currents also increase, leading to a more pronounced efficiency reduction than under nominal operating conditions.

Figure 13 presents the loss breakdown analysis for entire power range. The losses are categorized into transformer, inductor, snubber, and losses in the primary and secondary switches. It is observed that the secondary side losses are predominantly due to conduction losses in the semiconductors.

A comparison of various works from the literature is presented in Table 2. It is noticeable that, despite the variation in the power range of some prototypes and products, few works achieve an efficiency above 95%. Therefore, the efficiency achieved in this prototype reaches the typical industrial and academic experimental results.

V. CONCLUSION

This paper presented the design and experimental validation of an APM based on an HB-CD topology for EV applications. The proposed converter addresses challenges such as high output current, ripple mitigation, and conduction loss reduction.

The generalized structure supports parallel operation of converter modules, enabling ripple attenuation and current stress relief. Among the configurations, the interleaved two-module setup proved optimal in balancing performance and design simplicity.

A 3 kW prototype with two 1.5 kW modules confirmed the expected behavior, showing balanced current sharing, phase-shifted operation, and high efficiency, reaching 94.6% at 12 V/250 A and 95.9% under minimum input voltage conditions.

ACKNOWLEDGMENT

The authors thank the support provided by CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico), project 405061/2023-4. Furthermore, this work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior—Brasil (CAPES/PROEX)—Finance Code 001.

AUTHOR'S CONTRIBUTIONS

P.H.B.LÖBLER: Conceptualization, Investigation, Methodology, Software, Validation, Writing – Original Draft. **W.G.R.VOLZ:** Formal Analysis, Validation, Visualization, Writing – Review & Editing. **A.TOEBE:** Investigation, Resources, Software, Validation, Writing – Review & Editing. **C.RECH:** Project Administration, Supervision, Writing – Review & Editing. **L.SCHUCH:** Funding Acquisition, Project Administration, Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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