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Modeling and Control of a Bipolar DC-DC Boost Converter for Bipolar DC Microgrids

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ABSTRACT Bipolar direct current (DC) microgrids have emerged as a promising alternative for efficiently integrating of renewable energy sources. However, these systems are susceptible to voltage imbalance between the positive and negative poles, especially with asymmetric loads. This paper presents the modeling and control of a non-isolated DC–DC Boost converter with a symmetric bipolar output suitable for photovoltaic applications. The proposed topology eliminates issues related to voltage imbalance and leakage currents while providing continuous low-ripple input current, a reduced number of components, simplified operation, and common grounding with the output neutral point. The operating principle, modeling, and control strategy of the converter are discussed, and its performance is validated through simulations and experimental results from a 1500 W prototype. The results demonstrate stable operation under both balanced and unbalanced conditions.

KEYWORDS DC microgrids, non-isolated, renewable energy sources, symmetrical bipolar output.

I. INTRODUCTION

The growing demand for sustainable energy sources has driven the development of technologies based on renewable resources, with an emphasis on solar energy. This transition seeks to mitigate the scarcity of natural resources and reduce environmental impacts, such as greenhouse gas emissions and climate change. In this scenario, direct current (DC) microgrids have established themselves as a promising alternative to conventional alternating current (AC) systems, especially in contexts involving the integration of renewable sources, such as photovoltaic (PV) generation, energy storage systems, LED lighting, and electric vehicles (EV). The growing interest in these architectures comes from the several advantages associated with DC microgrids, including higher efficiency, simpler control, high reliability, and better compatibility with DC loads and sources. As a result, their adoption has expanded to a wide range of applications, including data centers, commercial buildings, and industrial facilities [1]–[10].

Fig. 1 (a) shows the configuration of a bipolar DC microgrid, composed of three voltage lines: positive (P), neutral (Z), and negative (N) [1]. The power distribution in DC microgrids can be classified as monopolar or bipolar. Monopolar architectures operate with a single voltage level, whereas bipolar ones use two voltage levels ($+V_{DC}$ and $-V_{DC}$). The bipolar architecture stands out for its versatility, being particularly advantageous for supplying high-

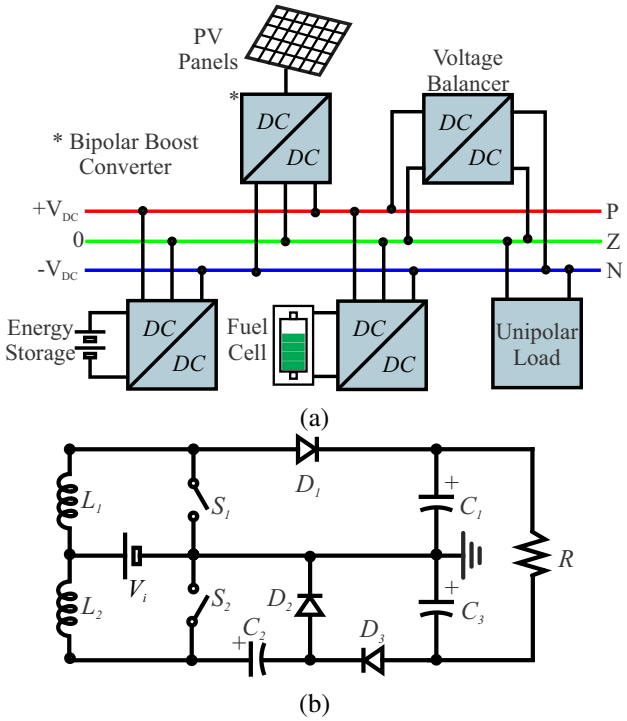

FIGURE 1. Bipolar DC microgrid: (a) Interconnection block diagram and (b) Non-isolated bipolar Boost converter.

power loads and providing greater operational flexibility to the system [10]–[12]. For efficient management of bipolar microgrids, DC-DC converters play a fundamental role, acting in voltage regulation and conversion between different voltage levels. Among the widely studied topologies, non-isolated converters stand out for presenting greater efficiency, smaller volume, and reduced cost compared to solutions with galvanic isolation [9], [11]. However, the lack of isolation can introduce undesirable effects, such as leakage currents and common-mode voltages, compromising power quality and system safety. To mitigate such problems, the literature has proposed the use of innovative topologies and advanced control strategies [3], [9], [13]–[15].

Despite their advantages, bipolar systems are susceptible to voltage imbalance between the positive and negative poles, usually caused by asymmetries in connected loads, sources, or storage units. As a more efficient solution, DC-DC converters with symmetrical bipolar outputs stand out, which, in addition to performing voltage conversion, contribute to the dynamic balancing of the microgrid without the need for additional components. Furthermore, dedicated voltage balancers can be integrated into DC microgrids to mitigate or eliminate bus voltage imbalances, thus improving system stability and performance [3], [16]–[19].

In recent years, several non-isolated bipolar DC–DC converter structures have been proposed not only to mitigate voltage imbalance, but also to improve the dynamic behavior of bipolar DC microgrids. The authors in [12] proposed a SEPIC–Cuk combination for bipolar DC microgrids using a single ground-referenced switch, experimentally validating the steady-state operation under basic PWM voltage regulation. The authors in [20] extended the Cuk–SEPIC concept with coupled inductors for PV systems, integrating MPPT and current/voltage controllers, but without a detailed state-space model or closed-loop dynamic analysis of the bipolar bus. In [21], the authors presented a Zeta–Buck–Boost SIMO converter with bipolar output and a single controllable switch, evaluating different operating modes under classical cascaded control. The authors in [22] applied the voltage-lift technique to a transformerless double-output converter, emphasizing reduced control complexity compared with transformer-based solutions while focusing mainly on voltage-gain characteristics. A dual-output high-gain converter with self-balancing bipolar voltages for DC microgrids was introduced in [23], prioritizing static gain and efficiency over a rigorous dynamic control design. Finally, the authors in [24] discussed a general family of three-level DC–DC converters and proposed a feedforward scheme to balance intermediate capacitor voltages, providing important insights but not a dedicated modeling and control framework for a non-isolated bipolar boost stage. Overall, these contributions concentrate on proposing new topologies and basic regulation schemes, whereas a detailed state-space averaged model, systematic control design, and experimental validation specifically oriented to the dynamic voltage regulation of a non-isolated bipolar boost converter remain comparatively less explored, which motivates the approach adopted in this work.

Considering this scenario, this work addresses the modeling and control of a non-isolated DC-DC Boost converter with symmetrical bipolar output, primarily intended for photovoltaic systems. By incrementing a bidirectional stage, the same structure can also be adapted for applications with other sources, such as energy storage systems and fuel cells. The adopted topology, shown in Fig. 1 (b), eliminates problems related to voltage unbalance and leakage currents, presenting continuous input current with low ripple, reduced number of components, simplified operation and common grounding with the output neutral point. This paper is organized as follows: Section II presents the structure and operational concept of the converter. Section III presents the modeling and control. Section IV presents the simulation and experimental results. Finally, the conclusion is presented in Section V.

II. DESCRIPTION OF THE DC-DC CONVERTER

To mitigate voltage unbalance in bipolar DC microgrids, the converters used must be capable of injecting power into both poles, thus balancing the bus voltages. Thus, the evaluated converter has two voltage outputs, V_{C1} and V_{C3}, allowing balanced energy injection into both poles of the microgrid. This configuration contributes to the self-balancing of the output voltage, dispensing with auxiliary circuits; however, with the help of voltage balancers, it is possible to ensure even more precise and stable.

The topology has several advantages, such as low input current ripple, fewer components, simple and efficient operation, and low stress on the semiconductors. The adopted bipolar strategy also reduces the leakage current, enabling the direct connection of the panel grounding to the AC grid neutral, complying with the IEC 62109-2 standard [25]. The circuit consists of two inductors (L_1, L_2), two switches (S_1, S_2), three diodes (D_1, D_2, D_3) and three capacitors (C_1, C_2, C_3).

In this section, the operating principle of the DC-DC converter is presented, together with the equations that describe its operation and the main associated waveforms.

A. PRINCIPLE OF OPERATING

The operation of the DC-DC converter with an equivalent resistive load is described as follows. To simplify the analysis, the following assumptions are made: 1) All semiconductors are considered ideal and lossless. 2) The input voltage source is assumed to be ideal, denoted by V_i. 3) All capacitors are sufficiently large so that their voltages are considered constant values. 4) An intrinsic resistance R_{D3} is included to dampen the current through diode D_3. 5) The converter operates in continuous conduction mode (CCM). The converter operation can be divided into two distinct stages over a switching period (Fig. 2). In the first stage, switches S_1 and

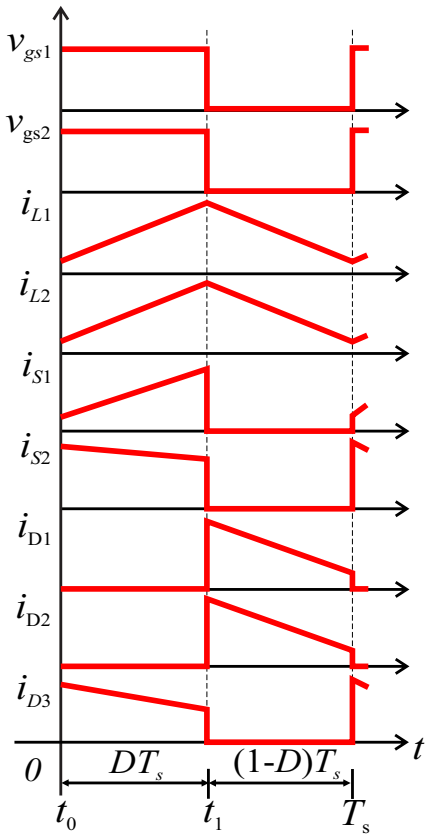

FIGURE 2. Typical waveforms of the proposed converter.

S_2 are turned on, and in the second stage, they are turned off. Additionally, the equivalent circuits corresponding to these operating modes are shown in Fig. 3.

1) **First stage** ($t_0 < t < t_1$) [Fig. 3 (a)]: In this stage, switches S_1 and S_2 are in conduction, allowing inductors L_1 and L_2 to be directly magnetized by input voltage V_i. As a result, the inductor currents increase linearly. Diodes D_1 and D_2 remain reverse-biased, while diode D_3 conducts. Capacitors C_1, C_2, and C_3 supply power to the load. The inductor currents in this stage are given by:

$$i_{L1}(t) = \frac{V_i}{L_1}(t) + i_{L1}(t_0) \tag{1}$$

$$i_{L2}(t) = \frac{V_i}{L_2}(t) + i_{L2}(t_0) \tag{2}$$

2) **Second stage** ($t_1 < t < T_s$) [Fig. 3 (b)]: In this stage, switches S_1 and S_2 are turned off. Inductors L_1 and L_2 are demagnetized, transferring energy to capacitors C_1 and C_2 through diodes D_1 and D_2, now forward biased. Diode D_3 is blocked. The voltages applied to the inductors are $V_{L1} = V_i - V_{C1}$ and $V_{L2} = V_i - V_{C2}$, which causes their currents to decrease according to:

$$i_{L1}(t) = \frac{V_i - V_{C1}}{L_1}(t) + i_{L1}(t_1) \tag{3}$$

$$i_{L2}(t) = \frac{V_i - V_{C2}}{L_2}(t) + i_{L2}(t_1) \tag{4}$$

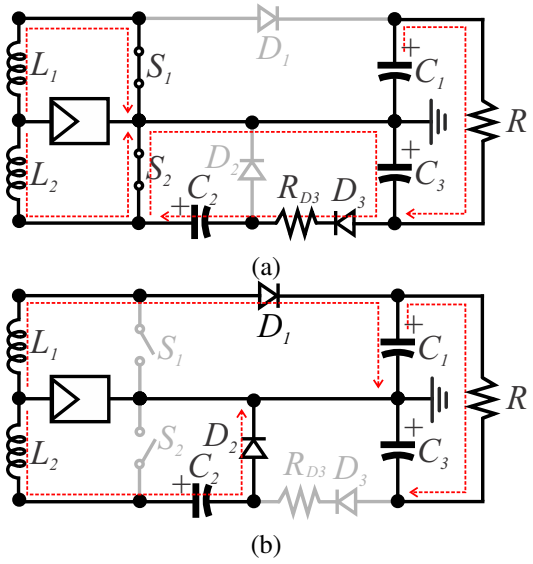

FIGURE 3. Operation stages. (a) First stage. (b) Second stage.

B. IDEAL STATIC VOLTAGE GAIN

In the steady state, by applying the volt-second balance to the inductors L_1 and L_2, respectively, the voltage gain can be obtained by:

$$\langle V_L \rangle = \frac{1}{T_s}\int_0^{T_s} [V_{L1}(t) + V_{L2}(t)]\, dt = 0 \tag{5}$$

Considering that V_{C2} = V_{C3}, and knowing that the output is bipolar, that is, the capacitors are stacked, then the output voltage V_o is given by the sum of the output capacitances:

$$V_o = V_{C1} + V_{C3} \tag{6}$$

Since the voltage of the capacitors is:

$$V_{C1} = V_{C2} = V_{C3} = \frac{V_i}{1-D} \tag{7}$$

Therefore the static gain of the converter is given by:

$$M = \frac{V_o}{V_i} = \frac{2}{1-D} \tag{8}$$

C. DESIGN OF INDUCTORS AND CAPACITORS

The design equation for inductors L_1 and L_2 is given by [26]:

$$L_1 = L_2 = \frac{V_i}{2\Delta i_L f_s} D \tag{9}$$

where V_i is the input voltage, Δi_L is the peak-to-peak inductor current ripple, f_s is the switching frequency, and D is the duty cycle.

And the design of capacitors C_1, C_2, and C_3 are given by [26]:

$$C_1 = C_2 = C_3 = \frac{\Delta i_o}{\Delta V_o f_s} \tag{10}$$

where Δi_o is the peak-to-peak output current ripple and ΔV_o is the peak-to-peak output voltage ripple.

III. MODELING AND CONTROL

Based on the analysis of the evaluated topology, the mathematical model of the converter and the control strategy appropriate to its operation are developed. In addition, the stability of the control system is evaluated under parametric variations, using the Routh–Hurwitz criterion and Lyapunov's direct method, demonstrating the robust performance of the bipolar DC–DC converter.

A. MODELING

The modeling is based on operation in two distinct stages, defined by the state of the switches.

The first stage of operation (Fig. 3 (a)) occurs when the switches are in conduction ($t_0 < t < t_1$). The differential equations that describe the dynamic behavior of the converter in this stage are:

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{1}{L_1}\, V_i = \dot{i_{L1}} \tag{11}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{1}{L_2}\, V_i = \dot{i_{L2}} \tag{12}$$

$$\frac{\mathrm{d}V_{C1}}{\mathrm{d}t} = \frac{1}{C_1}\left[-\frac{V_{C1}}{R} - \frac{V_{C3}}{R}\right] = \dot{V_{C1}} \tag{13}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\left[\frac{V_{C3}}{R_{D3}} - \frac{V_{C2}}{R_{D3}}\right] = \dot{V_{C2}} \tag{14}$$

$$\frac{dV_{C3}}{dt} = \frac{1}{C_3}\left[-\frac{V_{C1}}{R} - \frac{V_{C3}}{R} - \frac{V_{C3}}{R_{D3}} + \frac{V_{C2}}{R_{D3}}\right] = \dot{V_{C3}} \tag{15}$$

The second stage of operation (Fig. 3 (b)) occurs when the switches are off ($t_1 < t < T_s$). The dynamic equations in this condition are as follows:

$$\frac{\mathrm{d}i_{L1}}{\mathrm{d}t} = \frac{1}{L_1}\,[V_i - V_{C1}] = \dot{i_{L1}} \tag{16}$$

$$\frac{\mathrm{d}i_{L2}}{\mathrm{d}t} = \frac{1}{L_2}\,[V_i - V_{C3}] = \dot{i_{L2}} \tag{17}$$

$$\frac{\mathrm{d}V_{C1}}{\mathrm{d}t} = \frac{1}{C_1}\left[i_{L1} - \frac{V_{C1}}{R} - \frac{V_{C3}}{R}\right] = \dot{V_{C1}} \tag{18}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}\,[i_{L2}] = \dot{V_{C2}} \tag{19}$$

$$\frac{dV_{C3}}{dt} = \frac{1}{C_3}\left[-\frac{V_{C1}}{R} - \frac{V_{C3}}{R}\right] = \dot{V_{C3}} \tag{20}$$

The state vector is defined as $x = \begin{bmatrix} i_{L1} & i_{L2} & V_{C1} & V_{C2} & V_{C3} \end{bmatrix}^T$, containing the inductor currents and capacitor voltages. The state-space model is then expressed by:

$$\begin{cases} \dot{x} = A_i x(t) + B_i u(t) \\ y = C_i x(t) + D_i u(t) \end{cases} \tag{21}$$

where $i = 1$ refers to the first stage of operation (switches on) and $i = 2$ to the second stage (switches off). The matrices for each stage are:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1 R} & -\frac{1}{C_1 R} & 0 \\ 0 & 0 & -\frac{1}{C_3 R} & -(\frac{1}{C_3 R} + \frac{1}{C_3 R_{D3}}) & \frac{1}{C_3 R_{D3}} \\ 0 & 0 & 0 & \frac{1}{C_2 R_{D3}} & -\frac{1}{C_2 R_{D3}} \end{bmatrix} \tag{22}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{23}$$

$$C_1 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{24}$$

$$D_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{25}$$

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C1} & 0 & -\frac{1}{C_1 R} & -\frac{1}{C_1 R} & 0 \\ 0 & 0 & -\frac{1}{C_3 R} & -\frac{1}{C_3 R} & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 \end{bmatrix} \tag{26}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{27}$$

$$C_2 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{28}$$

$$D_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{29}$$

From the equations obtained in the modeling and using the parameters specified in Table 1, it is possible to determine the transfer function that relates the inductor current i_{L1} to

TABLE 1. DC-DC converter design parameters

Parameters	Value
Input voltage (V_i)	136 V
Output voltage (V_{C1}, V_{C3})	400 V
Duty cycle (D)	0.67
Output power (P_o)	1500 W
Switching frequency (f_s)	50 kHz
Capacitors (C_1, C_2, C_3)	27 μF (700 V, film)
Inductors (L_1, L_2)	500 μH (149.2 mΩ / 149 mΩ)
Diodes (D_1, D_2, D_3)	FFSH2065A (650 V / 20 A / 1.5 V)
Switches (S_1, S_2)	STW48N60DM2 (600 V / 40 A / 0.065 Ω)

the duty cycle, by linearizing the small-signal AC model, expressed by:

$$G_{iL1-u} = \frac{a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5}{b_1 s^5 + b_2 s^4 + b_3 s^3 + b_4 s^2 + b_5 s + b_6} \tag{30}$$

where: $a_1 = 5.44 \times 10^5$, $a_2 = 2.01 \times 10^{11}$, $a_3 = 7.5 \times 10^{13}$, $a_4 = 1.8 \times 10^{18}$, $a_5 = 6.9 \times 10^{20}$, $b_1 = 1$, $b_2 = 3.7 \times 10^5$, $b_3 = 8.8 \times 10^7$, $b_4 = 1.02 \times 10^{13}$, $b_5 = 9.7 \times 10^{14}$, $b_6 = 6.3 \times 10^{19}$.

The model validation is performed by comparing the behavior of the linear model with the simulated converter when both are subjected to the same input conditions. Applying to the plant obtained by modeling, a step of 0.02 in the duty cycle, in the time of 0.2 seconds, as shown in Fig. 4 (a). Similarly, a step of -0.02 was applied in 0.2 seconds, shown in Fig. 4 (b). The results demonstrate that the mathematical model accurately represents the dynamic behavior of the converter under duty cycle perturbations, capturing its transient response despite minor oscillations, thereby validating its suitability for control design.

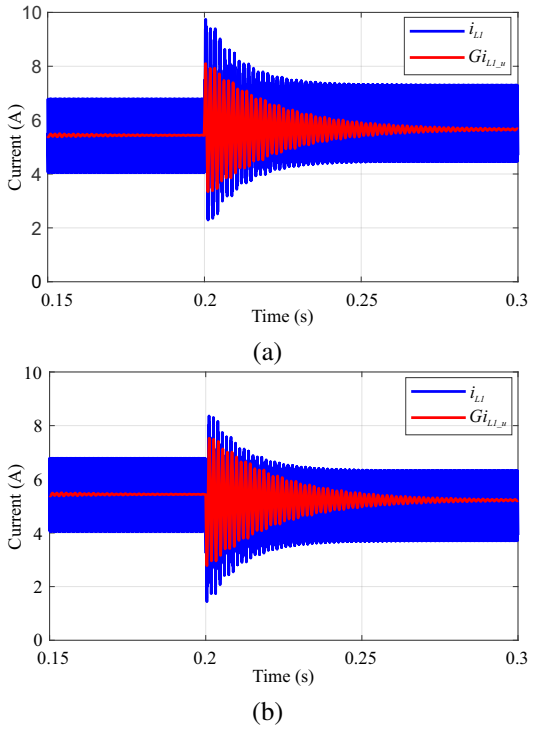

FIGURE 4. Model validation for duty-cycle variation: (a) $+0.02$ step and (b) -0.02 step.

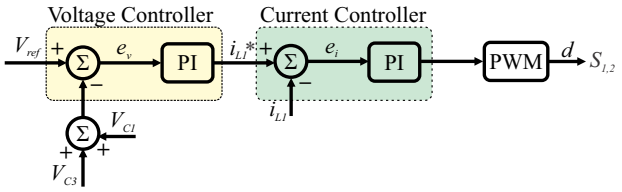

FIGURE 5. Control structure used.

B. CONTROLLER DESIGN

Under unbalanced load conditions, the proposed converter keeps the bipolar voltages regulated without the need for an external voltage balancer. As the power demanded by one pole increases, the corresponding currents in the inductor and switch change, and the input currents in the inductor are redistributed, while the control system maintains the bus voltages close to their reference values, preserving the symmetry of the bipolar bus.

The bipolar boost converter control system aims to regulate the DC-bus voltage $V_o = V_{C1} + V_{C3}$ around a reference value V_{ref}. To achieve this objective, a control strategy based on proportional–integral (PI) controllers is adopted. The internal control loop, characterized by faster dynamics, regulates the inductor current, ensuring a rapid transient response. The external control loop, with slower dynamics, is responsible for regulating the output voltage, guaranteeing that the capacitor voltages remain balanced and constant under different operating conditions. Fig. 5 illustrates the block diagram of the adopted control strategy.

For the external voltage circuit, a PI compensator was implemented to increase the system gain at low frequencies and eliminate steady-state error. The controller was set with a cutoff frequency of approximately 50 Hz, which is low enough to avoid interaction with the converter's switching frequency (50 kHz) but high enough to ensure good dynamic regulation of the bus voltage. Fig. 6 shows the Bode diagram of the closed-loop voltage controller plant. The transfer function of the voltage controller is:

$$C_{Vo} = \frac{418.87\,(s + 300)}{s\,(s + 31420)} \tag{31}$$

For the internal current circuit, the goal is to ensure an accurate tracking of the inductor current reference. The crossover frequency was chosen a decade below the switching frequency, around 5 kHz. To achieve this, an integrator was introduced for zero steady-state error, and a zero was placed a decade below the crossover frequency, at approximately 500 Hz, to improve stability. Fig. 7 shows

the Bode diagram of the closed-loop current controller plant. The resulting transfer function is:

$$C_{L1} = \frac{0.040431(s + 3710)}{s} \tag{32}$$

C. STABILITY ANALYSIS

The closed-loop stability of the proposed system was evaluated using the linearized state-space model around the operating point. The corresponding characteristic equation can be expressed in the general form:

$$s^5 + c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0 = 0, \tag{33}$$

where the coefficients c_i are functions of the converter parameters and controller gains.

The *Routh–Hurwitz* criterion was applied to this fifth-order polynomial, which requires that all the elements of the first column of the *Routh* array be positive. The *Routh* array is given by:

$$\begin{array}{c|ccc} s^5 & 1 & c_3 & c_1 \\ s^4 & c_4 & c_2 & c_0 \\ s^3 & \dfrac{c_4c_3 - c_2}{c_4} & \dfrac{c_4c_1 - c_0}{c_4} & 0 \\ s^2 & A & B & 0 \\ s^1 & \dfrac{A\left(\dfrac{c_4c_1 - c_0}{c_4}\right) - Bc_4}{A} & 0 & 0 \\ s^0 & B & 0 & 0 \end{array} \tag{34}$$

where:

$$A = \frac{\left(\frac{c_4c_3 - c_2}{c_4}\right)c_2 - c_4\left(\frac{c_4c_1 - c_0}{c_4}\right)}{\frac{c_4c_3 - c_2}{c_4}} \tag{35}$$

$$B = \frac{A\left(\frac{c_4c_1 - c_0}{c_4}\right) - 0}{A} \tag{36}$$

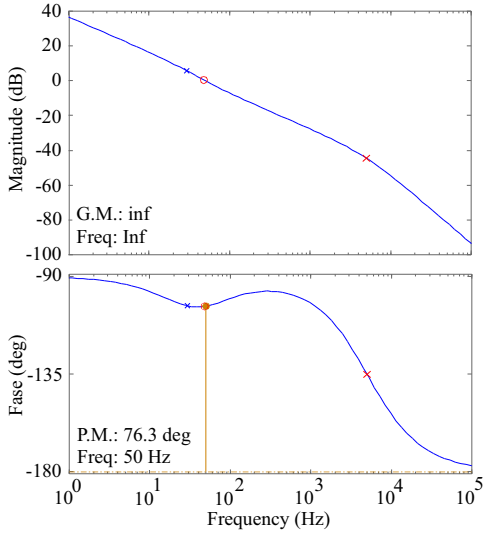

FIGURE 6. Bode for closed loop plant: voltage controller.

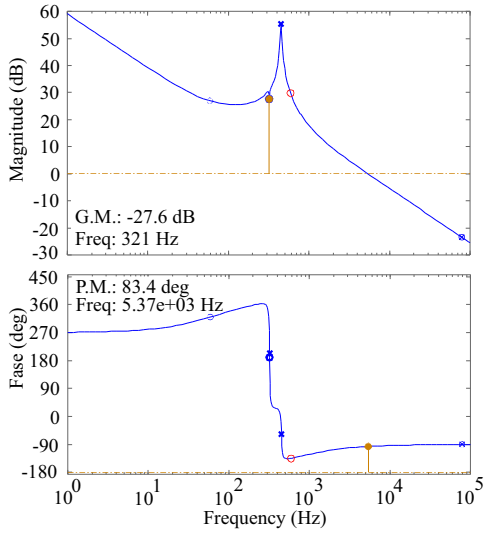

FIGURE 7. Bode for closed loop plant - current controller.

The conditions for stability are then:

$$\begin{aligned} &c_4 > 0, \quad \frac{c_4c_3 - c_2}{c_4} > 0, \quad A > 0, \\ &\frac{A\left(\frac{c_4c_1 - c_0}{c_4}\right) - Bc_4}{A} > 0, \quad B > 0. \end{aligned} \tag{37}$$

These requirements were verified for the nominal design parameters, confirming that the system is stable.

To investigate robustness, parametric variations of $\pm 20\%$ were applied to L_1, L_2, C_1, C_2, and C_3, as well as a 50% variation in load. The pole distribution obtained under these variations is shown in Fig. 8, where all poles remain in the left half-plane. The dominant poles maintain sufficient damping, and no migration to the unstable region was observed, confirming robust stability.

The stability margins were also quantified. The minimum damping ratio observed was $\zeta_{\text{min}} = 0.15$, while the minimum

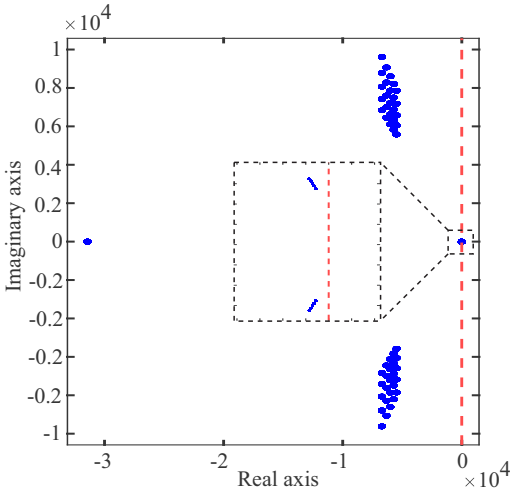

FIGURE 8. Pole distribution for ±20% components variations at 50% load.

phase margin was $PM_{\text{min}} = 42°$. Additionally, the gain margin remained above 6 dB in all tested conditions. These values, although reduced compared to the nominal case, still guaranty satisfactory transient performance. Therefore, the combined use of the *Routh–Hurwitz* criterion, pole distribution analysis, and margin quantification demonstrates that the proposed control strategy provides stable operation and robust performance even under significant parameter deviations and load variations.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To evaluate the performance of the proposed converter and control system, simulation and experimental analyses were performed using a 1.5 kW prototype, as shown in Fig. 9. The simulations were carried out in the PSIM software, and the parameters listed in Table 1 were used to obtain the results.

Fig. 10 (a) and (b) illustrate the system behavior when faced with a load step from 100 % to 50 % of nominal power, applied at $t = 0.25$ s. It can be observed that the total output voltage (V_o) remained regulated at 800 V, even after the disturbance occurred. The maximum voltage drop was approximately 20 % of nominal voltage, and the recovery time to steady state was $t = 17$ ms. The inductor current L_1 follows the reference satisfactorily, evidencing the effectiveness of the internal current control loop.

Furthermore, Fig. 11 (a) and (b) show the system response to an inverse step, from 50 % to 100 % load, applied at $t = 0.25$ s. The output voltage remained at 800 V after the disturbance, with a dip of approximately 16.5 % of the nominal voltage and a settling time of approximately $t = 27$ ms. The inductor current again followed the reference with good accuracy, confirming the robustness of the control even under abrupt load variations.

Details of the DC-DC converter waveforms can be seen from top to bottom as follows: V_{S1}, V_{S2}, V_i and V_o in Fig. 12, V_{C1}, V_{C2} and V_{C3} in Fig. 13, i_i, i_{L1} and i_{L2} in Fig. 14,

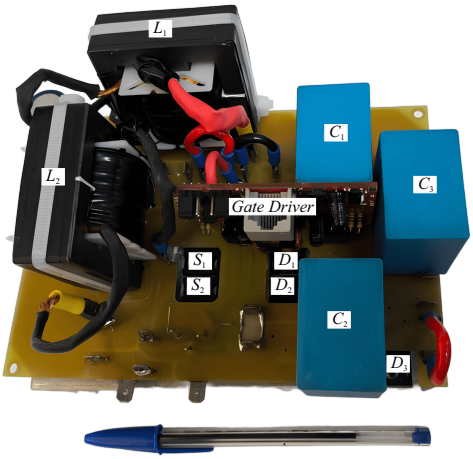

FIGURE 9. Prototype experimental circuit.

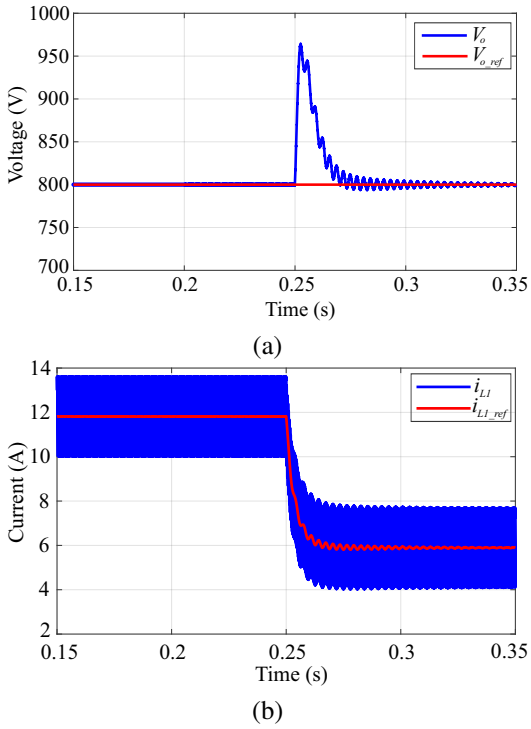

FIGURE 10. Load variation from 100% to 50%: (a) Output-voltage response and (b) Inductor-current response.

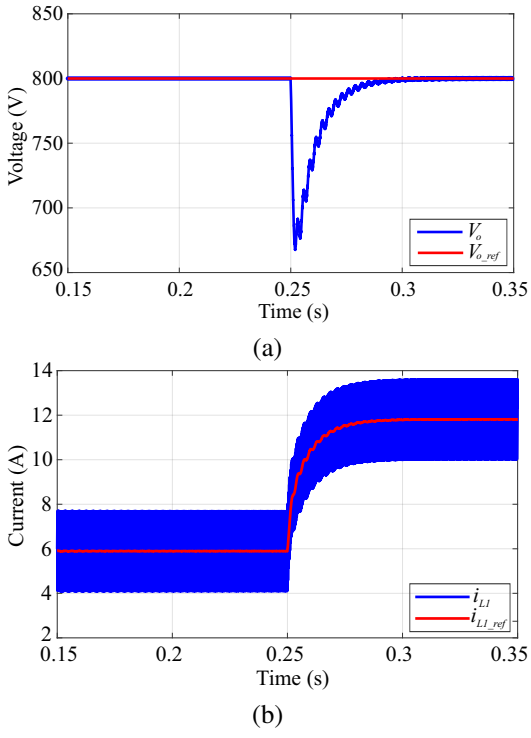

FIGURE 11. Load variation from 50% to 100%: (a) Output-voltage response and (b) Inductor-current response.

i_i, i_{S1} and i_{S2} in Fig. 15, respectively. The corresponding

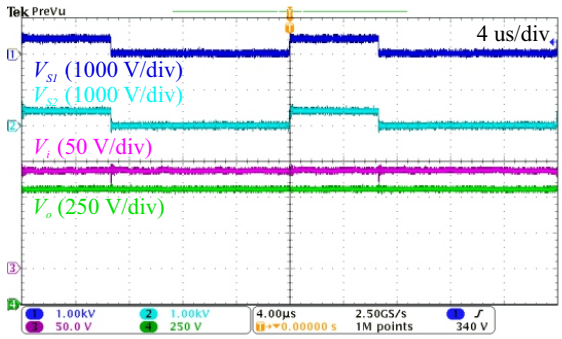

FIGURE 12. Voltages V_{S1} (1000 V/div), V_{S2} (1000 V/div), V_i (50 V/div) and V_o (250 V/div).

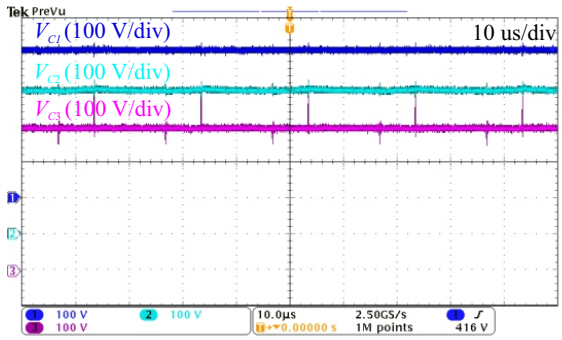

FIGURE 13. Voltages V_{C1} (100 V/div), V_{C2} (100 V/div) and V_{C3} (100 V/div).

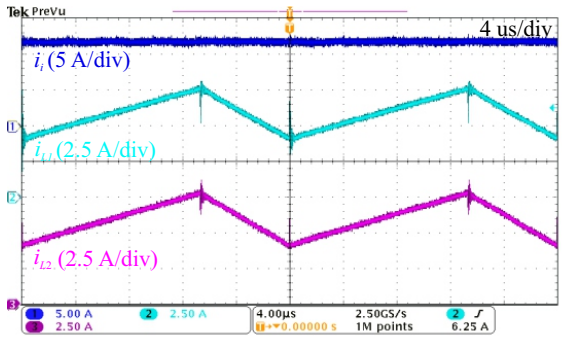

FIGURE 14. Currents i_i (5 A/div), i_{L1} (2.5 A/div) and i_{L2} (2.5 A/div).

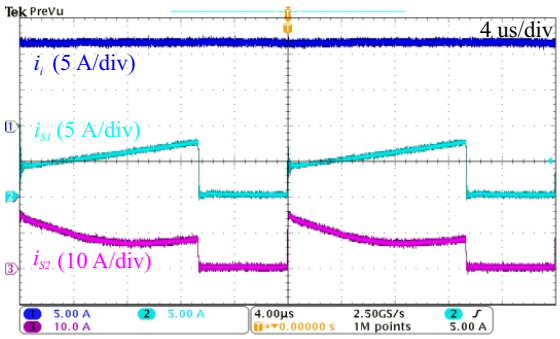

FIGURE 15. Currents i_i (5 A/div), i_{S1} (5 A/div) and i_{S2} (10 A/div).

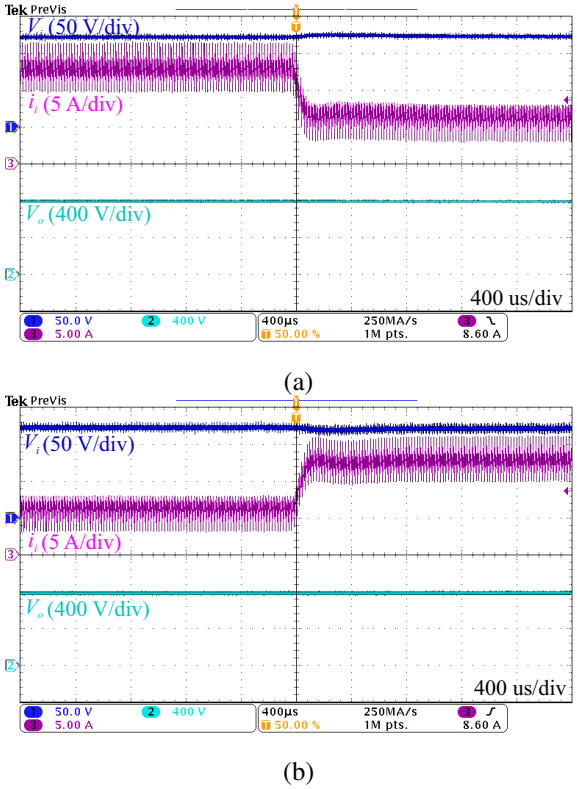

FIGURE 16. Waveforms: (a) Load step from 100 % to 50 % and (b) Load step from 50% to 100%.

voltages and currents are as follows: V_{S1} = 400 V, V_{S2} = 400 V, V_i = 136 V and V_o = 800 V, V_{C1} = 400 V, V_{C2} = 400 V, V_{C3} = 400 V, i_i = 11.2 A, i_{L1} = 5.6 A, i_{L2} = 5.6 A, i_{S1} = 5.6 A and i_{S2} = 8 A. Furthermore, it is noted that the inductor current is in CCM, as expected, ensuring low ripple and stable operation, and the capacitor voltages are balanced around 400 V.

Fig. 16 (a) and (b) show the experimental load step tests. In the first case, the load was reduced from 100% to 50% and then increased again from 50% to 100%. In both situations, the bus voltage quickly recovered after the disturbance and the control maintained the system stable, corroborating the results obtained in the simulation. Fig. 17 shows the unbalanced load test, where a 450 W load was connected to the positive pole and a 750 W load to the negative pole. Even with this asymmetry, the capacitor voltages remained balanced at 400 V, validating the topology's ability to maintain pole symmetry without the need for auxiliary circuits.

Fig. 18 and 19 show disturbances applied to the input of the converter. In Fig. 18 (a) and (b), the input voltage was varied from 100 V to 136 V and then from 136 V to 100 V, while in Fig. 19 (a) and (b) the input current was stepped from 8 A to 11 A and from 11 A to 8 A. In both cases, the bus voltage remained stable, demonstrating the robustness of the control against source disturbances.

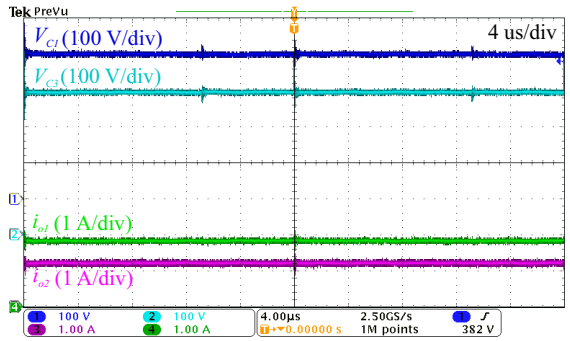

FIGURE 17. Results unbalanced load test.

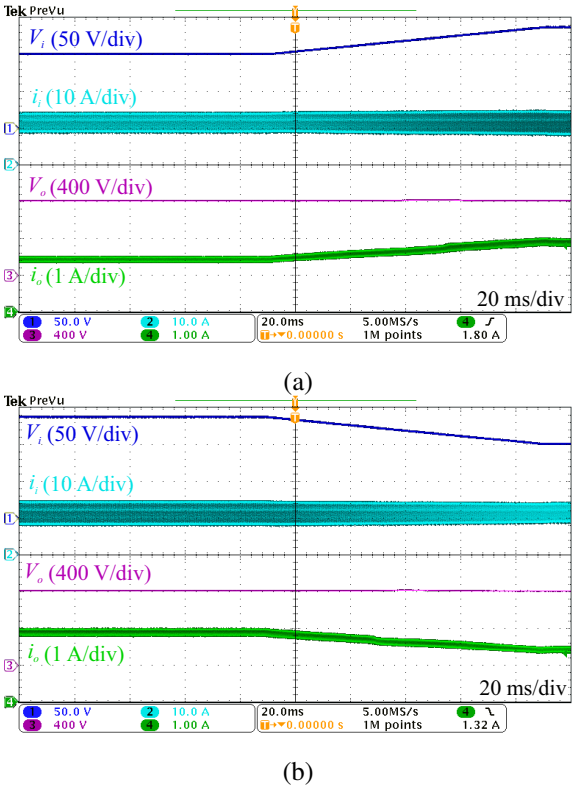

FIGURE 18. Waveforms: (a) Input voltage step from 100 V to 136 V and (b) Input voltage step from 136 V to 100 V.

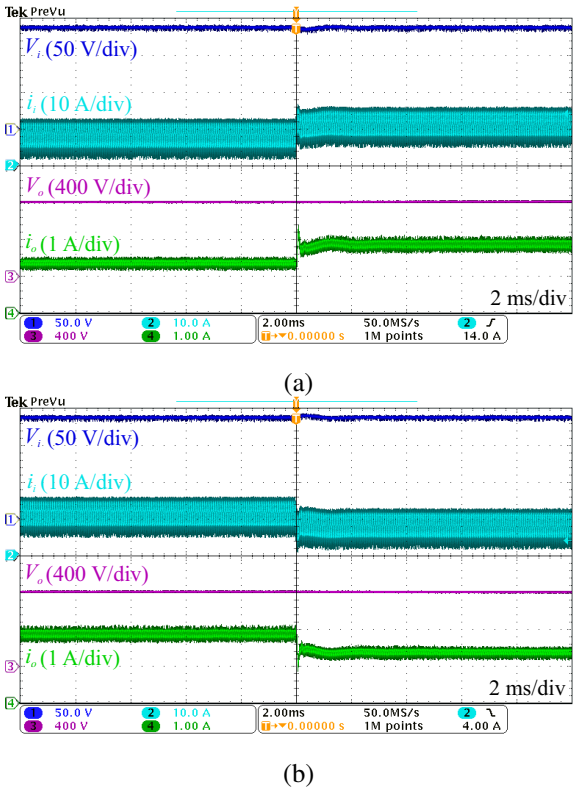

FIGURE 19. Waveforms: (a) Input current step from 8 A to 11 A and (b) Input current step from 11 A to 8 A.

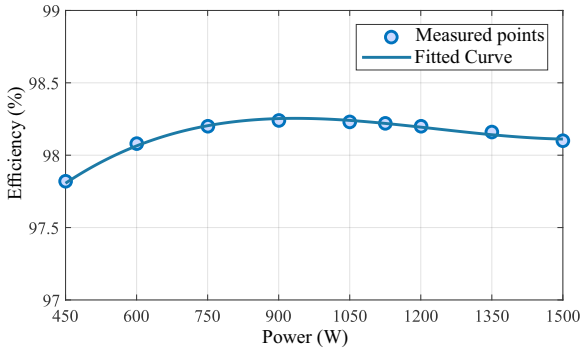

FIGURE 20. DC-DC converter efficiency.

Finally, Fig. 20 shows the converter's efficiency curve. The prototype achieved efficiency above 98%, remaining above 97% throughout almost the entire operating range. It can be seen that under light load conditions, semiconductor losses become more significant, reducing efficiency, while near nominal power, conduction and switching losses become more significant.

V. CONCLUSION

This paper presented the modeling, control, and validation of a non-isolated DC-DC Boost converter with symmetrical bipolar output, suitable for applications in photovoltaic systems, energy storage, and fuel cells. The proposed topology offers low input current ripple, simplified operation, and reduced component count, while contributing to voltage self-balancing in bipolar DC microgrids without the need for auxiliary circuitry. A mathematical model was developed and used to design an efficient two-loop control strategy. Simulation and experimental results obtained from a 1500 W prototype confirmed the converter's dynamic performance and voltage balancing capability under load variations, demonstrating its viability for practical applications.

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AUTHOR'S CONTRIBUTIONS

M.B.VENDRUSCOLO: Data Curation, Formal Analysis, Investigation, Methodology, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **A.TOEBE:** Investigation, Methodology, Validation, Writing – Review & Editing. **E.MATTOS:** Methodology, Supervision, Writing – Review & Editing. **L.MICHELS:** Methodology, Supervision, Writing – Review & Editing. **A.M.S.S.ANDRADE:** Conceptualization, Methodology, Project Administration, Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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