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Feasibility Implementation Analysis of the Parks-McClellan Algorithm in Capacitor Voltage Active Damping

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ABSTRACT This paper presents an analysis of the computational implementation of capacitor-voltage-based active damping (CVAD) for mitigating the resonance of LCL filters in power electronic converters based on Parks–McClellan (PM) FIR differentiator. The proposed approach relies on capacitor voltage feedback, eliminating the need for additional current sensors while ensuring both active damping and synchronization. The FIR differentiator, designed with the PM algorithm, emulates the derivative with low noise amplification and minimal phase delay, enabling effective resonance attenuation over a wide frequency range. The study addresses the implementation of the algorithm and provides a critical review of its applicability in conventional single-core and dual-core digital signal controllers, such as the TMS320F28335 and TMS320F28379D. Experimental validation on a single-phase grid-connected inverter demonstrates the effectiveness of the method in suppressing LCL resonance, highlighting its processing rate, feasibility for different filter orders, and practical viability in commercially available Digital Signal Controllers (DSCs) for both academic and industrial applications.

KEYWORDS Active damping, digital differentiator, Parks-McClellan algorithm, implementation technique, digital signal controller.

I. INTRODUCTION

Power Electronic Converters (PECs), especially inverters, are commonly used in the interfacing between Distributed Energy Resources (DERs), energy storage units, and the electrical grid [1]–[3]. Such devices employ low-pass filters for coupling to the power grid, with the aim of attenuating harmonics arising from their switching process, in order to comply with Power Quality (PQ) recommendations and regulatory requirements [4]. A widely used passive structure is the LCL filter, as it ensures low cost and greater harmonic attenuation compared to L and LC filters. However, such structures exhibit a resonance peak that requires damping in order to prevent instability [5].

Moreover, grid conditions are to anomalies at the Point of Common Coupling (PCC), exhibiting variations in line impedance and Total Harmonic Distortion (THD) in its voltage. This makes it essential for the control strategy of the PEC to handle such conditions, as well as to mitigate the effects of resonance [6]. In light of these effects, the THD of the current injected into the grid is limited to a maximum of 5% under normal operating conditions, as specified by IEEE 1547 [7] and IEC-61727 [8].

In general, the instability arising from the LCL filter is mitigated through passive damping techniques, by inserting a physical resistive element, which leads to reduced converter efficiency, or by means of Active Damping (AD) [9]. AD methodologies emulate a virtual resistor and are generally classified into digital filter-based approaches and multi-loop control schemes. The former introduces zeros and poles to attenuate the filter's resonant frequency, such as in methods based on low-pass filters and Notch filters [10]. However, it exhibits sensitivity to parametric variations, requiring more sophisticated adaptive techniques to compensate for this limitation [11].

In multi-loop control, damping is achieved through the control of the system's state variables, such as the feedback of the grid-injected current, the inverter-side inductor current, and the current through the LCL filter capacitor [12]. These solutions offer high efficiency and robustness; however, they require additional measurements, which increase the cost and hardware complexity due to the need for extra sensors and the introduction of potential points of failure [5]. In this regard, the AD strategy based on the derivative of the capacitor voltage, i.e., Capacitor Voltage Active Damping (CVAD) has proven to be attractive due to the reduced instrumentation circuitry, as it uses the capacitor voltage both for the synchronization algorithm and AD [13]. However,

it brings along challenges related to the nature of digital differentiators, which tend to amplify noise [14].

Thus, it is essential to design a digital filter that emulates the derivative within the frequency range of interest, so that the capacitor current can be estimated through the derivative of its voltage, ensuring attenuation of the LCL filter's resonance peak and effective rejection of noise present in the capacitor voltage.

In the literature, the derivative effect is emulated through direct differentiation [14], Lead-Lag Compensators [15], High-Pass Filters (HPF) [16], Quadrature-Second-Order Generalized Integrator (Q-SOGI) [17], nonideal Generalized Integrator (nGI) [14], among others. Direct differentiation introduces significant phase delay and is affected by the sampling process, compromising its effectiveness across the entire frequency spectrum of the signal [14]. The HPF performs differentiation adequately; however, it introduces phase delay [18]. The Q-SOGI differentiator has a narrow operating range around the resonance frequency and is susceptible to losing its damping capability with variations in the grid impedance [19].

Among these options, the nGI has stood out as one of the best solutions for obtaining a highly accurate derivative to date [20]. Its capability has been validated in the context of estimating the capacitor current via the voltage derivative for active damping strategies. Further details and discussions can be found in [11], [14], [19] and are beyond the scope of this work. However, there are still gaps in the design of new differentiators aimed at emulating the ideal differentiator within specific frequency ranges, while offering good noise rejection capability, simplicity, low phase delay, and reduced computational cost, among other desirable features.

Despite these advantages, the practical implementation of the differentiator at high sampling frequencies in Digital Signal Controllers (DSCs) is limited by the high sampling rate required. In other words, the main challenge is that the higher the sampling frequency, the shorter the computation window available for executing system tasks. In dual-core architectures, this situation can be mitigated, as one CPU operates in high frequency while the second asynchronously executes complementary tasks at frequency switching. However, this flexibility is not available in commercial single-core-based inverters, imposing additional challenges and constraints on the implementation.

Thus, there is a gap in the literature regarding the development of studies, analyses, as well as code partitioning methodologies, highlighting the feasibility of implementing high-frequency differentiators on single-core platforms. Another key element lies in the detailed analysis of the computation times associated with control, synchronization, and protection routines, including the delays introduced throughout a sampling period.

In this context, an alternative CVAD technique based on the Parks-McClellan (PM) algorithm is proposed in [11], [13]. Through this methodology, it is possible to effectively estimate the capacitor current via the derivative of its voltage. To the best of the authors' knowledge, these studies do not address implementation aspects related to firmware performance, such as initialization routines, configuration, time base, data acquisition, value conversion, control laws, and protection mechanisms. Thus, unlike [11], [13], this paper emphasizes implementation-oriented aspects, particularly an appropriate partitioning strategy for algorithm implementation and a critical analysis of its applicability to conventional microcontrollers. Regarding [21], it is worth noting that active damping is not achieved through capacitor voltage feedback, but rather through either capacitor current feedback or the inclusion of a physical resistor in series with the capacitor.

Therefore, the main contribution of this paper is an expansion of [11] and [13], with a focus on developing a systematic methodology for implementing the PM-based differentiator family in microprocessor-based systems, which are commonly used in power electronics research. This methodology enables the inclusion of practical implementation discussions among the different options of the PM differentiator family, as well as the validation of the trade-off between theoretical performance and practical complexity imposed by the requirement to operate at high frequencies, above the converter switching frequency.

This paper is organized as follows: Section II presents a brief modeling of the PEC with an LCL filter and the differentiators used. The proposed methodology is presented in Section III, and Section IV details the development of the analysis, validated through Hardware-In-the-Loop (HIL) scenarios and experimental results. Conclusions are drawn in Section V.

II. SYSTEM DESCRIPTION

Fig. 1 shows the configuration of the single-phase grid-connected inverter accoupled to grid, that is modeled by its voltage source (v_g) and the equivalent impedance at the PCC, represented by $Z_g = sL_g$. The DER is connected to the DC bus, represented by a constant voltage source, ensuring a constant DC-link voltage V_{dc} at the power electronics interface. The LCL filter consists of an inductor L_1 on the converter side, a filter capacitor C_f, an inductor L_2 on the grid side. The parasitic resistances of the LCL filter are neglected in order to consider a worst-case scenario, since their inclusion does not significantly affect the dynamic behavior of the LCL filter [21].

The variable i_1 represents the output current on the inverter side, i_2 represents the output current on the grid side, and i_{Cf} represents the current through the filter capacitor C_f. The grid current is controlled, and the capacitor voltage, v_{Cf}, is measured for the CVAD and a Phase-Locked Loop (PLL) in order to ensure synchronization with the grid. In addition, taking into consideration the one-sampling computation and pulsewidth modulation (considered as a zero-order holder) delay [22], the total delay G_d is designated as (1), where T_s is the sampling period.

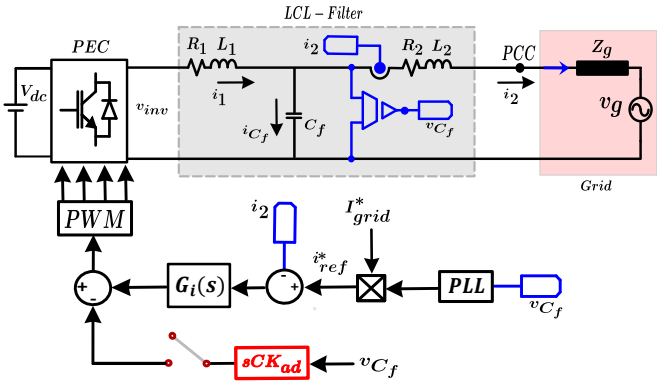

FIGURE 1. Schematic diagram of a PEC connected to the grid through an LCL filter.

$$G_d = e^{-1.5T_s s} \tag{1}$$

To avoid the need for an additional current sensor, i_{Cf} it is estimated from the derivative of v_{Cf}, as shown in Fig. 1, where K_{ad} is the damping gain and 's' is the differentiator based on a FIR filter, whose coefficients are obtained using the Parks-McClellan (PM) algorithm. The transfer function that relates the inverter output v_{inv} to the grid current i_2 is given in (2), where ω_r is the resonance frequency of the filter, expressed as shown in (3) [19].

$$G_{i2}(s) = \frac{i_2(s)}{v_{\text{inv}}(s)} = \frac{1}{L_T L_1 C_f\, s\,(s^2+\omega_r^2)} \tag{2}$$

$$\omega_r = \sqrt{\frac{L_1 + (L_2 + L_g)}{L_1(L_2 + L_g)C}} \tag{3}$$

As Fig. 2, the transfer functions relating v_{inv} to v_{Cf} and v_{inv} to $i_{Cf}(s)$ are given by (4) and (5), respectively [14].

$$G_{v_{Cf}}(s) = \frac{v_{Cf}(s)}{v_{\text{inv}}(s)} = \frac{1}{L_1 C_f\,(s^2+\omega_r^2)} \tag{4}$$

$$G_{i_{Cf}}(s) = \frac{i_{Cf}(s)}{v_{\text{inv}}(s)} = \frac{s}{L_1\,(s^2+\omega_r^2)} \tag{5}$$

To eliminate the steady-state error of the current at the fundamental frequency, ω_0, a Proportional-Resonant (PR) current controller, $G_i(s)$, is used, as described in (6), with a proportional gain K_p and a resonant gain K_i, given by (7) and (8), respectively [23].

$$G_i(s) = K_p + K_i \frac{sB_r}{s^2 + 2\zeta B_r s + \omega_r^2} \tag{6}$$

$$K_p = \frac{(2\xi+1)(\sqrt{2\xi+1})\,\omega_r L_{\text{eq}} - R_{\text{eq}}}{V_{\text{dc}}} \tag{7}$$

$$K_i = \frac{\omega_r^2 L_{\text{eq}}\left[(2\xi+1)^2 - 1\right]}{2V_{\text{dc}}} \tag{8}$$

where $L_{\text{eq}} = L_1 + L_2$, R_{eq} represents the sum of the resistances of the inductors in the LCL filter, ξ is the damping factor, ω_r is the angular resonance frequency, B_r is the resonant bandwidth in rad/s, and ζ is the damping factor of the resonant filter.

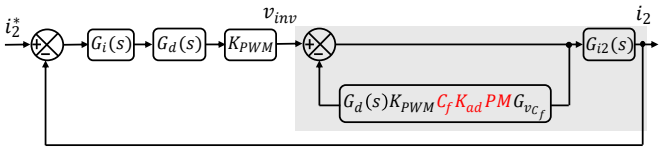

FIGURE 2. Block diagram of the control structure with CVAD for the PEC with an LCL filter.

According to [23], the value of B_r should be around 1.5 Hz, and ζ can take any value between 0.1 and 1, where $\zeta = 0.5$ causes the resonant filter to exhibit 0 dB at the resonance frequency. In contrast, ξ denotes the damping factor related to the PR controller design. Here, the PR controller was synthesized using the Naslin polynomial method, which requires specifying the damping factor ξ to shape the closed-loop system response. Further details on this method and on the PR controller design can be found in [23], [24], and the design of the damping gain K_{ad} has been extensively discussed in [25], and are therefore beyond the scope of this work.

It is important to highlight that, in the CVAD strategy, the derivative term $PM(z)$ is emulated by a 6th (PM6), 10th (PM10), and 20th (PM20) order FIR filter designed using the Parks-McClellan (PM) algorithm. Furthermore, the Parks-family differentiators of order $N = 6, 10$ and 20 are given by (9), with their coefficients listed in Table I, determined as described in [11].

$$PM(z) = \sum_{k=0}^{N} h_k\, z^{-k} \tag{9}$$

It should be noted that the phase response is influenced by the choice of sampling frequency: higher sampling frequencies are attractive as they allow for a wider stopband; however, they may also introduce additional complexity in the sampling process and increase the computational burden. Regarding the FIR filter order, previous studies have shown that orders up to 20 represent an effective trade-off between performance and implementation complexity. Additional information can be found in [11].

Finally, in practice, the digital derivative is emulated by different types of digital filters that reproduce its effect. However, these filters exhibit inherent characteristics that may introduce phase delay, improve noise immunity, increase computational cost, or even raise implementation complexity. With regard to the PM-based differentiator for a given sampling frequency, increasing the order of the PM-based differentiator generally leads to a higher phase delay.

III. PROPOSED METHODOLOGY

The differentiator based on the PM algorithm presents a trade-off between amplitude and phase shift. Although higher-order filters provide a more accurate approximation

TABLE 1. PM Coefficients.

Order	Coefficients PM (h_k)
$N = 6$	{ 0.0667, -0.1579, 0.3094, 0, -0.3094, 0.1579, -0.0667 }
$N = 10$	{ 0.0221, -0.0517, 0.0793, -0.1399, 0.3084, 0, -0.3084, 0.1399, -0.0793, 0.0517, -0.0221 }
$N = 20$	{ 0.00676, -0.00874, 0.001927, 0.003328, -0.0117405, 0.025037, 0.0456212, 0.0786987, -0.1399029, 0.30836821, 0, -0.3083683, 0.139903, -0.078699, 0.0456212, -0.025037, 0.011740, -0.003328, -0.001927, 0.0087412, -0.006762 }
$N = 30$	{ -0.001163, 0.002354, -0.002649, 0.003034, -0.002951, 0.002041, 0.000104, -0.003968, 0.010137, -0.019402, 0.032983, -0.053148, 0.085102, -0.144562, 0.310830, 0, -0.310830, 0.144562, -0.085102, 0.053148, -0.032983, 0.019402, -0.010137, 0.003968, -0.000104, -0.002041, 0.002951, -0.003034, 0.002649, -0.002354, 0.001163 }

of the magnitude response of an ideal differentiator, they introduce significant phase delay, which deteriorates the performance of the derivative estimation [13]. Since phase delay is more complex to compensate, amplitude errors can easily adjusted by tuning the firmware gain.

On the other hand, considering its digital implementation, the differentiator exhibits satisfactory performance when operated at a high sampling frequency (tens of kHz) [11]. Considering the definition of the interrupt routine, which is a mechanism where the processor's execution of its main loop is paused to handle a specific event without the need to constantly check for the occurrence of that event, the interrupt routine is an essential mechanism to ensure that signal acquisition, control, and parameter calculation routines, among others, are executed within the computation period defined in the design.

To evaluate the feasibility of implementing a high-frequency differentiator on single-core platforms, a methodology was developed that establishes the definition of the sampling frequency, the assessment of computation times, and the execution of control routines within the available period, following the design of the differentiators and the assessment of their performance through simulation and theoretical analysis (such as frequency response) [11]. This strategy enables the identification of processing limits and the establishment of criteria for the allocation of differentiation, control, and auxiliary routines, such as initialization, synchronization algorithm, among others.

Fig. 3 shows the flowchart for the implementation of a differentiator in a DSC, in which the proposed methodology can be briefly described in the following main steps:

1) Specify the differentiator order (N) and set the sampling frequency (f_s) according to the inverter switching frequency (f_{PEC}). In this work, a single-update modulation technique was adopted, according to (10).

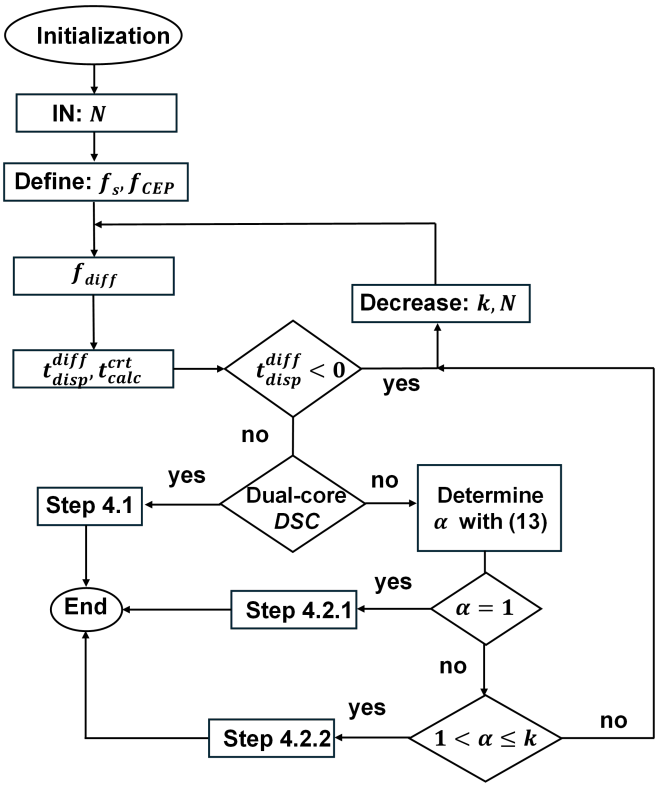

FIGURE 3. Flowchart for the implementation of a differentiator in a DSC.

$$f_s = f_{PEC} \tag{10}$$

2) Selection of the sampling frequency of the differentiator. A higher sampling frequency that is an integer multiple of the reference frequencies related to the electrical grid (60 Hz) and the switching frequency (18 kHz), represented by the parameter k in (11), ensures the proper performance of the frequency differentiator (f_{diff}) [11].

$$f_{diff} = k \cdot f_s, \quad k \in \mathbb{Z}^+ \tag{11}$$

3) By using an oscilloscope or a logic analyzer, computation times of the control routine (t_{calc}^{crt}) and the differentiator (t_{calc}^{diff}) are evaluated. Then, the available computation time of the differentiator (t_{diff}^{disp}) is determined according to (12), where T_{Diff} denotes the differentiator period, obtained as the inverse of f_{diff}.

$$t_{disp}^{diff} = T_{Diff} - t_{calc}^{diff} \tag{12}$$

4) Next, an analysis is carried out on the use of the DSC operating in dual-core or single-core mode, as follows:

   4.1 **Dual-Core Mode:** implement the control-interrupt routine on one DSC CPU operating at a rate of $1/k$ relative to the differentiator routine executed on the other CPU.

4.2 **Single-Core Mode:** determine the ratio between the computation time of the control routine (t_{calc}^{crt}) and the available time of the differentiator (t_{disp}^{diff}), given by parameter α, using a safety margin (β), which is typically adjusted within a range of 5% and 10%, depending on the project.

$$\alpha = \text{ceil}\left[(1+\beta)\cdot\frac{t_{crt}^{calc}}{t_{diff}^{disp}}\right], \quad \alpha \in \mathbb{Z}^{+} \qquad (13)$$

4.2.1 If $\alpha = 1$: add the control routine after the differentiator calculation task every k differentiator interruptions.

4.2.2 If $\alpha > k$: define a new k or reduce the order N of the differentiator.

4.2.3 If $1 < \alpha \leq k$: redistribute the control routine over α differentiator interruptions.

5) End.

IV. EXPERIMENTAL RESULTS

In order to evaluate the implementation of the proposed CVAD strategy in both single- and dual-core development scenarios, the Texas Instruments® DSC TMS320F28379D was employed for the computational cost analysis, incorporating the PEC control algorithm and its protections, which was programmed using Code Composer Studio (CCS). The analysis of single-core and dual-core architectures is therefore motivated by realistic implementation scenarios, particularly in systems that require the parallel execution of control tasks, signal processing, and communication routines. The experimental verification was conducted at different institutions using Tektronix DPO3000 and TPS2024B oscilloscopes for acquire voltage, current, and digital signals to verify algorithm processing times. The main parameters of the PEC are detailed in Table 2.

The effectiveness of the proposed control strategy was validated using a HIL platform based on the TMS320F28335 digital signal controller, a device widely recognized and used in both academia and industry. In this setup, as shown in Fig. 4, the power stage is emulated by the HIL402 system, while the control strategy is executed on the TMS320F28335. To interface the DSC with the HIL402, the HIL-DSP-100-Interface board from Typhoon was used, which provides offset and amplitude adjustments to ensure signal compatibility with the microcontroller. Regarding Fig. 4(a), it is emphasized that only the TMS320F28379D microcontroller PCB board was employed for experimental validation, whereas the main converter waveforms were obtained using the experimental HIL platform in Fig. 4(b).

The following scenarios are addressed in the next: (i) computational cost analysis, (ii) considerations regarding the strategy when implemented on a single-core DSC, and (iii) implementation of the strategy on the HIL platform, and (iv) considerations on the proposed partitioning method.

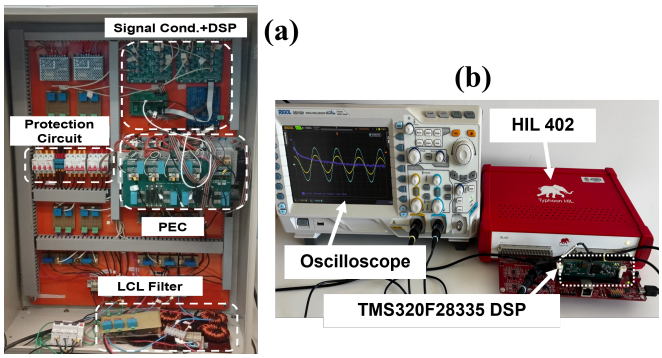

FIGURE 4. Configuration: (a) hardware setup for experimental validation, (b) experimental platform in HIL.

TABLE 2. Parameters of the single-phase converter and the system.

Parameter	Value	Parameter	Value
V_{grid}	$127V/60Hz$	L_g, R_g	0.33 mH; 0.1 Ω
P_{PEC}, V_{dc}	3 kW, 235 V	L_1, R_1	1.4 mH; 10 $m\Omega$
C_f	22 μF	L_2, R_2	23 μH; 10 $m\Omega$
ζ	0.975	B_r	1.5 Hz
ω_0	377 rad/s	f_{sw};f_{parks}	18 kHz; 90 kHz

A. SCENARIO I: COMPUTATIONAL TIME EVALUATION

Therefore, aiming to reduce its order, phase delay, and computational cost, its operating frequency was selected as a positive integer multiple of both the inverter switching frequency (18 kHz) and the grid fundamental frequency (60 Hz), resulting in a sampling frequency of 90 kHz, as discussed in [11], resulting in a ratio $k = 5$. This selection ensures that the sampling frequency remains within the maximum range allowed by the DSC register, preventing overflow issues that could lead to data loss during the differentiation process and improper algorithm operation. Therefore, the specified frequency provides an appropriate tradeoff, maintaining suitable accuracy in both amplitude and phase responses without significant degradation.

Due to the need to ensure real-time processing, precautions was taken to guarantee that the differentiator's computation time would not interfere with the control routines. In this context, the digital implementation strategy of the inverter employs two distinct sampling frequencies; one for the differentiator and another for the remaining routines, such as control, initialization, and protections, which is set to 18 kHz. This separation is managed with the aid of parallel processing, as shown in Fig. 5. To this end, both cores of the DSC TMS320F28379D are utilized, with the control/synchronization/protection routines implemented on CPU1, operating with a period of $T_{PEC} = 1/f_{PEC}$, where f_{PEC} is set to 18 kHz, while CPU2 executes the differentiator routine at 90 kHz.

Based on these considerations, an analysis is carried out to estimate the computational performance and number of clock cycles (n_{clk}) of the differentiators designed using the

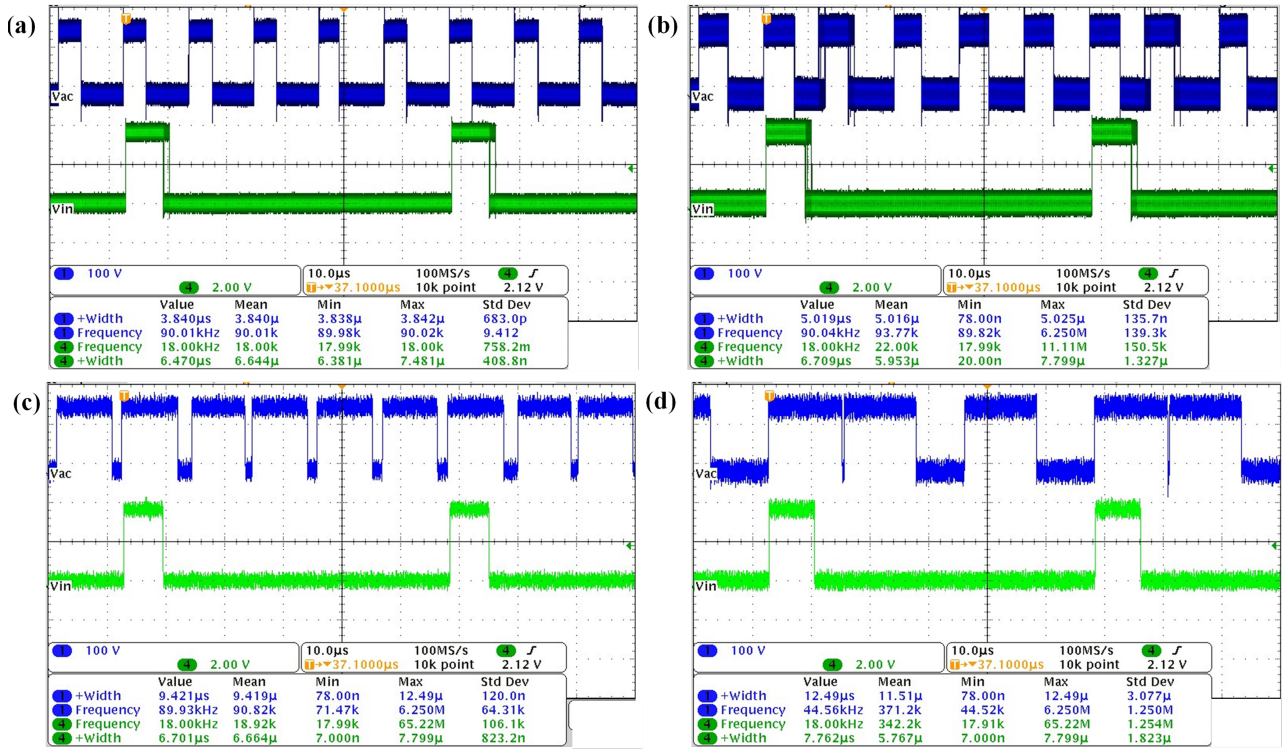

FIGURE 5. Comparative analysis among PM differentiators: (a) PM6, (b) PM10, (c) PM10, and (d) PM30.

PM algorithm. For this purpose, the computational time of PM-based differentiators of orders N equivalent to 6, 10, 20, and 30 is compared, as shown in Fig. 5 and detailed in Table 3. Considering a 200-MHz clock frequency for the TMS320F28379D microcontroller, the number of clock cycles was estimated as the product of the execution time and the clock frequency.

Fig. 5 shows that the execution time of the PEC tasks remains constant, i.e., the computational time of the control system is unchanged at each sampling step of 1/18 kHz. However, increasing the order of the PM differentiator raises the computational cost and number of clock cycles, as evidenced in Table 3. Considering the execution time constraints and parallel operation, the maximum viable order achieved was $N = 20$, whose computational time still does not exceed the sampling period of the differentiator (1/90 kHz).

Among these differentiators, the one with order $N = 6$ has the lowest computational cost, since its execution requires fewer mathematical operations, as shown in Fig. 5(a). The differentiator of order 10 has a longer computational time compared to the one of order 6, yet shorter than that of order 20, as depicted in Fig. 5(b). According to 'step (3)', the available time for each differentiator implementation is defined as the difference between the sampling period of differentiator, 1/90 kHz, and the computation time of each differentiator order, as reported in Table 3.

Based on this time interval, it can be stated that, in order to enable the application in a single-core system, the PEC routines could be to be partitioned into up to five segments ($T_{PEC}/5$), $k = 5$, such that each segment (1/5) remains shorter than the available time for each differentiator. Thus, it can be observed that only the differentiators of order 6 and 10 are capable of operating on a single-core DSC, since the control system code, when segmented and executed on CPU1, fits within the available time along with the execution of the differentiator on CPU2.

This is not feasible with the differentiator of order $N = 20$, since the computational time resulting from the integration of the partitioned control algorithm into the CPU, aiming for joint execution of the control routine and the differentiation, exceeds the allowed timing, as shown in Fig. 5(c). Finally, high-order differentiators, such as the one of order 30, do not meet the proposed requirement in the flowchart shown in Fig. 3, since the computational time overflows and data loss occurs, making them unsuitable for this application even in a dual-core system, as illustrated in Fig. 5(d). Continuing the analysis, it becomes essential to assess the feasibility of implementation under the constraint of a single processing core. In this context, the following investigation delves into the implications of this limitation, highlighting the technical challenges involved and the strategies employed to ensure the efficient and synchronized execution of the inverter and differentiator routines, while meeting the system's timing requirements.

For comparison with the state of the art, the computational cost of the widely used nGI differentiator was included. Its execution time was measured at approximately 295 ns, however, this method is sensitive to grid frequency variations,

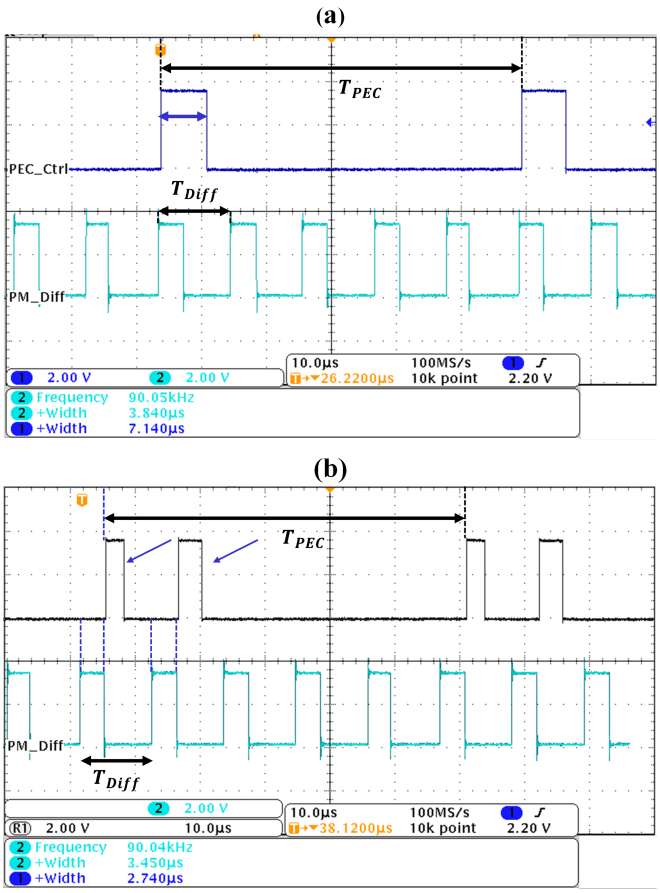

FIGURE 6. Analysis of the inverter firmware and differentiator implementation: (a) execution using dual-core, (b) execution consolidated on a single core.

TABLE 3. Computational Time Comparison.

Order PM	Available time (t_{disp}^{diff})	Computing Time (t_{calc}^{diff})	n_{clk}
$N = 6$	7.271 μs	3.840 μs	768
$N = 10$	6.092 μs	5.019 μs	≈1004
$N = 20$	1.690 μs	9.421 μs	≈1884

which may cause harmonic frequency drift and, in the worst case, excite the filter resonance [26].

B. SCENARIO II: CONSIDERATIONS WITH SINGLE-CORE MODE ON TMS320F28379D

In this scenario, the inverter firmware (PLL algorithm, control routines, data acquisition, protection, etc.) and the differentiator were implemented on a single CPU of the DSC TMS320F28379D. The primary objective of the PEC is active current injection into the electrical grid; therefore, load elements were not considered in the analyzed scenarios. Although the inclusion of a resistive load at the PCC could improve control-loop performance by providing additional damping. Aspects related to harmonic rejection and power quality enhancement, typically addressed through feedforward schemes or high-gain controllers such as repetitive control, is discussed in more detail in [27].

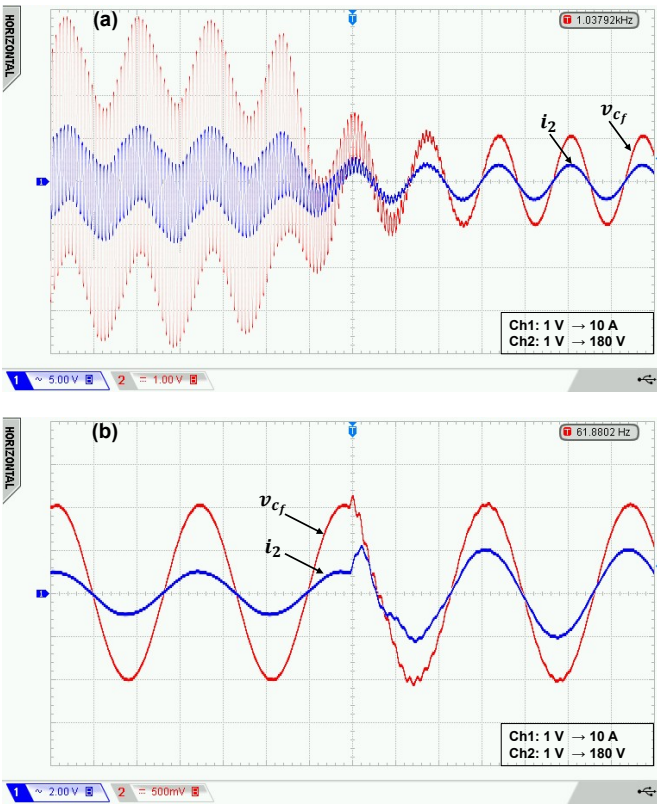

FIGURE 7. HIL setup analysis highlighting the effect on the injected current: (a) system without and with CVAD-PM6; (b) system with AD using a step in reference current of the CVAD-PM6.

Considering the previous implementation of the proposed strategy on two CPUs, and the constraints associated with the order of each differentiator, Fig. 6(a) illustrates how the inverter control and management routines implemented on CPU1 with a period of interruption T_{PEC} operate in parallel with the differentiator computation routine, which is sampled at 90 kHz on CPU2, with a period of T_{Diff}. In this case, the ceil function is determined based on the relationship between the computation times of the control routine and the differentiator, with a safety factor of 5%.

As previously described, this clearly demonstrates that the differentiator runs five times faster than the inverter firmware. In this context, it is evident that the maximum computation time associated with the inverter firmware on CPU1 is 7.885 μs. When combined with the differentiator execution time (3.84 μs), the total interval exceeds the differentiator period of 11.11 μs, resulting in 11.725 μs (3.84 μs + 7.885 μs > 11.11 μs). Therefore, to implement the proposed strategy on CPU1, the inverter firmware tasks were redistributed over two consecutive differentiator cycles. This reorganization was performed through a scheduling approach that ensured the sampling and processing of all inverter and differentiator tasks, as illustrated in Fig. 6(b). Thus, when considering the sixth-order differentiator, the parameter α obtained from the ceil function yields a value of two ($\alpha = 2$),

as shown in (13). In this case, the resulting value is lower than five, i.e., the parameter $k = 5$ defined in (11), thereby ensuring compatibility within a single processing core. It is emphasized that an analogous procedure is applied to the other differentiators.

After verifying the feasibility of implementing the differentiators on a single core, focuses on validating the CVAD strategy through the HIL platform. Fig. 7(a) presents the analysis of the experimental system with and without active damping, focusing on the CVAD. The differentiator is designed using the PM algorithm to operate as a sixth-order differentiator (PM6), resulting in the CVAD-PM6. Initially, the injected current exhibits significant oscillations due to the intentional deactivation of the active damping. However, when the CVAD is activated, the current injected into the grid, i_2, becomes smoother, eliminating oscillations and taking on a sinusoidal waveform in phase with the capacitor voltage, v_{C_f}, indicating correct current injection.

Fig. 7(b) illustrates the active current injection into the electrical grid, followed by a step change in the reference amplitude. The results show that the CVAD strategy continues to operate effectively even with the increased current, which causes a brief transient period in the capacitor voltage. It is observed that, in both situations, the control system performs efficiently. Therefore, this scenario is considered to satisfactorily meet the proposed requirement, thereby ensuring a unity power factor and a current THD of around 3%, below 5%, in accordance with the criteria established in IEEE 1547-2018 Stds [7].

C. SCENARIO III: CVAD - PM6 UNDER NOISE INJECTION

This scenario analyzes the insertion of noise measurement in the LCL filter capacitor voltage in order to evaluate the performance of the proposed technique, since such a condition is highly feasible in industrial environments. It is worth noting that the noise considered in the experiments corresponds to a random source generated by the native Typhoon HIL block, with an amplitude of approximately 2% of the fundamental voltage component, which is compatible with practical operating conditions. It is observed that, even in the presence of noise, it is not amplified by the control structure, the GCI injects active current into the power distribution network exhibits predominantly sinusoidal behavior, indicating stable converter operation, and with a power factor close to unity, as shown Fig. 8.

D. SCENARIO IV: CONSIDERATIONS ON THE PROPOSED PARTITIONING METHOD

The proposed partitioning method was designed to ensure predictable temporal behavior through the use of a dedicated hardware timer, implemented via an independent PWM peripheral that is separated from the PWMs driving the power switches. This peripheral generates the 90-kHz interrupt of the differentiator, thereby ensuring an accurate and isolated time base. The 18-kHz control routine is always triggered after a fixed number of differentiator cycles ($k = 5$), as

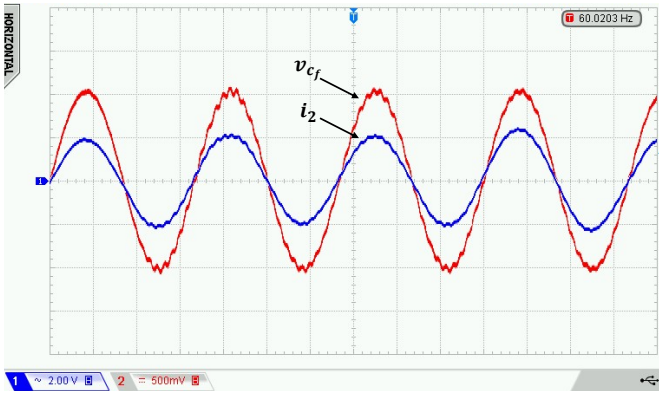

FIGURE 8. HIL setup analysis under noise injection with CVAD-PM6.

evidenced in Figs. 5 and 6, which keeps the execution of the control tasks within a deterministic time window.

Regarding jitter, its influence is mitigated by the high sampling frequency (90 kHz), which is well above the resonance frequency of the LCL filter, and by the no recursive nature of the FIR differentiator, which is less sensitive to timing variations than IIR-based approaches. Protection interrupts are given the highest priority and are executed within the *main* () routine, and task isolation between cores (in dual-core operation) is employed to ensure that critical events are not compromised.

Moreover, in the single-core case, the parameter α (computed using the ceil function) defines over how many differentiator cycles the control tasks are distributed, while β (between 5% and 10%) provides a safety margin to absorb execution-time fluctuations. This ensures that, even under high CPU load conditions, critical routines do not exceed the available time window. In this context, α should be interpreted as a sufficient (and conservative) condition to ensure the feasibility of implementation in single-core architectures. By enforcing $\alpha < 1$, the methodology guarantees that the computational burden of the control routine fits within the available execution time, even when accounting for uncertainties such as task scheduling jitter, interrupt handling, and additional background processes.

Although extreme CPU load scenarios may increase jitter, the measured timing margins and the adopted scheduling strategy ensure that the system operates in a stable and deterministic manner within the specifications of the CVAD control. Future FPGA-based implementations could offer even greater temporal robustness; however, the current solution already satisfies the real-time requirements of the application.

It is noted that, in the proposed methodology, there is a potential risk of numerical saturation or overflow in the differentiator computations, particularly when high filter orders or very high sampling frequencies are employed. The multiplication and accumulation operations inherent to FIR filters may exceed the dynamic range of the variables, especially in fixed-point implementations. To ensure numerical robustness and validation, three main strategies were

adopted: the use of 32-bit floating-point arithmetic, which provides a wide dynamic range in accordance with the IEEE 754 standard; normalization of the filter coefficients designed using the Parks–McClellan algorithm; and limitation of the input signal amplitude prior to processing. In this sense, it was verified that no saturation or significant loss of precision was observed in the obtained results when compared with the simulated scenarios used as initial references in the implementation process, ensuring that the proposed solution is numerically stable and suitable for CVAD operation under the specified conditions.

In this context, the main conclusions related to computational cost, memory requirements, and real-time feasibility are of a general nature for FIR differentiators. The aspects that are specific to the Parks–McClellan method are limited to the offline filter design stage, which does not impact the real-time implementation discussed in this manuscript.

V. CONCLUSION

This paper presented a critical analysis of the computational cost and the feasibility of implementing the active damping technique for grid-connected inverters on conventional microcontrollers, using CVAD and the Parks-McClellan algorithm. The proposed method successfully achieved active damping by estimating the capacitor current through the derivative of the capacitor voltage, employing the PM algorithm for orders 6, 10, and 20 (PM6, PM10, and PM20) in a dual-core digital signal controllers, thus eliminating the need for an additional current sensor. However, it was demonstrated that only PM6 and PM10 differentiators were feasible for implementation on single-core DSCs. It is important to highlight that the proposed methodology is valid for single-core DSCs. In this context, the authors conducted a Hardware-In-the-Loop test using the TMS320F28335 DSC, which is widely recognized and used in both academia and industry. The proposed control strategy was shown to be fully compatible with both dual-core and single-core microcontrollers. The proposed methodology stands out due to its capability to provide active damping without the need for additional sensors, as the capacitor voltage is used for both active damping and synchronization algorithm. The main limitations of the proposed technique are associated with increased computational cost and implementation complexity, particularly in the case of high-order differentiators or when using high sampling frequencies. Finally, future work will focus on comparing the proposed differentiator with others reported in the literature, evaluating the inverter's external stability, performing comparative analyses with current-based active damping strategies, and integrating additional functionalities into the control structure, such as active filtering. Moreover, the proposed partitioning strategy can be extended to other differentiation methods, including Kalman filters and Wavelet-based approaches, as well as to the assessment of code partitioning in applications involving state-of-charge estimation in batteries, smart meters, and power exchange management in microgrids. In addition, the integration of communication protocols in grid-tied inverters employing CVAD constitutes a relevant research direction, since, in commercial and industrial applications, communication is a critical aspect that must coexist with real-time control tasks.

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AUTHOR'S CONTRIBUTIONS

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PLAGIARISM POLICY

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DATA AVAILABILITY

The data used in this research is available in the body of the document.

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