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Design, FEA-Based Physical Insights, and Experimental Verification of a Planar Transformer for Two-Switch Flyback Converters

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ABSTRACT Parasitic parameters in high-frequency transformers directly impact losses, electromagnetic interference (EMI), and voltage/current stresses in power converters. This paper presents a comparative analysis and optimization of planar transformers (PT) applied to a two-switch Flyback (TSF) converter. The investigation focuses on balancing leakage inductance, AC resistance, and parasitic capacitances through different PCB winding arrangements using multiphysics Finite Element Analysis (FEA). By employing a structured analysis that correlates electromagnetic and thermal modeling with experimental validation, this work demonstrates how layer alignment and interleaving mitigate proximity effects and drastically reduce ringing in semiconductor switches. The results show that the optimized configuration achieved an 80% reduction in leakage inductance and a 57% reduction in AC resistance compared to conventional designs, resulting in an efficiency of 89.2% and a significant decrease in thermal stress. The study provides evidence-based design guidelines for mitigating parasitic effects in high-power-density converters.

KEYWORDS Finite element analysis, Double-switch flyback, Planar transformer, AC resistance, Leakage inductance, Stray capacitance.

I. INTRODUCTION

Magnetic components based on planar technology have been studied since the 1980s due to their advantages, such as low profile, high energy density, improved thermal dissipation, and ease of manufacturing [1],[2]. The adoption of wide-bandgap semiconductors like GaN and SiC has increased switching frequencies, amplifying the impact of transformer parasitic elements [3].

In planar transformers (PTs), key parasitic components — including AC resistance (R_{ac}), leakage inductance (L_{lk}), and inter-winding capacitance (C_{str}) — can be minimized during the design stage, ensuring predictable electrical characteristics and manufacturing consistency [4]. However, these parasitic effects directly impact power losses, voltage stresses, and Electromagnetic Interference (EMI) [5],[6].

While the use of Finite Element Analysis (FEA) simulation tools is well-established, the precise correlation between the physical arrangement of planar windings and the dynamic response in two-switch Flyback converters still presents practical design challenges. This work contributes to the field by conducting an in-depth investigation into how different winding topologies (aligned vs. misaligned) and interleaving strategies affect flux distribution and parasitic elements. Moving beyond purely analytical approaches, this research utilizes 3D electromagnetic analysis to isolate high-frequency phenomena that influence losses and transient converter behavior. The primary contribution lies in the experimental demonstration that geometric optimization of PCB tracks, validated through distinct prototypes, is key to minimizing voltage overshoot and enhancing thermal performance, offering a set of practical guidelines for the design of high-performance planar magnetic components.

The remainder of this paper is structured as follows: Section 2 describes the proposed topology and its application characteristics. Section 3 outlines the fundamental aspects of planar transformer design and key physical design concepts. Section 4 details the implementation and simulation process using Finite Element Analysis (FEA). Section 5 presents the experimental results, including a comparison with a conventional transformer. Finally, Section 6 provides conclusions and recommendations based on the findings.

II. AUXILIARY POWER SUPPLY DOUBLE-SWITCH FLYBACK

The Flyback converter, derived from the buck-boost topology, utilizes a coupled inductor as its magnetic component. It is widely employed as an auxiliary power

supply in applications requiring galvanic isolation and design simplicity.

In industrial equipment powered by a three-phase network, the input voltage typically ranges from 220 V to 480 V, leading to a DC bus voltage between 265 V and 750 V. A 48 V output is considered a safe voltage level, minimizing the risk of electrical shock while allowing easy access for connecting auxiliary devices, such as sensors and actuators, without shutting down the primary converter. Fig. 1 illustrates the two-switch Flyback (TSF) converter topology, which is advantageous for applications with power levels below 100 W and high input voltage requirements.

In the TSF topology, switching losses are relatively low, and the voltage stress is shared between the two switches. Fig. 2 presents simulated waveforms for a TSF converter operating in discontinuous conduction mode (DCM) with a high leakage inductance transformer.

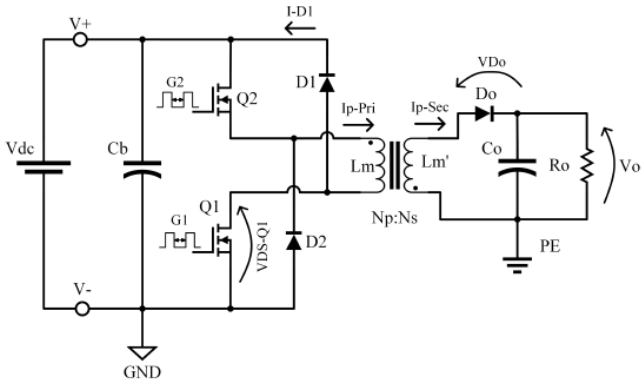


FIGURE 1. Two-switch flyback converter.

As shown in Fig. 2, the drain-source voltage (V_DS-Q1) is ideally clamped at 265 V (the DC bus voltage) due to the action of diodes D1 and D2. This mechanism helps limit voltage spikes caused by L_{lk} and enhances the TSF converter's efficiency by returning some of the leakage energy to the source. A notable disadvantage, compared to conventional Flyback topologies, is the need for a second power switch and an isolated gate driver.

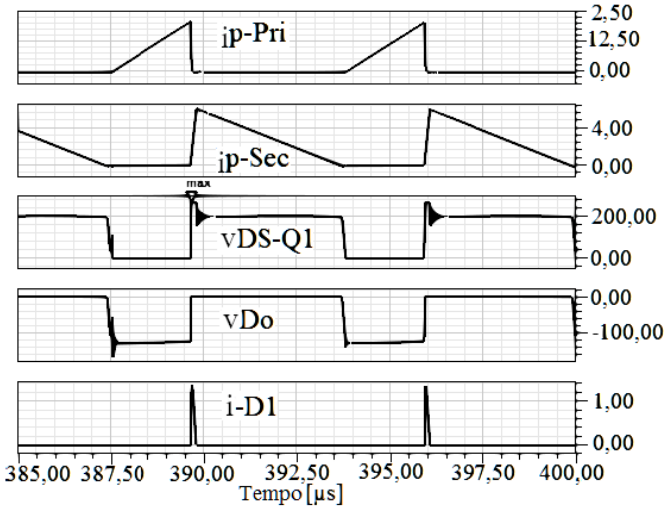


FIGURE 2. TSF waveforms: ip−Pri primary's current, ip−Sec secondary's current, VDS−Q1 switch voltage Q1, VDo diode voltage Do, i-D1 current's diode D1.

The converter's design specifications are listed in Table 1, including its input and output parameters, operating frequency, and estimated efficiency.

To further analyze the TSF converter, Fig. 3 depicts the power loss characteristics of the semiconductors and the transformer as a function of frequency, considering both minimum and maximum input voltage conditions. It can be observed that semiconductor losses increase significantly with input voltage and frequency, whereas transformer losses tend to decrease as frequency increases, even without accounting for the AC resistance effects of the conductors, which are later analyzed using FEA simulations.

Although semiconductor losses have a significant impact on overall converter efficiency, the coupled inductor remains the most expensive component. Given these trade-offs, a switching frequency of 160 kHz was chosen, as it ensures that transformer losses are reduced to 1/e of their peak value while maintaining an estimated efficiency of approximately 85% under worst-case operating conditions.

TABLE 1. TSF converter technical specification.

Parameter	Value
Input Voltage (AC)	220V/480V +10% -5%
Output Voltage	48V
Ouput Voltage Ripple	< 4%
Ouput Current	1.8A
Output Power	85W
Frequency	160kHz
Maximum Duty Cycle	35%
Estimated Efficiency	85%

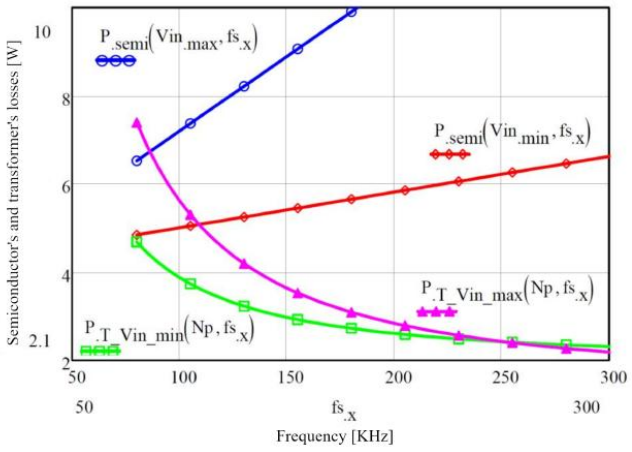


FIGURE 3. Semiconductor and transformer losses.

III. MAGNETIC ELEMENTS USING PLANAR CORES

A. *GENERAL ASPECTS*

The windings of a planar transformer can be implemented using a multilayer printed circuit board (PCB), as illustrated in Fig. 4. This approach ensures reproducible electrical characteristics in large-scale production while enabling flexible winding arrangements. Additionally, different layers can be connected in series or parallel, enabling further optimization of AC resistance, leakage inductance, and self-capacitance.

As highlighted in previous studies [7],[8], planar transformers excel in high-frequency applications due to their compact size and improved efficiency:
• Reduced height and low profile, making them ideal for applications with space constraints;
• Improved thermal dissipation, due to a high surface-to-volume ratio;
• Enhanced reproducibility, as PCB-based winding layouts provide consistent electrical characteristics in large-scale production;
• Simplified interleaving, which reduces leakage inductance (L_{lk}) and AC resistance (R_{ac}).

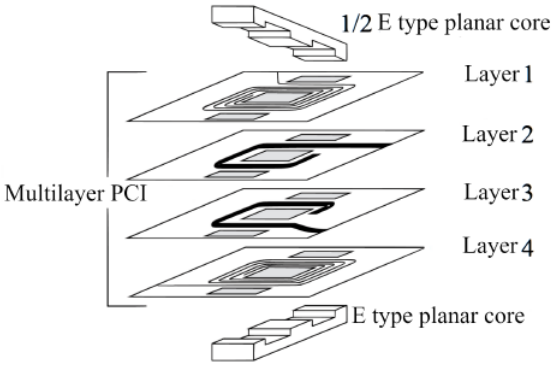


FIGURE 4. Planar transformer architecture using a multilayer PCB.

Despite these advantages, planar transformers also present some challenges [9]:
• Larger footprint, requiring more PCB area compared to conventional wire-wound transformers;
• Lower window utilization factor, meaning that a smaller percentage of the available core window is occupied by conductive material;
• Limited number of turns, as PCB traces cannot be stacked as easily as wire-wound windings;
• Higher self-capacitance, due to the close proximity of overlapping PCB layers, which can impact high-frequency performance.

To effectively balance these trade-offs, careful design considerations are required when selecting the winding arrangement, layer configuration, and insulation spacing. These factors directly influence the transformer's electrical parameters and overall performance in the power converter.

B. *DC AND AC WINDING RESISTANCE*

In addition to DC resistance (R_{dc}), which depends on the conductor's material, cross-sectional area, and length, high-frequency operation introduces AC resistance (R_{ac}) due to skin and proximity effects. At elevated frequencies, current tends to concentrate in specific regions of the conductor, forming paths that minimize inductive energy storage—even at the cost of increased ohmic losses.

The relationship between Rac and Rdc is described by (1), as proposed by Ouyang & Andersen [2]. This equation accounts for both the skin effect and the influence of multiple conductor layers:

$$\frac{R_{AC}}{R_{DC}}=\frac{\xi}{2}\left[\frac{sinh\xi+sin\xi}{cosh\xi-cos\xi}+(2m-1)^2\cdot\frac{sinh\xi-sin\xi}{cosh\xi+cos\xi}\right] \quad (1)$$

where $\xi = h/\delta$ represents the ratio of conductor thickness (h) to skin depth (δ), and m denotes the number of layers, determined by the magnetomotive force (MMF) distribution according to (2):

$$m=\frac{F(h)}{F(h)-F(0)} \quad (2)$$

For large values of h, reducing R_{dc} can lead to a significant increase in R_{ac}, particularly when the number of conductor layers is high. A key strategy for minimizing R_{ac} in planar transformers (PTs) is to interleave the primary and secondary windings. This helps to balance the MMF distribution, improving current uniformity and reducing proximity losses.

However, in Flyback transformers, where energy transfer is indirect (i.e., primary and secondary currents do not flow simultaneously), proximity losses cannot be effectively reduced through interleaving alone. Instead, conductor thickness must be carefully designed to satisfy $\xi = h/\delta < 1$, ensuring that skin effect losses remain controlled.

Although (1) provides an initial estimation, it is limited to a 1D analytical model that neglects complex current distributions in real-world applications. To obtain a more accurate estimate of R_{ac}, a 2D FEA was performed using Maxwell®, simulating an interleaved four-layer planar transformer. Fig. 5 presents the results of this simulation, showing the ratio R_{ac}/R_{dc} for different conductor thicknesses over a range of frequencies.

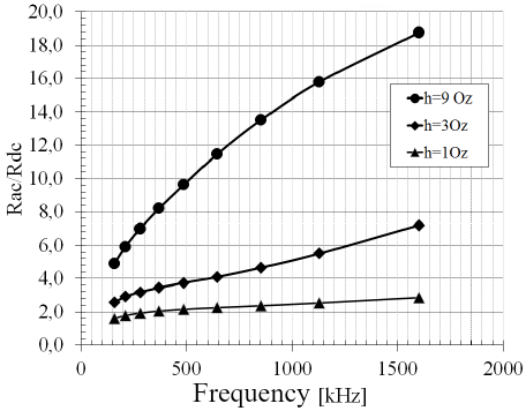


FIGURE 5. Graph of R_{ac}/R_{dc} ratio for different conductor thicknesses.

At 150 kHz, a 9 Oz (315 µm) thick conductor exhibits an R_{ac}/R_{dc} ratio of approximately 5, which increases to 18 at 1.5 MHz, confirming the strong frequency dependence of AC resistance. These results align with previous findings in [1],[2], emphasizing the need for optimized conductor sizing in planar transformer design.

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C. *LEAKAGE INDUCTANCE*

In an ideal transformer with infinite core permeability, all magnetic flux would be confined within the core. However, in real designs, leakage inductance (L_{lk}) arises from the portion of magnetic flux that does not couple between the primary and secondary windings. This energy is primarily stored in the insulation region between the windings, where the permeability is approximately μ_0 (air or dielectric material). The energy stored E in L_{lk} can be expressed as:

$$E=\frac{\mu_0}{2}\sum\int H^2(I_w b_w d_x) \tag{3}$$

where μ_0 is the vacuum permeability, b_w is the winding width, I_w is the peak current flowing through the winding, which corresponds to the primary current I_p in this analysis, H is the magnetic field intensity in the region between the windings and d_x is the insulation thickness between the windings.

For a uniform winding distribution and a constant magnetic field between turns, the energy per unit volume can be approximated by:

$$\frac{E}{V}=\frac{\mu_0}{2}\sum\left(\frac{NI}{b_w}\right)^2 \tag{4}$$

Since L_{lk} depends on the magnetomotive force (MMF), optimizing its distribution through interleaved winding configurations can significantly reduce leakage inductance (L_{lk}). By alternating primary and secondary layers, MMF variation is minimized, resulting in improved coupling and lower L_{lk} values.

D. *PARASITIC CAPACITANCE*

The overlapping of windings with different voltage levels creates intrinsic capacitances within the transformer. The self-capacitance (C_{po}) between adjacent layers and the interwinding capacitance (C_{pso}) between primary and secondary windings are particularly relevant at high frequencies. The capacitance C_o between two conductive layers separated by an insulating material follows the relation:

$$C_0=\varepsilon_r\varepsilon_0\frac{A_S}{h_\Delta} \tag{5}$$

where A_s is the overlapping surface area, h_Δ is the dielectric thickness, and ε_r is the relative permittivity of the insulation material.

Although interleaving reduces L_{lk} and R_{ac}, it also increases C_{pso}, which can lead to common-mode noise issues in high-frequency applications. As a trade-off, techniques such as layer pairing and optimized insulation spacing can be used to mitigate these effects while maintaining low L_{lk}.

In planar transformers, capacitances are inherently higher due to the small insulation thickness of PCB traces and foil windings. Therefore, careful design considerations must be made to balance L_{lk}, R_{ac}, and C_{str}, ensuring optimal high-frequency performance and minimizing unwanted EMI effects [2],[10].

IV. PLANAR TRANSFORMER DESIGN

The proposed planar transformer (PT) design methodology follows a structured approach to optimize the trade-off between leakage inductance (L_{lk}), AC resistance (R_{ac}), and parasitic capacitance (C_{str}) while ensuring manufacturability. The design process consists of three key steps:

1. Preliminary design using Ansys PExprt®, selecting the core material, geometry, and number of turns based on analytical models.
2. 2D FEA in Ansys Maxwell®, refining winding arrangements and evaluating high-frequency effects.
3. 3D FEA in Ansys Maxwell®, providing a detailed assessment of R_{ac}, L_{lk}, and C_{str} for validation against experimental data.

By integrating analytical modeling with FEA simulations, the methodology enables a more precise estimation of parasitic elements, leading to improved transformer performance in high-frequency applications.

A. *PRELIMINARY DESIGN*

The first step involves defining the electrical and mechanical parameters based on the converter specifications provided in Section 2. The key transformer parameters, including turn ratio, inductance, and current stresses, are listed in Table 2.

TABLE 2. Converter and transformer electrical parameters.

Parameter	Value	Transformer Current Stresses	Value
Turns ratio (N_p/N_s)	220V/480V +10% -5%	Ip_{pk}	2.2A
Inductance	260µH	Ip_{ef}min)	0.44A
Minimum Duty Cycle	12.26%	Ip_{ef}max)	0.77A
Maximum Duty Cycle	34.63%	Is_{pk}	6.6A
Output Capacitor (C_o)	2.4µF	Is_{ef}	3.04A

These parameters are input into Ansys PExprt®, along with manufacturing constraints such as PCB layer limitations, core material, and ambient temperature. Ansys PExprt® facilitates the selection of an appropriate core while ensuring that saturation limits are not exceeded. The core selection is based on (6), which defines the flux density variation:

$$\Delta B=\frac{V\Delta t}{NA_e} \tag{6}$$

To estimate core losses, the Modified Steinmetz Equation (MSE) is used, as shown in (7):

$$P=k{f_{eq}}^{(\alpha-1)}\left(\frac{\Delta B}{2}\right)^\beta f \tag{7}$$

where core loss coefficients (k, α, and β) are determined based on material properties and operating conditions. The equivalent sinusoidal excitation frequency is calculated using (8):

$$f_{eq}=\frac{2}{(\pi\Delta B)^2}\int_0^t\left(\frac{dB}{dt}\right)^2 dt \tag{8}$$

The track width (W_n) for the PCB windings is determined using (9), considering the available core window and insulation spacing:

$$W_n = \frac{B_w - s_p - (N_p - 1)s}{N_p} \quad (9)$$

A cross-sectional view of the planar transformer design with an EI38 core and a 4-layer PCB is illustrated in Fig. 6. To mitigate fringing flux losses, windings are positioned 2.2 mm away from the air gap, reducing proximity effect heating [11].

At this stage, copper losses are estimated based on DC resistance and skin effect considerations, while magnetic losses are calculated at the maximum input voltage (750 V) to account for worst-case conditions. The key transformer dimensions and characteristics derived from the analytical design are summarized in Table 3.

B. *CONCEPTUAL DESIGN AND 2D FEA*

Following the preliminary design, the 2D model is generated in Ansys PExprt® and exported to Ansys Maxwell® for FEA. The primary focus of this step is to refine the winding arrangement, optimizing L_{lk}, R_{ac}, and C_{str}. Two winding configurations were evaluated:

1. PPSS (Primary-Primary-Secondary-Secondary): Optimized for lower parasitic capacitance, reducing oscillations and EMI.
2. PSSP (Primary-Secondary-Secondary-Primary): Designed to minimize L_{lk} and R_{ac}, improving efficiency and reducing thermal stress.

The results from the 2D FEA simulations are presented in Table 4, comparing the key electrical parameters for the different winding configurations investigated. These results provide a preliminary assessment of the impact of track alignment and layer arrangement on the transformer's parasitic elements before the final 3D refinement.

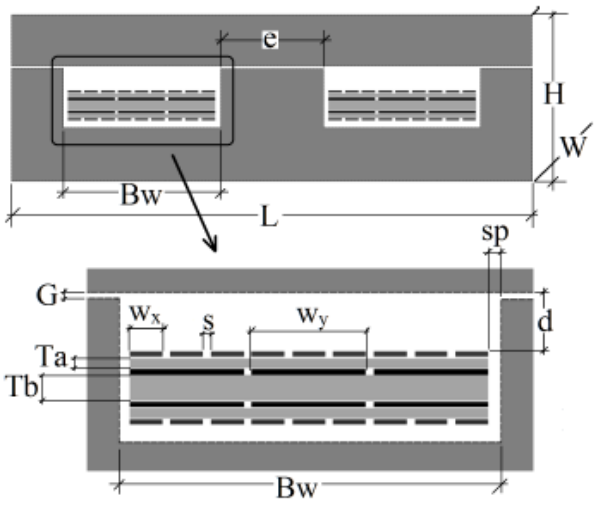


FIGURE 6. Cross-sectional view of PT with EI38 core and 4-layer PCB.

TABLE 3. Analytical design parameters from Ansys PExprt®.

Parameter	Value
Core material (Magnetics)	Ferrite R type
A_c - Central lag Area	192mm^2
V_c - Core Volume	8520mm^3
e - Central lag window	7.62mm
B_w - Window Length	11.4mm
L – Core Length	38.1mm
H - Core Height	12.0mm
W - Core Width	25.4mm
N_p - Primary turns	18
N_s - Secondary turns	6
W_x - primary's track width	0.92mm
W_y - secondary's track width	3.0mm
T_a - outer layer insulation thickness	0.32mm
T_b - inner layer insulation thickness	0.80mm
J_p - Primary current density	1356A/cm^2
J_s - Secondary current density	2708A/cm^2
G - Length gap	0.178mm
ΔB - magnetic flux density	162.9mT
P_{mag} - core losses at V_{in}=750V	1.91W
P_c- copper losses	1.47W

The equivalent circuit model of the transformer, incorporating these parameters, is illustrated in Fig. 7.

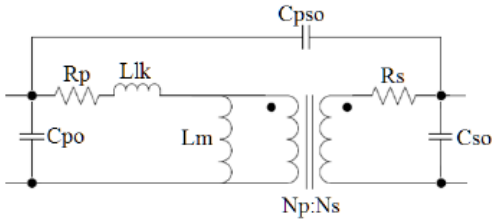


FIGURE 7. Transformer's equivalent circuit model.

The 2D FEA results confirm that interleaving the secondary winding between primary layers (PSSP) significantly improves magnetic coupling, reducing L_{lk} by approximately 80% compared to the PPSS configuration. However, C_{pso} (interwinding capacitance) is higher in the PSSP arrangement, requiring further analysis in the 3D FEA simulations discussed in the next section.

TABLE 4. Maxwell 2D analysis results.

Parameter	PPSS	PSSP
L_m[μH]	245.6	245.7
C_{po}[pF]	33.18	12.14
C_{pso}[pF]	47.3	249.21
L_{lk}[μH] @ 160 kHz	2.8	0.534
R_{pdc} - at DC [Ohm]	1.099	1.099
R_{sdc} - at DC [Ohm]	113	113
R_{pca} - at 160 kHz [Ohm]	1.53	1.68
R_{sca} - at 160 kHz [Ohm]	164	181
Pc - copper losses [W]	1.55	1.62
ΔT at 40 °C environment temperature [°C]	35.5	36.2

C. *PROTOTYPE DEVELOPMENT AND 3D FEA*

To validate the design methodology, three transformer prototypes were manufactured and tested. The prototypes, designated as PT-A, PT-B, and PT-B*, were fabricated by two different manufacturers. The primary difference between

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PT-A and PT-B lies in the PCB layout design, as shown in Fig. 8.

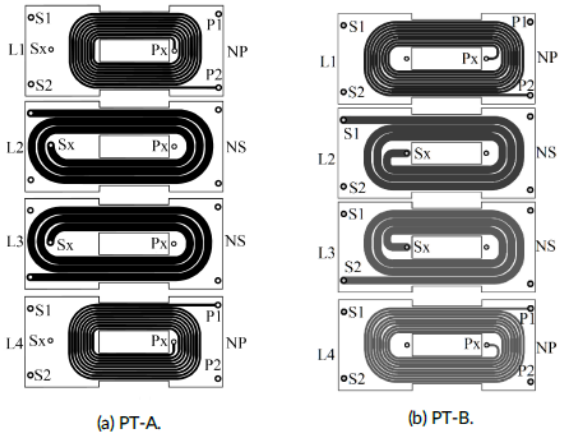


FIGURE 8. Layout comparison between PT-A (misaligned) and PT-B (aligned).

The PT-A prototype features misaligned windings, which can negatively impact leakage inductance (L_{lk}) and AC resistance (R_{ac}), whereas PT-B utilizes aligned windings, enhancing magnetic coupling and significantly reducing L_{lk}.

To further analyze these configurations, 3D FEA was performed in Ansys Maxwell®. The 3D models of both prototypes are depicted in Fig. 9.

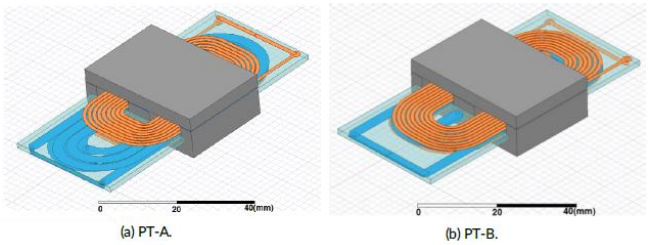


FIGURE 9. Ansys Maxwell 3D model of PT-A and PT-B.

The insulation distances were set at 5.5mm on the surface and 3.0 mm for internal layers. Interconnections between PCB layers were achieved using plated through-hole (PTH) vias, positioned at P_x and S_x (where P_1/P_2 are primary terminals and S_1/S_2 are secondary terminals).

During manufacturing, PT-B was produced with an external copper thickness of approximately 90µm, deviating from the initially specified 35 µm. This variation was incorporated into the Ansys Maxwell 3D simulations for accurate comparison.

D. *3D FEA RESULTS: LEAKAGE INDUCTANCE AND AC RESISTANCE*

The primary leakage inductance (L_{lk}) values for each transformer configuration were analyzed across different frequencies. The simulation results are presented in Fig. 10.

As frequency increases, L_{lk} decreases in all configurations. This effect occurs because, at higher frequencies, current concentrates near the inner turns, improving coupling and reducing fringing flux. However, this also increases AC resistance (R_{ac}), as shown in Fig. 11.

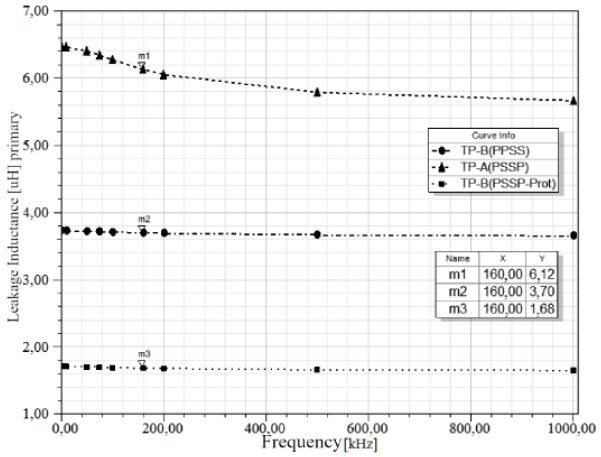


FIGURE 10. Leakage inductance variation with frequency (obtained by simulation).

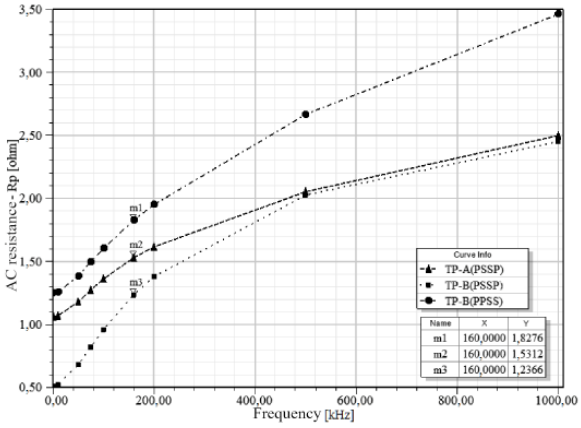


FIGURE 11. AC resistance variation with frequency (obtained by simulation).

PT-A, with misaligned windings, exhibited the highest leakage inductance (L_{lk}), more than three times greater than that of PT-B. In contrast, PT-B with a PSSP-aligned configuration demonstrated the lowest L_{lk}, confirming the benefits of interleaving and alignment in improving magnetic coupling. However, the PPSS-aligned configuration of PT-B resulted in higher AC resistance (R_{ac}) due to the absence of interleaving, which intensified proximity effect losses.

Although R_{ac} values remain similar across all configurations up to 200 kHz, they diverge as frequency increases. Among the prototypes, PT-B (PPSS) exhibits the highest R_{ac}, as its lack of interleaving increases proximity effect losses. In contrast, PT-A, despite its misaligned winding, achieved approximately 16% lower Rac compared to PT-B (PPSS) at 160kHz, while maintaining the same number of layers.

PT-B (PSSP) demonstrated the lowest R_{ac}, even though it had a longer mean length of turn (MLT) and part of its winding positioned further from the core cross-section compared to PT-A. This can be attributed to PT-A's primary winding being closer to the air gap, where the improved coupling from shorter turns was insufficient to offset the increased Rac caused by fringing flux. Above 200 kHz, R_{ac} values for PT-A and PT-B (PSSP) begin to converge, indicating that misaligned windings have a more pronounced effect at lower frequencies.

These findings highlight the critical role of winding alignment in planar transformer designs, an aspect that 2D FEA alone cannot fully capture.

V. EXPERIMENTAL RESULTS

To validate the proposed planar transformer (PT) design methodology, a two-switch Flyback (TSF) converter prototype was built and tested. The converter was assembled using STW10N95K5 MOSFETs, a STPSC10H065D SiC output diode (both from STMicroelectronics), and the UC2844 current-mode controller. Fig. 12 shows the assembled TSF prototype.

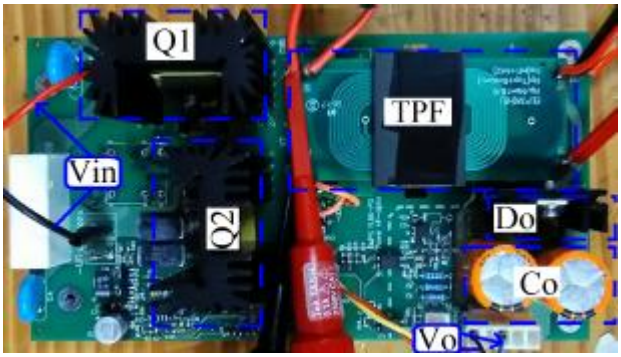


FIGURE 12. Flyback converter prototype with planar transformer.

Three different PT prototypes (PT-A, PT-B, and PT-B*) were integrated into the TSF converter to evaluate their voltage and current stresses, oscillatory behavior, efficiency, and thermal performance.

A. *PLANAR TRANSFORMER ELECTRICAL PARAMETER MEASUREMENTS*

The three PT prototypes were manufactured and tested to compare measured and simulated electrical parameters. Fig.13 shows the final physical implementations of PT-A, PT-B, and PT-B*. Electrical parameter measurements were conducted using an Agilent 4294 impedance analyzer, with results summarized in Table 5.



FIGURE 13. Photos of PT-A, PT-B, and PT-B* prototypes.

The distinction between prototypes PT-B and PT-B* (Fig. 13) lies in the winding strategy. PT-B (Interleaved and Aligned, Fig. 13b) employs a primary-secondary-secondary-primary (P-S-S-P) interleaving structure where the PCB traces are strictly aligned vertically. This configuration is designed to maximize the cancellation of MMF (Magnetomotive Force) between layers, thereby minimizing leakage inductance (L_{lk}) and reducing AC resistance (R_{ac}) caused by the proximity effect. In contrast, PT-B* (Non-Interleaved or Modified Aligned, Fig. 13c) refers to a variation where, although the layers remain aligned, the interleaving degree is reduced or the physical spacing between the primary and secondary is altered to evaluate the trade-off between parasitic capacitance (C_{pso}) and leakage inductance.

TABLE 5. Measured electrical parameters of planar and conventional transformers.

Parameters	PT-A	PT-B	PT-B*	ETD39
L_{pm} [µH] - primary	246.85	257.10	261.45	298.2
L_{sm} [µH] - secondary	28.03	28.7	29.33	26.8
N_p/N_s - turn ratio	2.96	3.33	2.99	3.33
C_{po} [pF]	20.24	17.39	55.20	55.10
C_{pso} [pF]	262.04	246.15	114.26	41.89
L_{lk} [µH] at 160 kHz	6.3	1.98	4.34	9.46
R_{pdc} - at DC [Ohm]	0.95	0.48	0.98	58.0
R_{sdc} - at DC [Ohm]	172	170	104	20
R_{pca} - at 160 kHz [Ohm]	1.58	1.42	1.72	3.30
R_{sca} - at 160 kHz [Ohm]	191	260	447	250

For reference, a conventional ETD39 transformer was also tested, using a similar design methodology but with non-interleaved windings of 25 AWG. The key geometric parameters of the planar and conventional transformers are provided in Table 6.

TABLE 6. Transformer geometric parameters comparison.

Transformer Parameter	ETD39	PT
A_e - Central lag area	127 mm^2	192 mm^2
V_e - Core Volume	11770 mm^3	8520 mm^3
L - Length	39.1 mm	75.2 mm
H - Height	30.0 mm	12.5 mm
W - Weight	39.6 mm	38.1 mm

The measured values of the planar transformer (PT) exhibited a strong correlation with the simulated results obtained using Ansys Maxwell 3D®. The two-step design methodology, which combines Ansys PExprt® for magnetic design with 2D and 3D FEA in Ansys Maxwell®, provided high accuracy and improved parameter prediction.

Maintaining insulation distances of 5.5 mm across the surface and 3.0mm for internal layer strands, along with variations in mean length of turn (MLT) between the designs, significantly affected leakage inductance (L_{lk}). This phenomenon was not captured in 2D FEA, but it became evident in 3D FEA analysis.

Comparing measured AC resistance with 3D FEA results, deviations of 3.09%, 12.9%, and 6.25% were observed for different prototypes. Similarly, leakage inductance measurements showed discrepancies of 2.86%, 15.15%, and 14.75%. These differences may be attributed to the fringing flux effect, which influences the winding behavior at high frequencies.

B. *TSF CONVERTER TESTS AND MEASUREMENTS*

The purpose of the test was to evaluate the voltage and current stresses in the planar transformer (PT), as well as its oscillatory behavior, which is directly influenced by parasitic elements such as leakage inductance (L_{lk}) and interwinding capacitance (C_{str}). The experiments were conducted at a

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switching frequency of 160 kHz, with a duty cycle of 23%. The converter operated with an input voltage of 350 V, delivering an output voltage of 48 V and an output power of 84 W.

The primary voltage and current waveforms for PT-A are shown in Fig. 14, where significant oscillations are observed when the switch turns off. This behavior results from the interaction between leakage inductance (L_{lk}) and parasitic capacitances, leading to unwanted ringing.

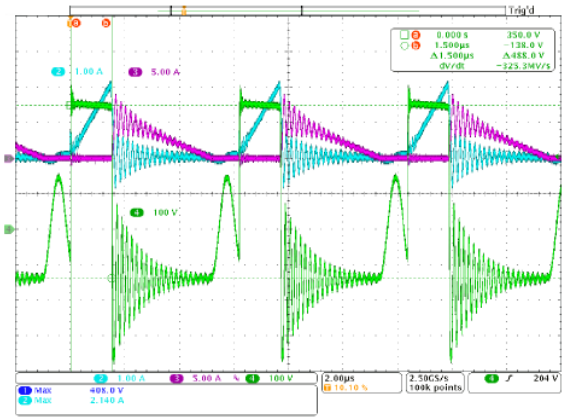


FIGURE 14. PT-A primary current and voltage waveforms.

Similarly, the secondary voltage and current waveforms for PT-A are presented in Fig. 15. While the secondary voltage oscillations are damped by the output capacitor, the secondary current waveform still exhibits noticeable ringing.

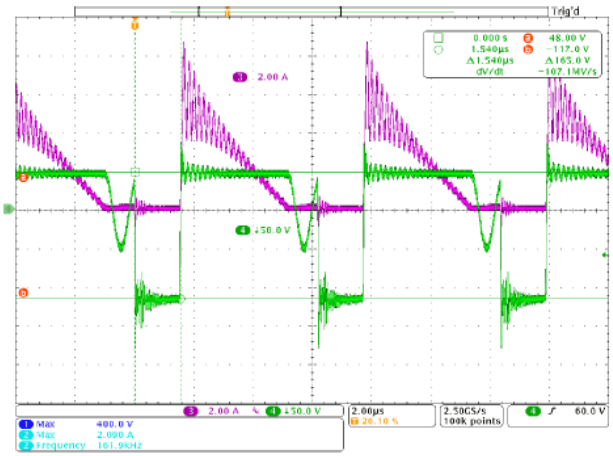


FIGURE 15 PT-A secondary current and voltage waveforms.

For PT-B, the improved transformer design resulted in faster oscillation damping, reducing the demagnetization time by approximately 40%, as shown in Fig. 16.

The corresponding secondary waveforms for PT-B, shown in Fig. 17, confirm this improvement, with significantly reduced ringing in the secondary voltage.

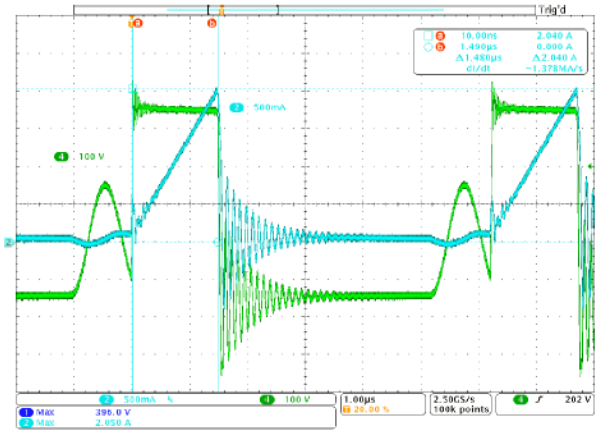


FIGURE 16. PT-B primary current and voltage waveforms.

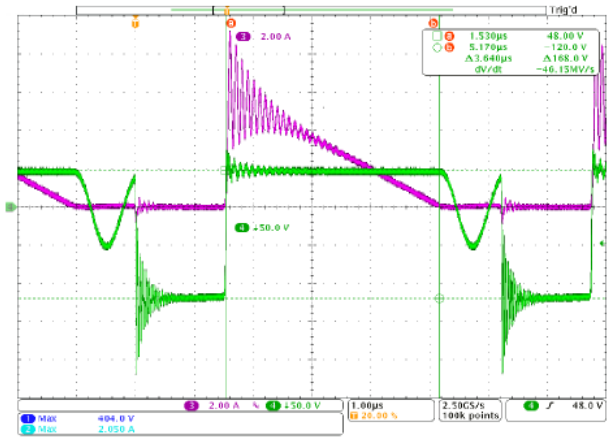


FIGURE 17. PT-B secondary current and voltage waveforms.

In contrast, PT-B* exhibited greater oscillation in the primary voltage compared to PT-B, as illustrated in Figs. 18 and 19. This behavior is attributed to the higher L_{lk} and self-capacitance (C_{po}) in PT-B*, which are approximately two and three times greater than in PT-B.

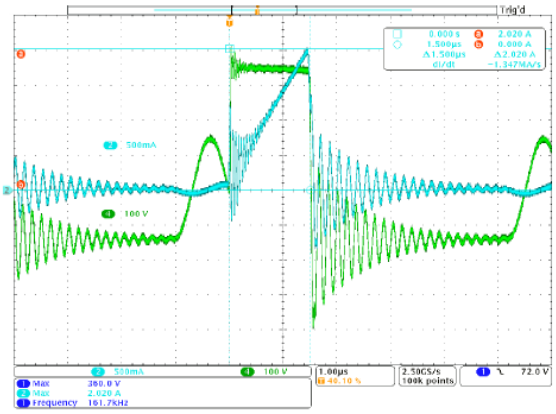


FIGURE 18. PT-B* primary current and voltage waveforms.

The high correlation between the ringing frequency observed in the experimental waveforms and the parasitic values extracted via 3D FEA confirms the model's accuracy.

Since the ringing frequency ($f_r \approx 1/2\pi\sqrt{L_{lk}C_{oss}}$) is highly sensitive to L_{lk}, the experimental match serves as an implicit validation of the transformer's parasitic characterization at the frequency of interest, making further wide-band impedance sweeps redundant for the scope of this performance optimization [15].

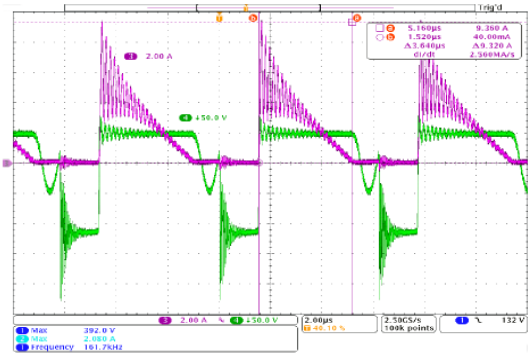


FIGURE 19. PT-B* secondary current and voltage waveforms.

C. *EFFICIENCY AND THERMAL PERFORMANCE*

The efficiency and temperature rise of each transformer configuration were evaluated under nominal operating conditions. The results are summarized in Table 7.

TABLE 7. Efficiency, losses, and temperature rise for each PT.

Parameters	PT-A	PT-B	PT-B*
*V*in - Input Voltage [V]	349.9	352.6	349.3
*P*in - Input power [W]	95.4	94.3	93.9
*P*o - Output power [W]	83.8	83.9	83.7
ρ – Efficiency [%]	87.71	88.93	89.17
Total Losses [W]	11.6	10.4	10.2
*T*amb - Environmental temperature [°C]	28.0	27.0	25.0
*T*max - Environmental temperature [°C]	77.8	65.2	59.0

Although the PT-B* prototype showed a slightly higher efficiency at Vin = 350 V (89.17%), the difference in total power losses compared to PT-B is only 0.2 W, which can be considered negligible for this operating power. Furthermore, PT-B demonstrates superior performance across the full operating range due to its optimized winding alignment and thickness, as detailed in Table 7.

Temperature measurements, illustrated in Fig. 20, further highlight these differences. The PT-A prototype exhibited the highest core temperature (77.8°C), while PT-B maintained a lower maximum temperature of 65.2°C, and PT-B achieved the lowest value at 59.0°C.

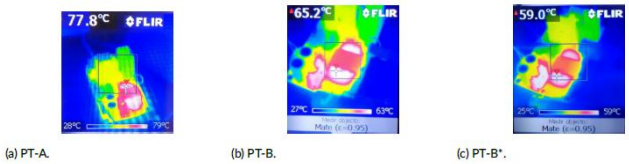


FIGURE 20. Temperature measurements for PT-A, PT-B, and PT-B*.

These results confirm that proper interleaving and winding alignment not only improve electrical performance but also contribute to lower thermal stress, extending transformer lifespan in high-frequency applications.

VI. CONCLUSIONS

This paper investigated the impact of winding arrangements on the parasitic parameters and overall performance of planar transformers for two-switch Flyback (TSF) converters. By correlating multiphysics modeling with experimental validation, it was demonstrated that the precise physical alignment and interleaving of PCB layers are the most critical factors for enhancing converter efficiency and reliability.

The comparative analysis revealed that the choice of winding arrangement can be tailored according to specific design figures of merit. Although the modified configuration (PT-B*) achieved a slightly higher peak efficiency of 89.17% at a specific operating point due to reduced capacitive losses, the interleaved and aligned winding configuration (PT-B) provides a far superior global trade-off between electrical parameters. PT-B achieved a critical 80% reduction in leakage inductance (L_{lk}), a 57% decrease in AC resistance (R_{ac}), and a 68% reduction in interwinding capacitance (C_{str}) compared to conventional or misaligned designs. This drastic reduction in leakage inductance makes PT-B globally better for the converter's overall operation, as it directly minimizes voltage spikes and high-frequency ringing on the semiconductors while reducing core temperature by up to 18.8°C.

The results highlight that while 1D analytical equations and 2D FEA offer valuable initial estimates, they fail to capture complex 3D phenomena such as fringing flux at the core gaps and the effects of track misalignment. The high correlation between 3D FEA simulations and experimental data, with leakage inductance deviations below 1%, confirms that high-fidelity electromagnetic modeling is essential for the design of high-frequency magnetic components. This approach allows for a predictable design process, ensuring that parasitic elements are optimized to reduce EMI and switching losses. Future work will explore the application of these design guidelines to higher-frequency converters and alternative core materials, further enhancing the power density and manufacturability of planar magnetics.

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N.O.SOUZA: Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Validation, Writing – Original Draft. **D.WEINZIERL:** Data Curation, Formal Analysis, Visualization, Writing – Review & Editing. **M.W.M.CARVALHO:** Data Curation, Formal Analysis, Visualization, Writing – Original Draft, Writing – Review & Editing. **R.HEINRICH:** Formal Analysis,

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PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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