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Online SoC Balancing Strategy for Distributed Single-Stage MMC-Based BESS

Juan A. P. Garay[1,*], **Pedro M. Almeida**[1], **Pedro G. Barbosa**[1]

[1]Federal University of Juiz de Fora, Graduate Program in Electrical Engineering, Juiz de Fora, MG, Brazil.

e-mails: juan.peralta@estudante.ufjf.br*, pedro.machado@ufjf.br, pedro.gomes@ufjf.br.
*Corresponding author.

ABSTRACT This paper proposes an online state-of-charge (SoC) balancing strategy for a distributed single-stage Modular Multilevel Converter-based Battery Energy Storage System (MMC-BESS). The main contribution is the development of a low-complexity sorting-based selection algorithm integrated into the smart-battery concept, enabling real-time energy redistribution among submodules without requiring additional auxiliary balancing circuits. The proposed method operates jointly with a phase-disposition pulse width modulation (PD-PWM) strategy and is coordinated with conventional grid current control in the synchronous reference frame and circulating current suppression control, thereby ensuring stable converter operation. The complete three-phase MMC-BESS, composed of 18 submodules per arm, was modeled and validated using PSCAD/EMTDC simulations. The performance of the proposed balancing algorithm was evaluated under multiple operating conditions, including active power injection, active power absorption, and reactive power support. Simulation results demonstrate effective SoC equalization across all submodules while maintaining high-quality AC voltage and current waveforms and while ensuring suppression of internal circulating currents. The simulation results confirm the robustness, scalability, and practical applicability of the proposed control strategy, highlighting its potential for improving reliability, extending battery lifetime, and enabling MMC-based BESS to provide ancillary services and support large-scale integration of renewable energy sources.

KEYWORDS Modular multilevel converter, battery energy storage systems, SoC balancing algorithm, circulating current, ancillary services.

I. INTRODUCTION

In recent years, renewable energy sources (RES), particularly photovoltaic (PV) and wind power plants, have experienced a significant increase in deployment as part of global efforts to meet the continuously rising demand for electricity and reduce dependence on fossil-based generation [1], [2]. However, despite the remarkable progress in penetration levels and technological maturity, the intrinsic variability and intermittency of these resources remain critical limitations. Such fluctuations in generation profiles often lead to operational challenges in power systems, including curtailment of available renewable energy during periods of oversupply and difficulties in maintaining grid stability and reliability [3].

In this context, Battery Energy Storage Systems (BESS) have emerged as one of the most prominent technologies to mitigate the above issues and enable the large-scale integration of renewable resources. Their modular architecture, scalability, and rapid dynamic response allow BESS to fulfill both short- and long-term system requirements, ranging from frequency and voltage regulation to peak shaving and energy arbitrage. Furthermore, their ability to be deployed across multiple voltage levels makes them highly versatile assets for applications at the generation, transmission, and distribution layers [4]–[6]. However, since battery cells inherently produce a DC output, power electronic converters are required for effective integration with the AC power grid.

Conventional two- and three-level IGBT-based converters are typically employed in low-voltage and low-power applications [7]. To achieve reliable operation at high voltage and power levels, multilevel converter topologies have emerged as an attractive solution. Among these, the Cascaded H-Bridge Multilevel Converter (CHBMC) has been proposed in the literature for its capability to achieve high output voltages and enhanced fault tolerance through the series interconnection of numerous modules. Nonetheless, CHBMC are primarily used in medium-voltage installations. Consequently, BESS applications at higher voltage levels generally require converter configurations more suitable for large-scale integration [8], [9].

Fig. 1 illustrates an alternative topology, the Modular Multilevel Converter (MMC), which structure supports different submodule (SM) configurations. Furthermore, the MMC offers enhanced scalability, improved controllability, and lower harmonic content in the synthesized voltages,

enabling more efficient and reliable grid integration. In MMC-BESS architectures, battery packs may be connected either in a centralized manner at the DC bus or distributed across the DC bus of the submodules, depending on the desired configuration and control objectives [10].

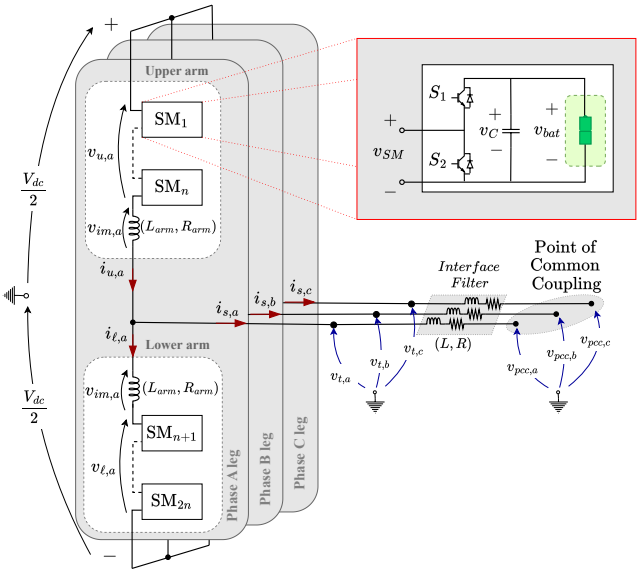


FIGURE 1. MMC-BESS connected to the system.

The centralized configuration is less attractive since achieving the DC bus voltage requires long battery strings, increasing complexity and potentially reducing system reliability. On the other hand, the distributed approach exploits converter modularity, with batteries connected directly to each SM (single-stage) or interfaced via DC-DC bidirectional converters (two-stage), improving efficiency, reliability, and control flexibility [11], [12]. However, unequal charging and discharging among the energy storage SM can accelerate battery degradation, impact the overall performance, and compromise system reliability. To alleviate these issues, effective equalization control is essential. Consequently, recent research on MMC-BESS systems has focused on state-of-charge (SoC) balancing strategies, SoC equalization thresholds, and state-of-health (SoH) management.

Focusing only on SoC balancing, several methods have been proposed in the literature and can be grouped into dissipative, capacitor-based, inductor-based, transformer-based, and converter-based strategies.

In [13], the authors investigated fixed resistor-based balancing as a simple and low-cost solution, dissipating surplus energy as heat, and experiments confirmed that parameter optimization could improve pack consistency. However, the intrinsic energy waste and the associated thermal burden remain critical drawbacks. In [14], the authors proposed a hierarchical switched-resistor scheme designed to reduce balancing time and energy loss compared with conventional adjacent cell-to-cell methods, but the requirement for multiple balancing circuits still increases complexity and cost at larger scales. These dissipative methods illustrate the trade-off between simplicity and efficiency.

To overcome the above issues, capacitor- and inductor-based solutions have been explored. In [15], a double-tiered switched-capacitor method was presented, achieving faster charge redistribution than single-tier approaches, but at the cost of higher circuit complexity and switching losses. In [16], a single-inductor balancing circuit with SoC-based logic was investigated, where rapid equalization was demonstrated under hybrid electric vehicle conditions, though the bulky inductor and precise current regulation remain limiting factors. In [17], the authors proposed a multi-switched inductor balancing scheme controlled by fuzzy logic, which improved balancing speed and recovered capacity compared to PI-based controllers. Nevertheless, the increased number of switches and sophisticated control algorithms add cost and reduce reliability in large-scale applications.

Transformer- and converter-based balancing methods offer greater flexibility but introduce new challenges. In [18], a multi-winding transformer configuration was introduced, enabling bidirectional energy redistribution and showing measurable improvements in pack capacity, although its cost and physical size restrict scalability. In [19], the authors presented a time-shared flyback topology that allows regenerative energy transfer with fewer components, but sequential operation limits its balancing speed. Converter-based approaches were also proposed: in [20], a buck–boost design integrated with a neural-network-based BMS was developed, which achieved accurate SoC estimation but at the expense of higher control overhead. In [21], the authors proposed a Cuk converter with fuzzy control, which provided fast and efficient equalization but increased circuit complexity. In [22], the authors developed a cell-to-cell equalization system using a bidirectional flyback-based converter, achieving high balancing efficiency, although the design requires multiple magnetic components, which increases system bulk and complexity. In [23], a cascaded full-bridge multilevel converter was proposed, enabling direct cell-level SoC balancing without auxiliary circuits; however, the scalability of this method for very large packs is constrained by control and management complexity. Finally, in [24], a quasi-resonant zero-current-switching bidirectional converter was introduced, offering soft-switching operation and reduced losses, but its reliance on precise resonance conditions makes control design more challenging and sensitive to parameter variations.

As a contemporary method in SoC balancing, the concept of smart batteries has emerged as a promising strategy, as demonstrated in [25]. In this approach, each individual cell is directly interfaced with a dedicated power converter, which enables decentralized control and significantly increases the flexibility of battery management.

By allowing independent regulation of each cell within the submodules, this configuration enhances efficiency, and supports more adaptive operating conditions.

More recently, SoC balancing strategies specifically applied to MMC-based battery energy storage systems have started to attract increasing attention in the literature. In [26], the authors proposed a SoC balancing strategy for a grid-scale three-phase BESS based on a hybrid MMC topology composed of cascaded H-bridges and L-bridges, where the balancing process is achieved through current-prioritized cell activation criteria. Although the method improves cell utilization and enables redundant cell management, the converter structure and balancing strategy rely on additional switching stages and hybrid converter arrangements.

In [27], a three-layer SoC balancing strategy for MMC-BESS was developed together with power fluctuation suppression, PCC voltage regulation, and harmonic mitigation functions in grid-connected wind farms. The proposed approach reconstructs the modulation signals of the submodules and employs additional circulating current control actions to redistribute energy among phases, arms, and submodules. However, the balancing process becomes strongly dependent on multiple coordinated control loops and modulation reconstruction stages.

A distributed sequential balancing strategy based on consensus control theory was proposed for MMC-BESS in [28]. The local controllers exchange information among adjacent submodules to achieve energy consensus across different converter layers. Despite the scalability advantages of the distributed framework, the method requires sequential energy balancing procedures and distributed communication among submodules. Similarly, in [29], a double closed-loop decoupling control and voltage equalization strategy for MMC-BESS was introduced, combining AC-side power regulation with additional equalization control loops. Although satisfactory balancing performance was reported, the equalization process depends on supplementary voltage balancing controllers integrated into the converter control structure.

Different from the aforementioned approaches, the strategy proposed in this work performs the SoC balancing process directly during the submodule selection stage of the PD-PWM modulation strategy. The proposed algorithm employs an online sorting-based criterion associated with the instantaneous arm current direction, enabling the MMC-BESS itself to redistribute energy among the submodules without requiring hybrid converter structures, distributed communication frameworks, modulation reconstruction procedures, or additional equalization control layers.

A. Motivation and contribution of the work

Despite the growing interest in SoC balancing strategies for MMC-based battery energy storage systems, several challenges still remain regarding the integration of balancing algorithms with the modulation and control structure of distributed single-stage MMC-BESS configurations.

Bearing in mind the fundamentals presented in [30], this work introduces an online SoC balancing algorithm integrated into the smart battery concept, employing a sorting-based control mechanism [31]. The proposed method is implemented in a three-phase MMC-BESS configured in a double-star topology with a distributed single-stage battery arrangement. SoC balancing performance is evaluated under multiple converter operating conditions, including both active and reactive power exchanges with the grid. The developed approach is verified through digital simulations in PSCAD/EMTDC, considering an MMC-BESS comprising 18 submodules per arm.

Although the present work focuses specifically on the SoC balancing problem in MMC-BESS applications, reliability aspects associated with battery aging and submodule fault conditions are also relevant in large-scale distributed energy storage systems. In this context, the modular structure of the MMC facilitates maintenance procedures and allows faulty or degraded submodules to be isolated or bypassed without compromising the overall converter operation. However, detailed fault diagnosis and state-of-health (SoH) management strategies are beyond the scope of this paper and remain topics for future investigation.

Therefore, the main contributions of this paper are summarized as follows:

- A comprehensive investigation of the SoC balancing problem in MMC-BESS architecture operating under the smart battery concept;
- The development of an online SoC balancing algorithm based on a sorting technique, ensuring reduced complexity and enhanced practical applicability;
- Assessment of the proposed algorithm under multiple operating conditions, such as active and reactive power exchange/support, confirming its effectiveness in maintaining stable and well-balanced operation across all cases.

The remainder of this paper is organized as follows. Section II presents the fundamental principles of the modular multilevel converter integrated with a battery energy storage system, along with the employed modulation scheme and the SoC balancing algorithm proposed in this work. Section IV presents the mathematical modeling and control design for the AC current regulation and circulating current suppression implemented in the MMC. Section V discusses the digital simulation results, validating the proposed strategies. Finally, Section VI summarizes the main findings and presents the conclusions of the study.

II. MMC-BESS BASIC CONFIGURATION

Fig. 1 presents the single-stage, distributed, three-phase MMC-BESS configuration used in this work. The converter consists of three legs, each one composed of an upper arm

(positive pole) and a lower arm (negative pole). Every arm contains N series-connected submodules along with an arm inductor L_{arm}. The resulting arm impedance consists of the inductance and the equivalent conduction resistance R_{arm}, which accounts for the inductor losses and the on-state resistance of the semiconductor switches within each SM. On the AC grid side, each converter output terminal is connected in series with a first-order filter modeled by an inductor L and its equivalent conduction resistance R. The half-bridge submodule (HBSM) was adopted due to its simplicity and lower cost compared with other versatile topologies [32]. The MMC's DC terminals are left open because the BESS architecture is distributed, meaning that each submodule (SM) contains its own battery unit.

Fig. 2 shows a detail of the configuration of the MMC-BESS submodule. Each half-bridge SM consists of two insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes, operated in a complementary manner to produce two distinct switching states: inserted and bypassed, as listed in Table 1. In the inserted state, the upper IGBT is turned on and the lower device is turned off, causing the SM output voltage to equal the battery pack voltage, which corresponds to the DC-link capacitor voltage. Conversely, in the bypassed state, the upper IGBT is turned off and the lower device is turned on, resulting in zero voltage at the SM terminals.

TABLE 1. Operating modes of the HBSM.

Status	S_1	S_2	v_{SM}
Inserted	1	0	v_{bat}
Bypassed	0	1	0

As depicted in Fig. 2, in the single-stage configuration, the batteries are directly connected to the submodule (SM) DC terminals, reducing conversion losses and simplifying the SM architecture. However, this configuration imposes more stringent requirements on SoC estimation accuracy, submodule-level balancing strategies, and voltage control.

The battery pack model is derived from a simplified version of the Electrical Performance (EP) model for Lithium-ion cells, providing a practical balance between modeling accuracy and computational efficiency for system-level simulations. This formulation enables straightforward scaling from a single cell to a complete pack through the parameters N_s and N_p, which define the number of series-connected cells and the number of parallel-connected strings, respectively. These scaling factors determine the pack's nominal voltage, current capability, energy capacity, and dynamic response under varying load conditions.

The scalability is particularly important in distributed MMC-BESS architectures, where each SM incorporates an independent battery unit composed of numerous cells. In this work, to ensure realistic electrochemical behavior, the Kokam SLPB120216216 Lithium-ion cell model [33] was selected due to its well-documented performance characteristics, high-power capability, and widespread adoption in advanced energy storage systems.

Fig. 3 shows the open-circuit voltage versus SoC ($e_{bat}\times$SoC) and internal resistance versus SoC ($R_{bat}\times$SoC) characteristic curves for the Kokam SLPB120216216 lithium-ion cell. The no-load battery voltage e_{bat} is modeled as a function of both the battery current i_{bat}, and the state-of-charge, thereby incorporating variations associated with different discharge rates and temperature-dependent characteristics. This controlled voltage source is connected in series with the internal resistance R_{bat}, which represents the cell ohmic losses.

Unlike conventional approaches based on a constant internal resistance, this work adopts a variable-resistance model in which R_{bat} is defined as a function of the SoC through a look-up table, as illustrated in Fig. 2. The corresponding characteristic curve, presented in Fig. 3, was obtained from battery discharge tests performed under variable temperature conditions, considering an initial temperature of 23°C. This modeling approach enables the influence of operating conditions on battery behavior to be represented more accurately, improving model fidelity while maintaining a computational complexity suitable for system-level MMC-BESS simulations.

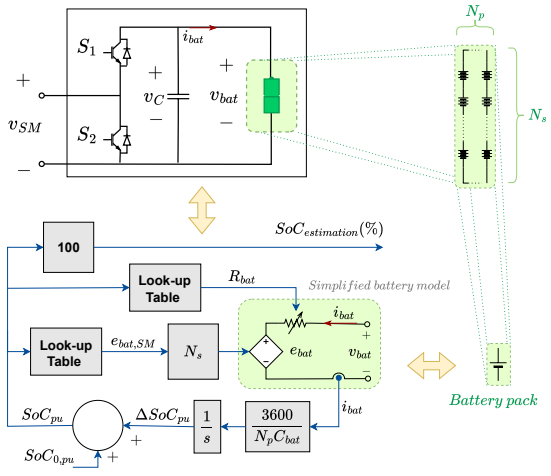
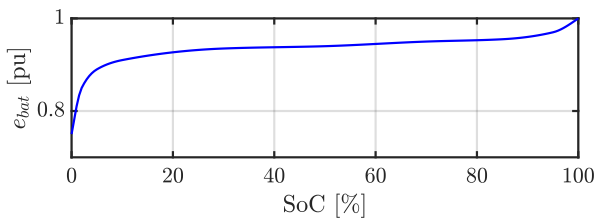


FIGURE 2. Battery pack model connected to the HBSM.

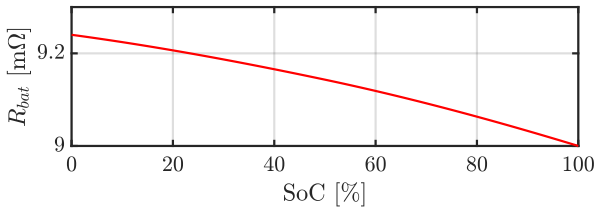
Similarly, the total number of SM per arm is established based on the rated DC bus voltage of the MMC-BESS and the system's energy storage requirements, thereby guaranteeing sufficient energy buffering and operational flexibility [34].

III. THE PROPOSED SoC BALANCING ALGORITHM

Assuming that each battery pack connected to the MMC-BESS submodules is supervised by a dedicated Battery Management System (BMS), an additional supervisory balancing layer at the converter level is



(a) Open-circuit voltage versus SoC



(b) Internal resistance versus SoC

FIGURE 3. Kokam SLPB120216216 Lithium-ion cell curves.

still required to ensure homogeneous energy distribution among all SM. Although the local BMS is capable of monitoring and protecting the individual battery cells, unequal power processing among the submodules naturally leads to progressive divergence of their SoC values during converter operation. As a consequence, some SM may become overcharged or excessively discharged earlier than the remaining units, thereby reducing the usable energy capacity of the converter and accelerating battery degradation.

This issue becomes even more critical in distributed MMC-BESS architectures, since the batteries are directly connected to the submodules. Consequently, the converter modulation strategy itself determines how much energy is processed by each battery pack during every switching interval. In this context, the balancing strategy must operate continuously, acting directly on the SM selection process to redistribute the processed energy among all SM of each converter arm.

The balancing method proposed in this work is integrated with the multicarrier modulation strategy described in Section IV. Instead of directly generating the gating signals for the semiconductor switches, the modulation stage first determines how many SM must be inserted in each arm at every sampling instant. Subsequently, the balancing algorithm decides which specific SM will be activated according to their instantaneous SoC values and the direction of the arm current.

The proposed strategy is inspired by the capacitor voltage balancing principle commonly employed in conventional MMC [31]. However, instead of regulating capacitor voltages, the algorithm operates directly on the battery SoC values, enabling energy equalization among the distributed storage units while preserving the normal power conversion functionality of the MMC-BESS.

Initially, the controller acquires the instantaneous SoC values associated with all submodules of the upper and lower arms. For a generic converter phase, the SoC vector associated with one converter arm can be represented as:

$$\mathbf{SoC}_k^j = \left[SoC_k^j(1), SoC_k^j(2), \ldots, SoC_k^j(N)\right], \quad (1)$$

where $SoC_k^j(n)$ represents the state-of-charge of the n^{th} submodule connected to the arm $j \in \{u, \ell\}$, corresponding to the upper (u) or lower (ℓ) arm of phase $k \in \{a, b, c\}$, and N is the total number of submodules per arm. In this work, $N = 18$.

The average SoC value of each arm is continuously calculated according to:

$$\overline{SoC}_k^j = \frac{1}{N}\sum_{n=1}^{N} SoC_k^j(n), \quad (2)$$

where $\overline{SoC}_k^j$ corresponds to the mean energy level stored in the batteries of a given arm. This quantity acts as the equilibrium point toward which all submodules converge during the balancing process.

Simultaneously, the AC current controller and the circulating current suppression controller generate the modulation references responsible for synthesizing the converter terminal voltages and compensating the internal circulating currents. Based on these control loops, the reference voltages for the upper and lower converter arms are obtained as:

$$v_{j,k}^* = \frac{V_{dc}}{2} \mp v_{t,k}^* - v_{im,k}^*, \quad (3)$$

where $v_{j,k}^*$ is the reference voltages for the arm j of phase k, V_{dc} is the equivalent MMC-BESS DC bus voltage, $v_{t,k}^*$ is the converter terminal voltage reference generated by the AC current controller, and $v_{im,k}^*$ is the imbalance voltage produced by the circulating current suppression controller (CCSC).

The signals given by (3) are compared with the N triangular carriers of the PWM strategy. As a result of this comparison, the controller determines the number of submodules that must remain inserted in each converter arm during the corresponding switching interval. These quantities are represented by $SM_{k,on}^u$ and $SM_{k,on}^\ell$ for the upper and lower arms, respectively.

Once the required number of inserted SM is determined, the balancing stage begins. The complete algorithm implemented in the embedded controller is based on a sorting routine executed online at every sampling period. The fundamental objective is to prioritize the insertion of the submodules that most contribute to reducing the SoC dispersion within the arm.

For this purpose, all SoC values are arranged in ascending order using the Bubble Sort algorithm [34]. The ordered vector can be represented as:

$$\mathbf{SoC}_{k,ord}^j = \left[SoC_k^j(ord(1)), \ldots, SoC_k^j(ord(N))\right], \quad (4)$$

where $ord\,(n)$ denotes the index associated with the reordered position of each SM after the sorting procedure. Consequently,

$$SoC_k^j\,(ord\,(1)) \leq \cdots \leq SoC_k^j\,(ord\,(N))\,. \tag{5}$$

Therefore, the first positions of the vector correspond to the least charged SM, whereas the last positions correspond to the most charged ones.

The balancing decision is then performed according to the instantaneous direction of the arm current. Since the MMC SM process energy differently depending on the current polarity, the arm current naturally defines whether the inserted batteries are being charged or discharged.

When the arm current is positive,

$$i_j > 0\ , \tag{6}$$

the energy flow occurs from the AC system toward the batteries, characterizing a charging interval for the inserted submodules. Under this operating condition, the balancing algorithm prioritizes the insertion of the least charged batteries, allowing them to absorb more energy and increase their SoC values faster than the remaining SM.

Consequently, the controller activates the first SM_{on}^j positions of the ordered vector according to:

$$S_k^j\,(ord\,(n)) = 1, \qquad n = 1, 2, \ldots, SM_{k,on}^j\ , \tag{7}$$

where $S_k^j\,(ord\,(n))$ represents the switching state associated with the selected SM. When $S_k^j\,(ord\,(n)) = 1$, the corresponding SM is inserted into the converter arm. Conversely, when $S_k^j\,(ord\,(n)) = 0$, the SM remains bypassed.

On the other hand, when the arm current becomes negative,

$$i_j < 0\ , \tag{8}$$

the inserted batteries deliver energy to the converter and consequently discharge. Under this condition, the balancing strategy prioritizes the most charged submodules, forcing them to process more power and reducing their SoC levels.

Therefore, the controller activates the last positions of the ordered vector according to:

$$S_k^j\,(ord\,(n)) = 1, \quad n = \left(N - SM_{k,on}^j + 1\right), \ldots, N. \tag{9}$$

This operating principle allows the converter itself to redistribute energy among the batteries without requiring additional equalization circuits, dissipative resistors, auxiliary DC-DC converters, or external balancing hardware.

The complete balancing criterion can therefore be summarized as:

$$\begin{cases} \text{Insert SM with the lowest SoC values,} & i_j > 0 \\ \text{Insert SM with the highest SoC values,} & i_j < 0 \end{cases}. \tag{10}$$

The proposed balancing routine is executed online at every sampling instant, continuously selecting the appropriate submodules according to their instantaneous SoC values and the arm current direction. Consequently, the energy distribution among the 18 SM is progressively equalized during normal MMC-BESS operation. The complete balancing logic implemented in the controller is summarized in Fig. 4.

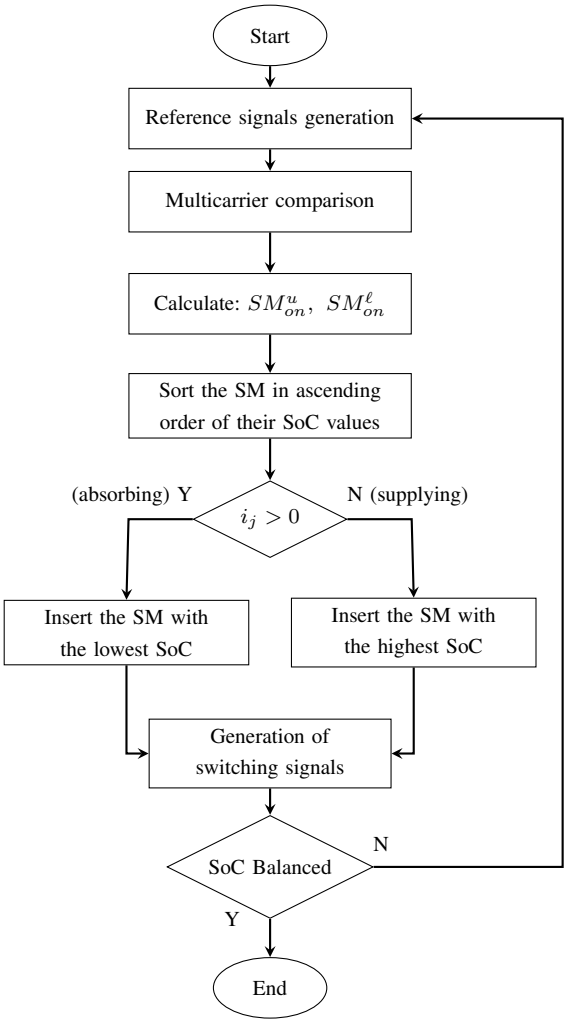


FIGURE 4. Flowchart of the SoC balancing algorithm.

Overall, the balancing routine progressively reduces the SoC dispersion among the submodules, promoting a more uniform energy distribution within the converter arms during normal MMC-BESS operation. Additional details regarding this methodology are presented in [34].

IV. OVERALL MMC-BESS CONTROL ARCHITECTURE

The MMC-BESS was modeled with two coordinated control loops to regulate the AC-side currents and suppress internal circulating currents. The first loop implements the classical grid current control in the synchronous reference frame (SRF) [35], generating *dq*-axis current references that define the converter terminal voltage references. This approach enables independent regulation of active and reactive power exchanged at the MMC-BESS terminals.

The second loop is dedicated to circulating current suppression control (CCSC), aiming to mitigate internal

circulating currents within the converter arms [36]. Although the DC component of these currents is inherently zero due to the open-circuit condition at the DC side of the MMC-BESS, undesirable AC components may still arise. To eliminate them, zero circulating current references are imposed, allowing the controller to produce compensating signals associated with arm voltage imbalances.

Finally, the reference voltages generated by the control loops are combined and processed by the modulation stage. These signals are continuously compared with multiple level-shifted carrier waveforms to determine the number of active submodules required in each converter arm at every switching instant. Based on this comparison, the modulation stage generates the corresponding SM insertion commands, thereby defining the instantaneous switching states of the MMC-BESS.

A. Control of the AC Currents

By neglecting the harmonic components generated by the converter in Fig. 1 and assuming a balanced three-phase power system, the dynamic equations of the MMC-BESS can be expressed in the synchronous reference frame (SRF) as follows:

$$v_{t,d} - v_{pcc,d} + \omega L_{eq} i_{s,q} = L_{eq} \frac{di_{s,d}}{dt} + R_{eq} i_{s,d} \ , \quad (11)$$

$$v_{t,q} - v_{pcc,q} - \omega L_{eq} i_{s,d} = L_{eq} \frac{di_{s,q}}{dt} + R_{eq} i_{s,q} \ , \quad (12)$$

where $v_{t,d}$ and $v_{t,q}$ denote the MMC-BESS terminal voltages in the *dq* reference frame, $v_{pcc,d}$ and $v_{pcc,q}$ represent the voltages at the point of common coupling (PCC), and $i_{s,d}$ and $i_{s,q}$ correspond to the MMC-BESS output currents, all expressed in *dq* coordinates. The equivalent inductance and resistance seen from the converter terminals are defined as $L_{eq} = \left(L + \frac{L_{arm}}{2}\right)$ and $R_{eq} = \left(R + \frac{R_{arm}}{2}\right)$, respectively.

Applying the Laplace transform to (11) and (12), and isolating the MMC-BESS output currents, while considering that $V_{t,dq}(s) = m_{s,dq}\,(V_{dc}/2)$, one can write:

$$I_{s,d}(s) = \left(\frac{1}{sL_{eq} + R_{eq}}\right)\left[m_{s,d}\left(\frac{V_{dc}}{2}\right) - V_{pcc,d}(s) + \omega L_{eq} I_{s,q}(s)\right] \ , \quad (13)$$

$$I_{s,q}(s) = \left(\frac{1}{sL_{eq} + R_{eq}}\right)\left[m_{s,q}\left(\frac{V_{dc}}{2}\right) - V_{pcc,q}(s) - \omega L_{eq} I_{s,d}(s)\right] \ , \quad (14)$$

where $m_{s,d}$ and $m_{s,q}$ are the direct- and quadrature-axis modulation indices, respectively, and V_{dc} is the DC-bus voltage of the MMC-BESS.

Thus, by controlling $m_{s,d}$ and $m_{s,q}$, it is possible to regulate the currents $I_{s,d}(s)$ and $I_{s,q}(s)$ through the adjustment of the terminal voltages synthesized by the MMC-BESS [37]. Therefore, by defining two new control variables, $U_{s,d}(s)$ and $U_{s,q}(s)$, the block diagram shown in Fig. 5 can be derived for the AC current control of the MMC-BESS.

B. Control of Circulating Currents

Even after balancing the SoC values and equalizing the output voltages of the submodules, energy transfer will still occur between the converter's SM, resulting in a

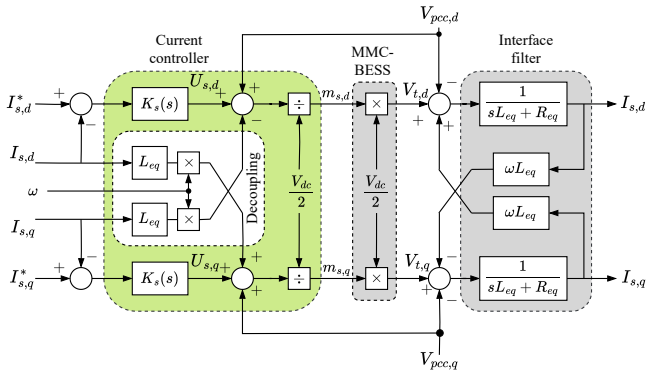


FIGURE 5. Block diagram of the MMC-BESS control architecture.

current flow between the arms of the MMC-BESS. These internal currents, also referred to as circulating currents, primarily consist of oscillating components, which include even harmonic multiples of the fundamental frequency of the AC grid current, with the predominant component being the second harmonic (2ω).

Therefore, considering the current directions indicated in Fig. 1, the following relations can be written for the circulating currents:

$$i_{circ,k} = \left(\frac{i_{u,k} + i_{\ell,k}}{2}\right) \ , \quad (15)$$

where $i_{u,k}$ and $i_{\ell,k}$ are the currents in the upper and lower arms, respectively, and $k \in \{a, b, c\}$.

Although the internal currents do not directly affect the AC currents synthesized by the MMC-BESS, they increase the RMS value of the currents in the converter arms, leading to additional losses and a reduction in overall efficiency. Therefore, it is crucial to compensate for these currents to prevent the oversizing of the converter components [38].

In order to ensure complete compensation of the internal currents through the converter arms, the direct control technique known as circulating current suppression control (CCSC) is employed [36]. In this way, by adopting the same procedure described in the previous section, the following expressions can be derived in the synchronous reference frame for the circulating currents:

$$I_{circ,d}(s) = \left(\tfrac{1}{sL_{arm}+R_{arm}}\right)[V_{im,d}(s) - 2\omega L_{arm} I_{circ,q}(s)], \quad (16)$$

$$I_{circ,q}(s) = \left(\tfrac{1}{sL_{arm}+R_{arm}}\right)[V_{im,q}(s) + 2\omega L_{arm} I_{circ,d}(s)], \quad (17)$$

where $V_{im,d}(s) = m_{i,d}(V_{dc}/2)$ and $V_{im,q}(s) = m_{i,q}(V_{dc}/2)$ are the imbalance voltages in the converter arms in the *dq* coordinates, respectively.

Normalizing (16) and (17) with respect to V_{dc}, the following control laws for the circulating currents of the converter can be written:

$$m_{i,d} = \left(\tfrac{2}{V_{dc}}\right)[U_{im,d}(s) + 2\omega L_{arm} I_{circ,q}(s)] \ , \quad (18)$$

$$m_{i,q} = \left(\tfrac{2}{V_{dc}}\right)[U_{im,q}(s) - 2\omega L_{arm} I_{circ,d}(s)] \ , \quad (19)$$

where $U_{im,d}(s)$ and $U_{im,q}(s)$ are the new control variables.

Based on (16)–(19), the block diagram shown in Fig. 6 can be designed for the decoupled direct control of circulating currents in the synchronous reference frame. In this scheme, proportional–integral controllers $K_{circ}(s)$ process the errors between the measured currents and their reference values, generating the imbalance voltage references that the arms of the MMC-BESS must synthesize in order to suppress these undesired currents.

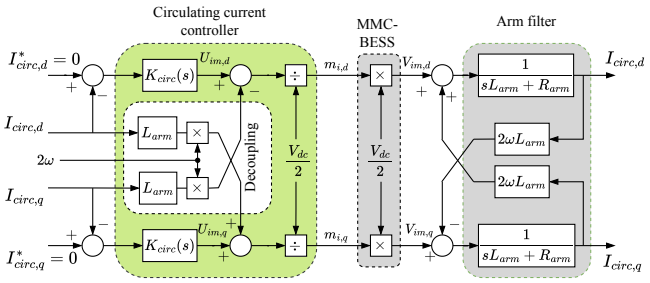


FIGURE 6. Block diagram of the circulating current control.

In Fig. 6, the references $I^*_{circ,d}$ and $I^*_{circ,q}$ are set to zero to suppress the internal circulating currents of the MMC. As a result, the control loop output together with the inverse Park transformation, operating at a rotating frequency of 2ω, generates the reference signals in the *abc* frame associated with the arm imbalance voltages.

C. Modulation Strategy

As mentioned previously, the signals $v^*_{t,k}$ and $v^*_{im,k}$, generated respectively by the grid current controller and the CCSC loop, are combined before being compared with the multiple triangular carrier waveforms in order to generate the switching patterns for the MMC semiconductor switches.

Several multicarrier pulse-width modulation (PWM) strategies have been proposed in the literature for multilevel converters [39]. They are grouped into phase-shifted carrier-based PWM (PS-PWM) and level-shifted carrier-based PWM (LS-PWM) schemes.

In contrast to the phase-shifted carrier-based PWM, the level-shifted carrier-based PWM techniques vertically offsets the carriers within the same amplitude range, thereby dividing the modulation window into N distinct bands corresponding to the number of submodules (SM) per arm. The main variants include phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) [31]. These techniques exhibit different trade-offs between harmonic distortion and switching losses [40].

In this work, the PD-PWM strategy was adopted. However, instead of directly generating the switching patterns for the semiconductor switches, the comparison between the reference signals and the N level-shifted triangular carrier waveforms determines the number of active submodules required in each arm of the MMC-BESS. More details regarding this modulation strategy can be found in [31].

The number of active SM obtained from the modulation stage is subsequently combined with the SoC balancing algorithm described in Section III. Based on the arm current direction and the SoC values of the submodules, the balancing algorithm determines which SM must be inserted or bypassed at each switching instant, thereby redistributing the processed energy among the submodules of each converter arm [30].

Fig. 7 shows a summary of the control structure implemented for the operation of the MMC-BESS, where $SM^j_{k,n}$ refers to the n^{th} SoC value of each submodule in each phase, associated with the upper (^{u}) or lower ($^\ell$) arm. Regardless of the SoC balancing algorithm, the synthesized output voltage waveform can exhibit $(N+1)$ or $(2N+1)$ levels, depending on whether a single reference or a pair of complementary reference signals are compared to the triangular carriers [34].

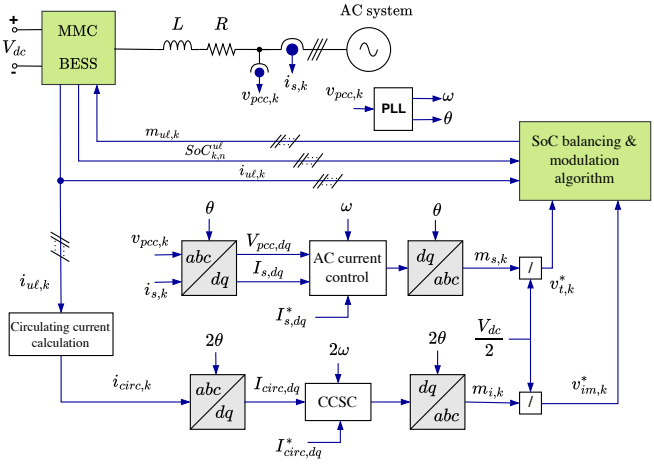


FIGURE 7. Block diagram of the MMC-BESS control structure.

V. SIMULATION RESULTS

The three-phase MMC-BESS shown in Fig. 1 was implemented in the PSCAD electromagnetic transient simulation program using 18 submodules (SM) per converter arm. The arm inductance and SM capacitance were initially designed considering the operation of the MMC as a static synchronous compensator (STATCOM), based on the methodology proposed in [41]. The design parameters were: the MMC apparent power $S_{mmc} = 50.0\,\text{MVA}$, the equivalent capacitor time constant $H = 15\,\text{ms}$, and a resonant angular frequency $\omega_r = 2 \times 377\,\text{rad/s}$. The remaining system parameters and controller gains are listed in Table 2 and Table 3, respectively. As depicted in Fig. 2, the batteries are directly connected to the DC terminals of the submodules, thereby simplifying the SM architecture.

A phase-locked loop (PLL) tracks the phase angle and frequency of the AC system voltage, enabling the

transformation of MMC-BESS voltages and currents into the synchronous dq-reference frame. Using the angle provided by the PLL and adopting a grid-voltage-oriented reference frame, the q-axis current component regulates the active power exchanged by the converter, whereas the d-axis current component controls the reactive power.

Furthermore, the control algorithm framework incorporates an SoC-based sorting and selection algorithm for submodule management, implemented in conjunction with PD-PWM, as presented in Section II.

The performance of the MMC-BESS is evaluated by imposing step variations in the synthesized converter current references along the direct and quadrature axes. Three operating scenarios are investigated, considering the MMC-BESS injecting and absorbing active power at its AC terminals, as well as providing reactive power support to the AC power system. In all simulation cases, the SoC of the batteries connected to the 18 submodules (SM) per arm is initially distributed uniformly within the range of 47% to 52% of battery capacity.

TABLE 2. Simulation Parameters.

Parameter	Value
MMC-BESS DC bus voltage (V_{dc})	30 kV
Phase RMS voltage ($V_{s,k}$)	6.124 kV
MMC-BESS arm inductance (L_{arm})	6.4 mH
MMC-BESS arm resistance (R_{arm})	1 mΩ
Series interface inductance (L)	3.2 mH
Series interface resistance (R)	1.0 mΩ
Number of SM per pole (N)	18
Battery pack rated capacity (Q)	53 A h
Battery pack nominal voltage (V_{bat})	1,66 kV
Loss of capacity at nominal discharge current	20 %
Initial SoC range	47-52 %
SM capacitance (C)	4950 µF
PWM carrier frequency (f_{sw})	1260 Hz
Grid fundamental frequency (f_s)	60 Hz

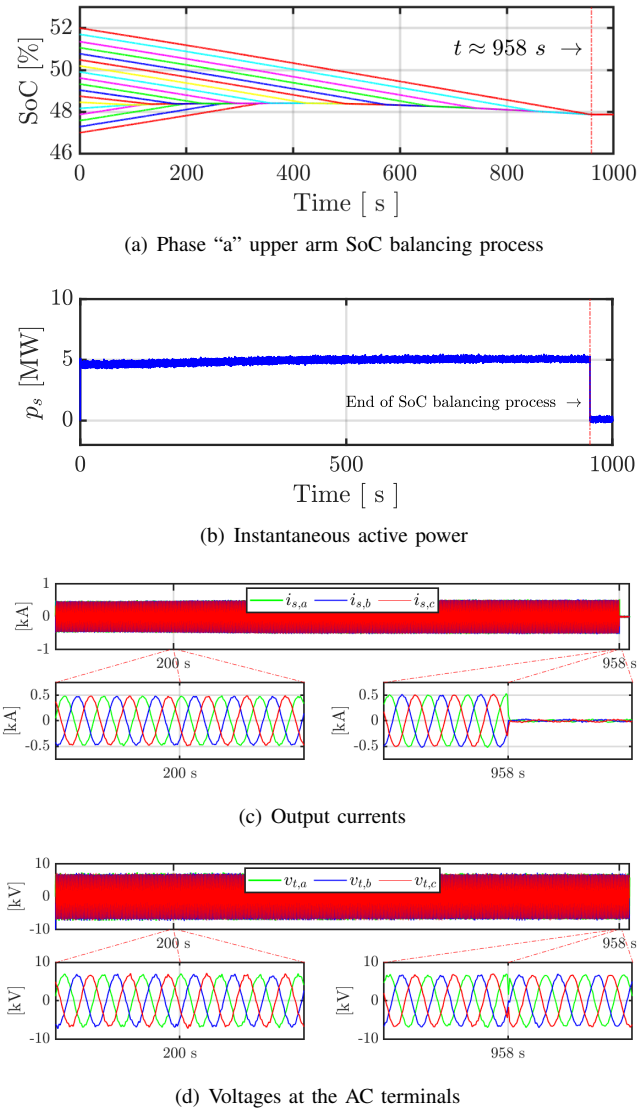
TABLE 3. Controller Gains.

Parameter	Value
Current controller proportional gain ($k_{p,s}$)	10 V/A
Current controller integral gain ($k_{i,s}$)	3 V/As
CCSC loop proportional gain ($k_{p,circ}$)	12 V/A
CCSC loop integral gain ($k_{i,circ}$)	1 V/As

A. MMC-BESS Supplying Active Power

In this simulation case, the MMC-BESS injects 5 MW into the grid by applying a reference current of 0.5 kA to the q-axis current component of the converter controller. Fig. 8(a) depicts the dynamic response of the proposed SoC balancing strategy during the discharging interval of the submodule (SM) batteries in the MMC-BESS. The SoC equalization among the SM batteries of each arm is achieved at approximately $t \approx 958$ s.

It can be observed that, initially, the submodules whose battery SoC values are below the average arm SoC are partially charged until they converge to the arm average value. After reaching this level, these SM are discharged together with the remaining submodules, preserving equalization with the corresponding arm average SoC until full balancing is achieved. Once the SoC equalization among the 18 SM in the arm is completed, the reference current $I^*_{s,q}$ is set to zero, as shown in Fig. 8(b). Since the MMC-BESS stops injecting power to AC system, from this time forward, the SoC of the batteries remain equalized and constant at 47.8%. In practical applications, the MMC-BESS can continue injecting power to the grid until the batteries reach their minimum capacity.



(a) Phase "a" upper arm SoC balancing process

(b) Instantaneous active power

(c) Output currents

(d) Voltages at the AC terminals

FIGURE 8. MMC-BESS behavior during SoC balancing process by discharging the batteries.

Fig. 8(c) and Fig. 8(d) show the currents and voltages synthesized by the MMC-BESS during the SoC balancing

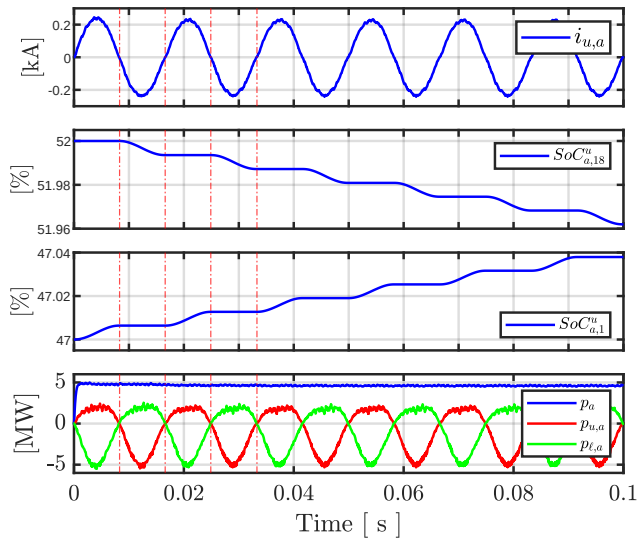


FIGURE 9. Dynamics behavior of phase "a" upper arm in detail during Case A.

process, respectively. The output currents present an average total harmonic distortion (THD) of 1.48% at $t = 200$ s, which progressively decreases as the SoC values converge, reaching 1.39% toward the end of the balancing interval. Similarly, the converter terminal voltages exhibit an RMS value of 5.62 kV, with an average THD of 3.03% at $t = 200$ s, reducing to 2.44% immediately prior to the completion of the SoC equalization process.

Fig. 9 illustrates a detailed view of the dynamic behavior of the upper arm of phase "a" during the initial stage of the SoC balancing process shown in Fig. 8(a). For simplicity, in addition to the upper-arm current waveform $i_{u,a}$, only the waveforms of the submodules exhibiting the highest and lowest SoC values are presented, namely $SoC^u_{a,18}$ and $SoC^u_{a,1}$, respectively.

Note that, although the MMC-BESS is delivering active power to the AC system, $SoC^u_{a,1}$ increases during the positive half-cycle of the upper-arm current $i_{u,a}$, indicating that the battery pack of this submodule is being charged, while $SoC^u_{a,18}$ remains constant. During the negative half-cycle of the arm current, the 18^{th} submodule is discharged, whereas the 1^{st} submodule is bypassed. This operating pattern is maintained until the submodules with the lowest SoC values reach the average SoC of the arm. From that instant onward, all submodules exhibit the same behavior, discharging during the same half-cycle as the 18^{th} submodule.

The last subplot of Fig. 9 shows the active power flowing through the upper and lower arms, as well as the output terminals of the MMC-BESS. Note that the active powers of the upper and lower arms exhibit negative pulses, indicating that the MMC-BESS is injecting active power to the grid, as confirmed by the constant output active power p_a waveform, which remains equal to 5 MW. Nevertheless, the $(p_{u,a})$ and $(p_{\ell,a})$ present small positive intervals, indicating that the upper and lower arms momentarily absorb active power from the grid to equalize the batteries SoC.

B. MMC-BESS Absorbing Active Power

The behavior of the SoC balancing algorithm while the MMC-BESS absorbs active power from the grid is illustrated in Fig. 10. Similarly to the previous case, the SoC values of the SM in the arm were initially distributed between 47% and 52% of the battery capacity. From the beginning of the operation until the completion of the SoC balancing process, the q-axis reference current of the controller is set to -0.5 kA; in other words, the MMC-BESS is controlled to absorb 5 MW from the grid.

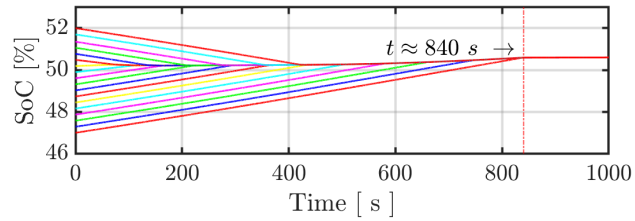
Fig. 10(a) shows the SoC profile of the phase "a" upper arm submodules. Since the converter absorbs active power from the grid, the batteries undergo the balancing process while being charged, reaching the equalized state at approximately $t \approx 840$ s and stabilizing at 50.6% of the rated capacity. The balancing time in this case is shorter than in the previous scenario, since the battery voltage increases with SoC, resulting in greater power exchange during each half-cycle of the arm current.

Note that the SM batteries with SoC values above the arm average are initially discharged until they converge to the arm average SoC. After reaching this level, these SM are charged together with the remaining submodules, maintaining equalization with the arm average SoC until full balancing is achieved. Once equalization is completed, the active power absorbed by the converter decreases to zero, as shown in Fig. 10(b). In practical applications, during periods of low grid demand or surplus generation, the MMC-BESS can be scheduled to operate in charging mode, enabling sustained power absorption from the grid until the batteries reach their maximum allowable SoC.

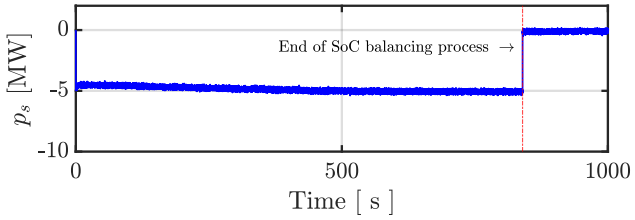
Fig. 10(c) and Fig. 10(d) show the output currents and terminal voltages synthesized by the MMC-BESS, respectively. The output current exhibits an average THD of 1.40% around $t = 200$ s, decreasing as the SoC values converge and reaching 1.33% shortly before the completion of the balancing process. At the same instants, the terminal voltages exhibit average THD values of 2.99% and 2.35%, respectively.

Fig. 11 illustrates a detailed view of the dynamic behavior of the upper arm of phase "a" during the initial stage of the SoC balancing process shown in Fig. 10(a). For clarity, only the waveforms of the submodules exhibiting the highest and lowest SoC values are presented, namely $SoC^u_{a,18}$ and $SoC^u_{a,1}$, respectively.

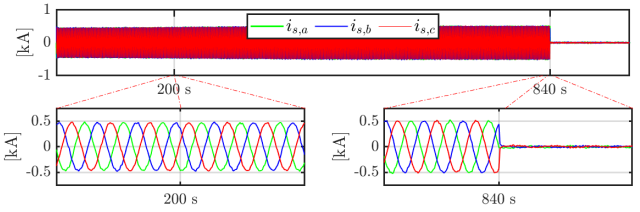
Note that, although the MMC-BESS is absorbing active power from the grid, $SoC^u_{a,18}$ decreases during the negative half-cycle of $i_{u,a}$, indicating that the battery pack of this submodule is being discharged, while $SoC^u_{a,1}$ remains constant. During the positive half-cycle of the arm current, the 1^{st} submodule is charged, whereas the 18^{th} submodule



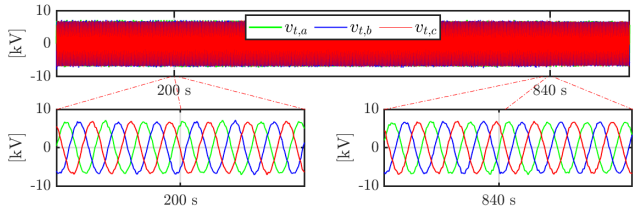
(a) Phase "a" upper arm SoC balancing process



(b) Instantaneous active power



(c) Output currents



(d) Voltages at the AC terminals

FIGURE 10. MMC-BESS behavior during SoC balancing process by charging the batteries.

is bypassed. This operating pattern is maintained until the submodules with the highest SoC values converge to the average SoC of the arm. From that instant onward, all submodules exhibit the same behavior, charging during the same half-cycle as the 1st submodule.

The last subplot of Fig. 11 shows the active power flowing through the upper and lower arms, as well as the output terminals of the MMC-BESS. The active powers of the upper and lower arms exhibit positive pulses, indicating that the MMC-BESS absorbs active power from the grid, as confirmed by the constant output active power waveform p_a, which remains equal to -5 MW. Nevertheless, the waveforms of $(p_{u,a})$ and $(p_{\ell,a})$ present small negative intervals, indicating that the arms momentarily deliver active power to the grid as part of the internal energy redistribution required for the SoC equalization process.

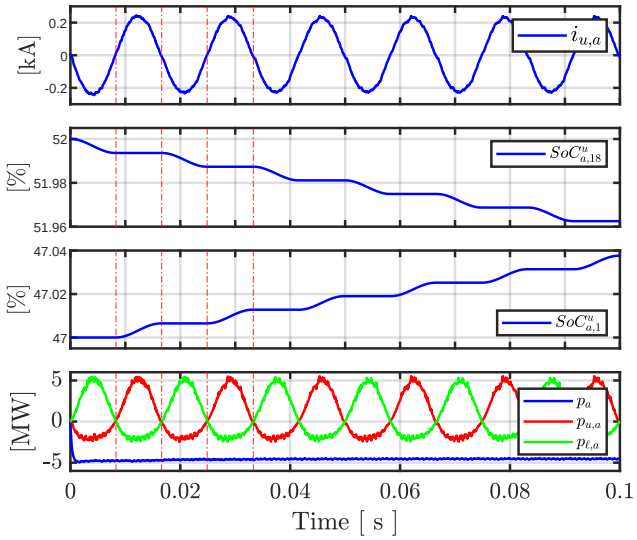


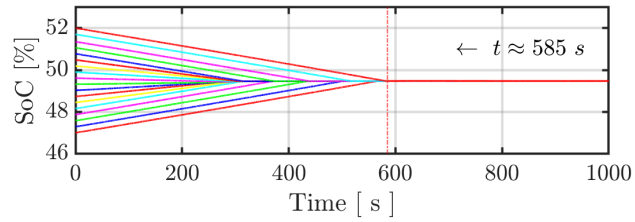
FIGURE 11. Dynamics behavior of phase "a" upper arm in detail during Case B.

C. MMC-BESS Supporting Reactive Power

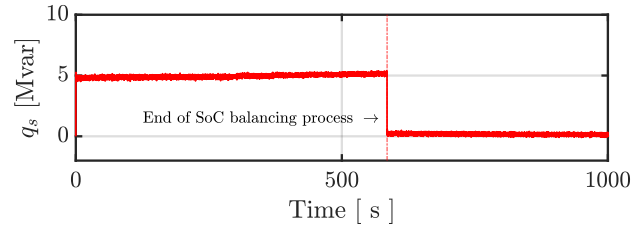
In the final case, the MMC-BESS neither injects nor absorbs active power into the AC grid. Instead, it is controlled to support 5 Mvar of reactive power to the grid by applying a 0.5 kA reference current to the d-axis component of the converter's current controller.

Fig. 12(a) shows the dynamic response of the proposed SoC balancing strategy during the operation of MMC-BESS. The SoC equalization among the SM batteries of each arm is achieved at approximately $t \approx 585$ s. The faster balancing observed in this case results from the absence of active power exchange between the MMC-BESS and the grid, which keeps the arm average SoC nearly constant, neglecting losses, and allows faster convergence of the 18 submodules due to the symmetric initial SoC deviations. Once balancing was completed, the converter reference current $I^*_{s,d}$ is set to zero, as shown in Fig. 12(b). As in the previous cases, in practical applications the MMC-BESS can be scheduled to operate continuously, providing support to the grid. However, this operating condition was not evaluated in this work to reduce computational burden.

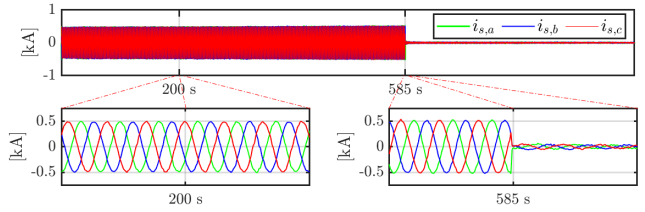
Fig. 12(c) and Fig. 12(d) show the currents and voltages synthesized by the MMC-BESS during the SoC balancing process, respectively. The output currents present an average total harmonic distortion (THD) of 1.31% at $t = 200$ s, which progressively decreases as the SoC values converge, reaching 1.28% toward the end of the balancing interval. The voltages reach an RMS value of 5.90 kV with an average THD of 2.35% at $t = 200$ s. After the balancing process is completed, the converter ceases operation, causing the reactive power to drop to zero and the terminal voltages to return to an RMS value of 5.62 kV with an average THD of 1.91%.



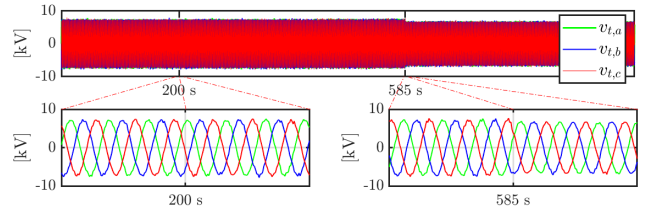
(a) Phase "a" upper arm SoC balancing process



(b) Instantaneous reactive power



(c) Output currents



(d) Voltages at the AC terminals

FIGURE 12. MMC-BESS behavior during SoC balancing process by injecting reactive power to the grid.

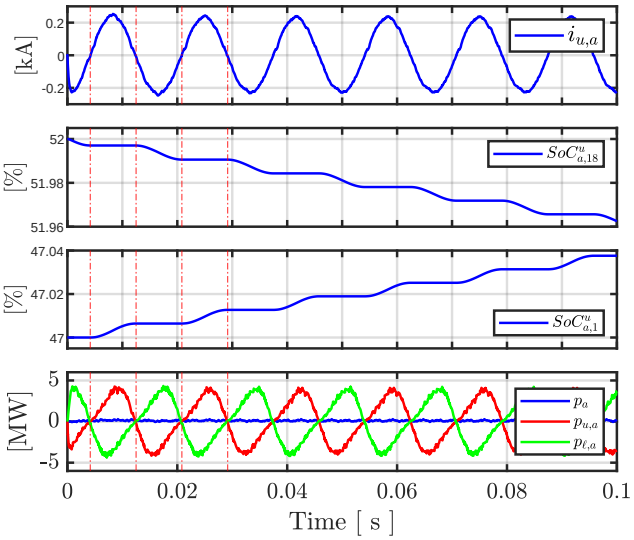


FIGURE 13. Dynamics behavior of phase "a" upper arm in detail during Case C.

Fig. 13 shows a detailed view of the dynamic behavior of the upper arm of phase "a". The upper-arm current $i_{u,a}$ is plotted together with the highest and lowest SoC values, $SoC^u_{a,18}$ and $SoC^u_{a,1}$, respectively. During the balancing process, approximately half of the submodules are discharged while the others are charged until all converge to the arm average SoC. This occurs because, during the negative half-cycle of the upper-arm current, $SoC^u_{a,18}$ decreases, indicating discharge of this SM and energy transfer to submodules with lower SoC, while $SoC^u_{a,1}$ remains unchanged. During the positive half-cycle, the 1st SM is charged, whereas the 18th SM is bypassed. This behavior results from internal circulating currents that enable energy exchange between the upper and lower arms even when the terminal active power of the MMC-BESS is zero. The instantaneous arm active powers shown in Fig. 13 confirm this internal energy exchange, as their sum results in zero terminal active power.

Finally, it is worth noting that the circulating currents were fully compensated by the CCSC loop of Fig. 6 in all three cases. Since their waveforms exhibited identical behavior, they are omitted due to the lack of space.

VI. CONCLUSIONS

This paper presented an online state-of-charge (SoC) balancing strategy for a distributed single-stage Modular Multilevel Converter-based Battery Energy Storage System (MMC-BESS). The proposed method integrates a sorting-based selection algorithm within the smart-battery concept, enabling real-time management of energy distribution among submodules while maintaining low implementation complexity. The control structure combines grid current regulation in the synchronous reference frame with a circulating current suppression controller, ensuring stable converter operation and effective mitigation of internal current oscillations.

Simulation results obtained in PSCAD/EMTDC demonstrated the effectiveness and robustness of the proposed algorithm under different operating conditions, including active power injection or absorption, and reactive power support. In all evaluated scenarios, the method successfully achieved uniform SoC equalization among the 18 submodules per arm while maintaining high-quality AC voltage and current waveforms. The results also confirmed that the balancing process occurs without requiring additional energy-dissipative circuits, preserving system efficiency and improving energy utilization. Furthermore, the circulating current suppression strategy effectively eliminated internal oscillatory currents,

preventing additional losses and improving overall converter performance.

Finally, the proposed strategy advances MMC-based energy storage technologies, improving reliability and flexibility. Future work may extend SoC equalization across converter arms and phases to further enhance the battery energy management.

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AUTHOR'S CONTRIBUTIONS

J.A.P.GARAY: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Writing – Original Draft, Writing – Review & Editing. **P.M.ALMEIDA:** Conceptualization, Formal Analysis, Investigation, Methodology, Project Administration, Supervision, Writing – Original Draft, Writing – Review & Editing. **P.G.BARBOSA:** Formal Analysis, Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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BIOGRAPHIES

Juan Alberto Peralta Garay received the B.S. and M.Sc. degrees in Electrical Engineering from the Federal University of Juiz de Fora (UFJF), Brazil, in 2023 and 2025, respectively. He is currently pursuing the Ph.D. degree in Electrical Engineering at the same institution.

Pedro Machado de Almeida received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Juiz de Fora, Juiz de Fora, Brazil, in 2009, 2011, and 2013, respectively. Since 2014, he has been with the Department of Electrical Engineering at Federal University of Juiz de Fora, where he is currently an Associate Professor. His research interests include control of power electronics, three-phase grid-connected converters, and integration of renewable energy systems.

Pedro Gomes Barbosa received the B.S. degree in electrical engineering from the Federal University of Juiz de Fora, Juiz de Fora, Brazil, in 1986 and the M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Rio de Janeiro, Rio de Janeiro, Brazil, in 1994 and 2000, respectively. From 1987 to 1992, he worked as an Engineer at the Rio de Janeiro Navy Arsenal, Rio de Janeiro, Brazil. Since 1999, he has been with the Department of Electrical Engineering at the Federal University of Juiz de Fora, where he is currently a Full Professor. His research interests include power electronics and its applications in electric power systems.