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Transformerless Six-Leg Single-Phase to Split-Phase Power Converter with Grid Disturbance Mitigation

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ABSTRACT This article proposes a transformerless six-leg single-phase to two-phase AC-DC-AC converter for applications in single-phase three-wire distribution systems, also known as single split-phase systems. Featuring an architecture built upon a pair of three-leg converters, and employs space vector pulse-width modulation to synthesize the output voltages, this modulation scheme reduces harmonic content. Under severe load unbalances, the implemented control scheme successfully preserves fixed amplitude and frequency for the output voltages, while ensuring a predominantly fundamental grid current with low harmonic distortion and a high power factor, including when supplying nonlinear loads. In addition, the proposed topology can mitigate grid disturbances, such as voltage sags and swells, maintaining the load voltages with constant amplitude and frequency and preserving a high grid-side power factor under voltage disturbances, as well as nonlinear and unbalanced loads conditions. When contrasted with the conventional four-leg AC-DC-AC converter, the proposed converter mitigates grid current harmonic distortion while reducing semiconductor losses. The validity of the entire system are thoroughly confirmed through simulation and experimental evaluations.

KEYWORDS AC-DC-AC Converter, grid disturbance mitigation, space vector modulation, six-leg, split-phase system, single-phase three-wire converter, transformerless.

I. INTRODUCTION

The single-phase three-wire electrical power system, frequently referred to as a split-phase system, sees extensive utilization across residential and small commercial sectors in nations like the United States and Japan. In this arrangement, two distinct phase voltages operate with a 180° displacement, producing a combined line-to-line voltage that doubles the magnitude of the individual phase voltages [1]. Typically, these split-phase architectures rely on the secondary side of a center-tapped transformer to establish the three-wire connection. However, this traditional setup faces challenges during unbalanced load operations, leading to asymmetrical output voltages and a degradation of the source power factor. Furthermore, the presence of nonlinear loads tends to introduce severe harmonic distortions into the grid current [2].

To improve power quality, several converter-based solutions have been proposed. Unified power quality conditioner topologies have been reviewed in [3], while a transformerless online UPS (uninterruptible power supply) was presented in [4]. Comprehensive reviews of multilevel converters, covering their operating principles, topologies, modulation strategies, and applications, were presented in [5], [6]. A multifunctional control strategy for an asymmetrical cascaded H-bridge inverter operating in microgrids was proposed in [7].

Several single-phase three-wire converter topologies have also been reported for battery energy storage systems and inverter applications [8], [9], photovoltaic systems [10], transformerless UPSs [11], and fuel-cell generation systems for microgrids [12]. More recently, in [13] two-level and three-level single-phase three-wire converters were presented, and their semiconductor losses and harmonic distortion were evaluated, while in [14] a reactive power control strategy for electric vehicle smart chargers on single-phase three-wire distribution feeders was proposed. These studies seek to provide regulated load voltages while maintaining low-distortion grid currents and unity power factor. Throughout this paper, the term *sinusoidal* denotes a waveform that is predominantly fundamental with low harmonic distortion.

Recent studies have also contributed to the advancement of transformerless converter topologies and advanced control strategies. For instance, a transformerless common-ground single-phase inverter for battery energy storage sys-

tem (BESS) applications was proposed in [15], whereas a feedback linearization control strategy was proposed for transformerless common-ground voltage source inverters in [16]. More recently, predictive control has been applied to single-phase AC-DC-AC converters with parallel rectifiers to regulate the grid current, minimize circulating currents, and reduce harmonic distortion [17]. These contributions further demonstrate the continued interest in developing high-performance power converters with improved efficiency, power quality, and control capabilities, motivating the investigation of alternative converter topologies such as the one proposed in this article.

As a baseline for comparison, the conventional four-leg (4L) AC-DC-AC topology introduced in [18] (illustrated in Fig. 1(a)) is adopted. Proper operation of this conventional converter demands a DC-link voltage level equivalent to twice the load voltage amplitude, which consequently results in high voltage stress across the power switches. Additionally, the resulting output voltages present a low modulation index.

To address these drawbacks, a novel transformerless six-leg topology for single-phase two-phase AC-DC-AC converter applications is put forward in [19]. Building upon that foundation, this extended article provides the load terminals with an alternating voltage of constant amplitude, fixed frequency, and a precise 180-degree phase displacement. In addition, it maintains a clean supply-side performance characterized by a sinusoidal input current and a unity power factor, even under grid disturbance conditions and nonlinear load profiles. The analytical modeling, the pulse-width modulation approach, and the control strategy are comprehensively detailed, with validation provided by simulation and experimental results. Moreover, Section V provides a comparative assessment against the conventional four-leg counterpart, focusing specifically on semiconductor power losses and current harmonic attenuation.

This work represents an extended and improved version of [19]. The main contributions include: 1) Additional pulse-width modulation equations have been included to provide a more detailed description of the modulation scheme, along with corrections to the existing equations; 2) New simulation results under voltage sag, alongside simulation and experimental results under 30–32% voltage swell, validating robustness under grid disturbances; and 3) Expanded experimental tests under grid, load transients, and nonlinear loads, reinforcing the converter's performance and applicability.

II. PROPOSED CONVERTER MODEL

The topology introduced in this work is structured by connecting two standard 3L (three-leg converters) in series, as illustrated in Fig. 1(b). The system provides two output phase voltages v_{l_1} and v_{l_2}, which are phase-shifted by $180°$. Consequently, the resulting line-to-line voltage, defined as $v_{l_{12}} = v_{l_1} + v_{l_2}$, exhibits an amplitude exactly twice that of a single phase. Let q_{s_k} denote the switching state of the upper semiconductor device in leg s_k, where $s \in \{1, 2, 3\}$ and $k \in \{a, b\}$. Under these conditions, the pole voltages are given by:

$$v_{s_k 0_k} = (2q_{s_k} - 1)\frac{v_{C_k}}{2}, \tag{1}$$

where $v_{s_k 0_k}$ denotes the voltage between the pole terminal of leg s_k and the point 0_k. Here, 0_k denotes the DC-link midpoint, i.e., the node between the two series-connected DC-link capacitors of converter k. For example, v_{1a0a} denotes the voltage between node $1a$ and the midpoint $0a$ of converter A, whereas v_{3b0b} denotes the voltage between node $3b$ and the midpoint $0b$ of converter B. Moreover, v_{C_k} denotes the total DC-link voltage of converter k. Expressed in terms of these pole voltages, the converter input voltage v_g and the output phase voltages v_{l_1} and v_{l_2} are given by:

$$v_g = v_{1_a 0_a} - v_{1_b 0_b} - v_{2_a 0_a} + v_{2_b 0_b} \tag{2}$$

$$v_{l_1} = v_{3_a 0_a} - v_{2_a 0_a} \tag{3}$$

$$v_{l_2} = v_{3_b 0_b} - v_{2_b 0_b}. \tag{4}$$

Furthermore, the grid voltage e_g is expressed as:

$$e_g = L_g \frac{di_g}{dt} + v_g. \tag{5}$$

Considering the internal resistance of the inductor (R_g), the following equation is obtained:

$$e_g - v_g = R_g i_g + L_g \frac{di_g}{dt}. \tag{6}$$

The values of v_g, v_{l1} and v_{l2} are limited so they obey the following conditions:

$$|v_g| \leq v_{Ca} + v_{Cb} \tag{7}$$

$$|v_{l1}| \leq v_{Ca} \tag{8}$$

$$|v_{l2}| \leq v_{Cb}. \tag{9}$$

The operating constraints during under- and over-voltage conditions are defined by (7)–(9). Unlike the conventional topology, which limits the converter input voltage to a single DC link ($|v_g| \leq v_C$), the proposed converter operates with the input voltage supported by the sum of both DC-link voltages ($|v_g| \leq v_{C_a} + v_{C_b}$). This structural feature provides a wider modulation margin to handle severe grid anomalies, such as voltage sags and swells, without affecting the voltage synthesis at the loads.

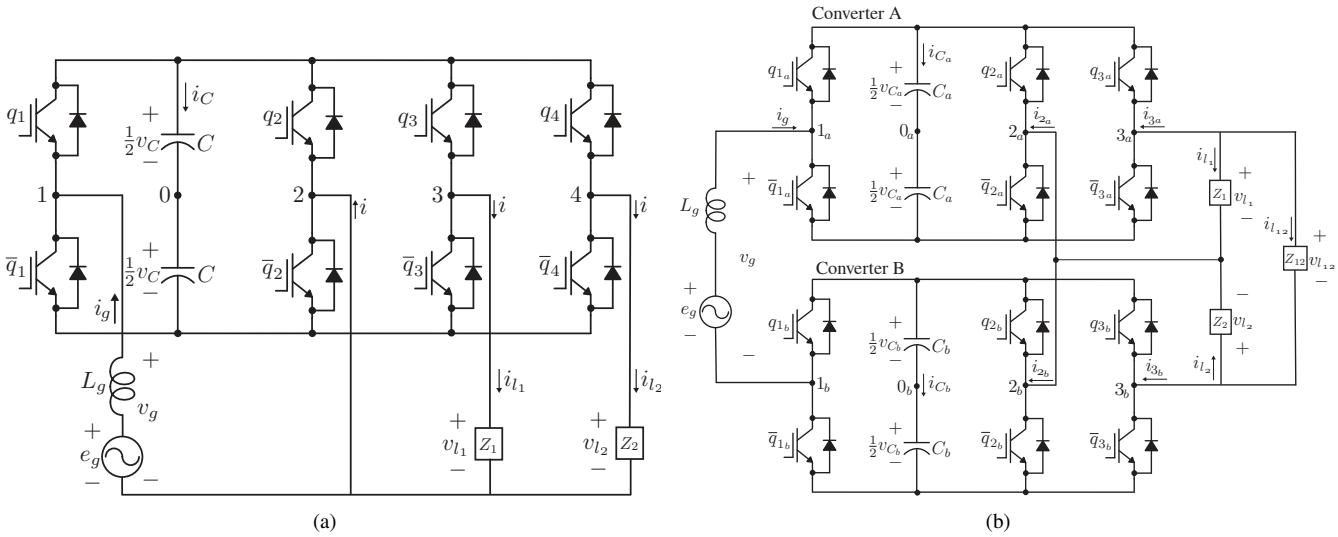


FIGURE 1. Single-phase to single-phase three-wire converters: (a) conventional four-leg (4L), and (b) proposed six-leg (6L) [19].

III. PULSE-WIDTH MODULATION (PWM)

Throughout this analysis, a superscript asterisk $(*)$ designates reference variables. Rewriting (2) in terms of the reference voltages yields:

$$v_g^* = v_{1_a0_a}^* - v_{1_b0_b}^* - v_{2_a0_a}^* + v_{2_b0_b}^* \tag{10}$$

Rearranging the terms, the input voltage reference of the converter can be expressed as two components, v_{g1}^* and v_{g2}^*, as follows:

$$v_g^* = \underbrace{(v_{1_a0_a}^* - v_{2_a0_a}^*)}_{v_{g1}^*} - \underbrace{(v_{1_b0_b}^* - v_{2_b0_b}^*)}_{v_{g2}^*} = v_{g1}^* - v_{g2}^* \tag{11}$$

For the first load (z_1), the voltage reference v_{l1}^* can be rewrittenby introducing the voltage between legs $3a$ and $1a$, denoted as v_{3a1a}^*. Knowing that $v_{3a1a}^* = v_{3a0a}^* - v_{1a0a}^*$, the equation is expanded by adding and subtracting the term v_{1a0a}^*:

$$v_{l1}^* = v_{3a0a}^* - v_{2a0a}^* = (v_{1a0a}^* - v_{2a0a}^*) + (v_{3a0a}^* - v_{1a0a}^*) \tag{12}$$

$$v_{l1}^* = v_{g1}^* + v_{3a1a}^* \tag{13}$$

Analogously, for the second load (z_2) voltage reference v_{l2}^* can be expressed as a function of the leg-to-leg voltage v_{3b1b}^*. By noting that $v_{3b1b}^* = v_{3b0b}^* - v_{1b0b}^*$ and applying the same mathematical procedure of adding and subtracting the term v_{1b0b}^*, one obtains:

$$v_{l2}^* = v_{3b0b}^* - v_{2b0b}^* = (v_{1b0b}^* - v_{2b0b}^*) + (v_{3b0b}^* - v_{1b0b}^*) \tag{14}$$

$$v_{l2}^* = v_{g2}^* + v_{3b1b}^* \tag{15}$$

Considering an auxiliary variable v_x^*, the components v_{g1}^* and v_{g2}^* are formulated as:

$$v_{g1}^* = \frac{v_g^*}{2} + v_x^*, \tag{16}$$

$$v_{g2}^* = -\frac{v_g^*}{2} + v_x^*. \tag{17}$$

subtracting (17) from (16) yields:

$$v_{g1}^* - v_{g2}^* = \left(\frac{v_g^*}{2} + v_x^*\right) - \left(-\frac{v_g^*}{2} + v_x^*\right) = v_g^*, \tag{18}$$

which confirms that the auxiliary variable v_x^* does not affect the resulting input voltage reference. Therefore, v_x^* can be expressed as:

$$v_x^* = \frac{v_{g1}^* + v_{g2}^*}{2}. \tag{19}$$

Rewriting the voltage relationships in terms of the reference variables v_{g1}^*, v_{g2}^*, v_{l1}^*, v_{l2}^*, and v_x^*, the following system is obtained:

$$\begin{cases} v_g^* = v_{g1}^* - v_{g2}^* \\ v_{l1}^* = v_{g1}^* + v_{3_a1_a}^* \\ v_{l2}^* = v_{g2}^* + v_{3_b1_b}^* \\ v_x^* = 0.5v_{g1}^* + 0.5v_{g2}^*. \end{cases} \tag{20}$$

Solving (20), one can determine v_{g1}^*, v_{g2}^*, $v_{3_a1_a}^*$, and $v_{3_b1_b}^*$:

$$v_{g1}^* = \frac{v_g^*}{2} + v_x^*, \tag{21}$$

$$v_{g2}^* = -\frac{v_g^*}{2} + v_x^*, \tag{22}$$

$$v_{3_a1_a}^* = -\frac{v_g^*}{2} + v_{l1}^* - v_x^*, \tag{23}$$

$$v_{3_b1_b}^* = \frac{v_g^*}{2} + v_{l2}^* - v_x^*. \tag{24}$$

The DC-link reference voltages are assumed to be equal, i.e., $v^*_{Ca} = v^*_{Cb} = v^*_C$. The four voltage references (v^*_{g1}, v^*_{g2}, v^*_{3a1a}, and v^*_{3b1b}) must comply with the DC-link linear constraint. Since these are leg-to-leg voltages, the limit is $\pm v^*_C$. Imposing $-v^*_C \leq v^* \leq v^*_C$ for each of them yields:

Constraint for v^*_{g1}:

$$\begin{aligned} -v^*_C &\leq \frac{v^*_g}{2} + v^*_x \leq v^*_C \\ -v^*_C - \frac{v^*_g}{2} &\leq v^*_x \leq v^*_C - \frac{v^*_g}{2} \end{aligned} \tag{25}$$

Constraint for v^*_{g2}:

$$\begin{aligned} -v^*_C &\leq -\frac{v^*_g}{2} + v^*_x \leq v^*_C \\ -v^*_C + \frac{v^*_g}{2} &\leq v^*_x \leq v^*_C + \frac{v^*_g}{2} \end{aligned} \tag{26}$$

Constraint for v^*_{3a1a}:

$$\begin{aligned} -v^*_C &\leq \left(-\frac{v^*_g}{2} + v^*_{l1}\right) - v^*_x \leq v^*_C \\ -v^*_C - \left(-\frac{v^*_g}{2} + v^*_{l1}\right) &\leq -v^*_x \leq v^*_C - \left(-\frac{v^*_g}{2} + v^*_{l1}\right) \\ -v^*_C + \left(-\frac{v^*_g}{2} + v^*_{l1}\right) &\leq v^*_x \leq v^*_C + \left(-\frac{v^*_g}{2} + v^*_{l1}\right) \end{aligned} \tag{27}$$

Constraint for v^*_{3b1b}:

$$\begin{aligned} -v^*_C &\leq \left(\frac{v^*_g}{2} + v^*_{l2}\right) - v^*_x \leq v^*_C \\ -v^*_C - \left(\frac{v^*_g}{2} + v^*_{l2}\right) &\leq -v^*_x \leq v^*_C - \left(\frac{v^*_g}{2} + v^*_{l2}\right) \\ -v^*_C + \left(\frac{v^*_g}{2} + v^*_{l2}\right) &\leq v^*_x \leq v^*_C + \left(\frac{v^*_g}{2} + v^*_{l2}\right) \end{aligned} \tag{28}$$

From the four described above, the auxiliary variable v^*_x must satisfy all conditions simultaneously. Therefore, the lower and upper bounds for v^*_x are given by the maximum of the lower limits and the minimum of the upper limits, respectively:

$$\begin{aligned} v^*_{x,min} &= \max\Big(-v^*_C - \frac{v^*_g}{2},\ -v^*_C + \frac{v^*_g}{2}, \\ &\qquad -v^*_C - \frac{v^*_g}{2} + v^*_{l1},\ -v^*_C + \frac{v^*_g}{2} + v^*_{l2}\Big) \\ &= -v^*_C + \max\Big(-\frac{v^*_g}{2},\ \frac{v^*_g}{2}, \\ &\qquad -\frac{v^*_g}{2} + v^*_{l1},\ \frac{v^*_g}{2} + v^*_{l2}\Big) \end{aligned} \tag{29}$$

$$\begin{aligned} v^*_{x,max} &= \min\Big(v^*_C - \frac{v^*_g}{2},\ v^*_C + \frac{v^*_g}{2}, \\ &\qquad v^*_C - \frac{v^*_g}{2} + v^*_{l1},\ v^*_C + \frac{v^*_g}{2} + v^*_{l2}\Big) \\ &= v^*_C + \min\Big(-\frac{v^*_g}{2},\ \frac{v^*_g}{2}, \\ &\qquad -\frac{v^*_g}{2} + v^*_{l1},\ \frac{v^*_g}{2} + v^*_{l2}\Big) \end{aligned} \tag{30}$$

To synthesize v^*_x within these established limits, a proportional factor μ^* such that $0 \leq \mu^* \leq 1$ is introduced. Thus, v^*_x for each of them yields:is defined as:

$$v^*_x = \mu^* v_{x,max} + (1 - \mu^*) v_{x,min}. \tag{31}$$

The space vector pulse-width modulation (SVPWM) scheme is implemented according to the methodology described in [19]. In this approach, the modulation solution is derived simultaneously across all three converter legs prior to executing the phase-wise PWM synthesis.

Once the voltage references v^*_{g1}, v^*_{g2}, v^*_{l1}, and v^*_{l2} are determined from (20), they can be mapped onto the complex planes v^*_{gj} X v^*_{lj} for $j \in \{1, 2\}$, as illustrated in Fig. 2. Eight distinct switching state combinations, denoted by q_{sk}, are possible, yielding stationary voltage vectors $\mathbf{v}_j = v_{gj} + iv_{lj}$ that partition the plane into six triangular sectors (1 through 6).

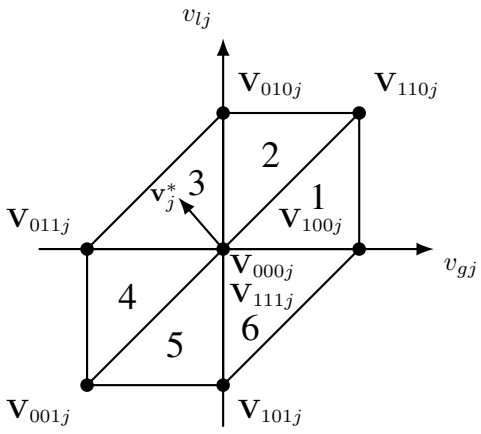


FIGURE 2. Voltage vectors and sectors.

The reference voltage vector to be synthesized by the converter is defined as $\mathbf{v}^*_j = v^*_{gj} + iv^*_{lj}$. To minimize harmonic distortion, this vector is approximated using a linear combination of the three nearest adjacent vectors. Assuming $\mathbf{v}^*_j$ remains constant over the sampling period T, and denoting these adjacent vectors as $\mathbf{v}_{wj}$, $\mathbf{v}_{nj}$, and $\mathbf{v}_{mj}$, the following relationship is obtained:

$$\mathbf{v}^*_j = \frac{t_{wj}}{T}\mathbf{v}_{wj} + \frac{t_{nj}}{T}\mathbf{v}_{nj} + \frac{t_{mj}}{T}\mathbf{v}_{mj}, \tag{32}$$

where t_{wj}, t_{nj}, and t_{mj} denote the application times corresponding to each voltage vector.

Decomposing the complex vector in (32) into its orthogonal real (v^*_{gj}) and imaginary (v^*_{lj}) components yields the following scalar expressions:

$$v^*_{gj} = \frac{t_{wj}}{T}v_{gwj} + \frac{t_{nj}}{T}v_{gnj} + \frac{t_{mj}}{T}v_{gmj}, \tag{33}$$

$$v^*_{lj} = \frac{t_{wj}}{T}v_{lwj} + \frac{t_{nj}}{T}v_{lnj} + \frac{t_{mj}}{T}v_{lmj}. \tag{34}$$

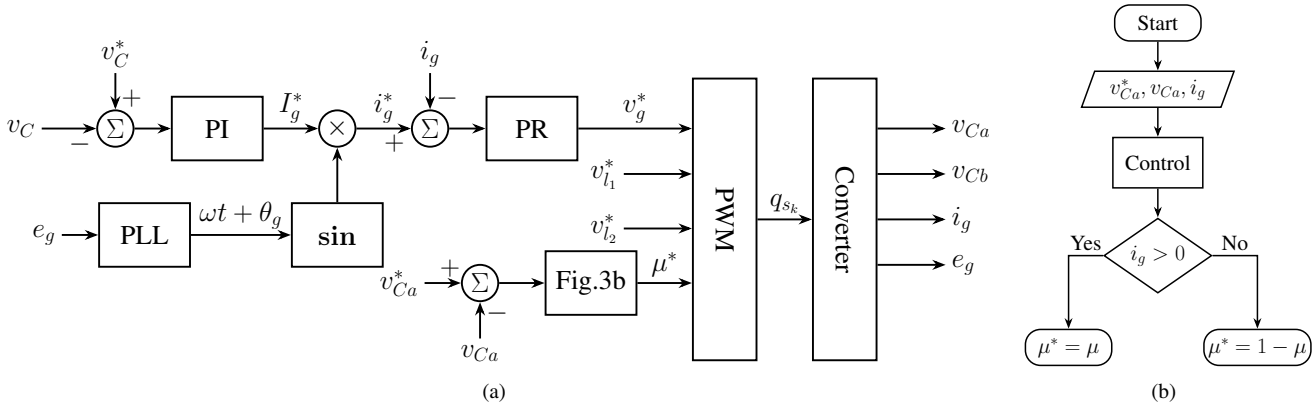


FIGURE 3. Control Strategy: (a) overall control strategy, and (b) Flowchart of DC-link voltage control.

IV. CONTROL STRATEGY

A. Overall Control Strategy

The overall configuration and control architecture are depicted in the block diagram of Fig. 3(a). The control structure adopted in this work is the same as that presented in [19]. The average DC-link voltage $[v_C = (v_{C_a} + v_{C_b})/2]$ is regulated to the reference value v_C^* by a proportional-integral (PI) controller. This controller output is the amplitude of the reference grid current (I_g^*), which is multiplied by a normalized value, resulting in the reference grid current i_g^*. A phase-locked loop (PLL) is used to determine the phase angle of e_g, such that i_g^* has the same phase angle e_g (θ_g). The block R_{i_g} represents a resonant controller, which provides zero steady-state error in the operating frequency. This controller is used to control the grid current and produces v_g^* as output.

The controller parameters were selected to ensure stable operation of the cascaded control structure. First, the outer PI controller regulates the average DC-link voltage. Next, the auxiliary PI balancing controller (Control) and the inner PR current controller are regulated. Finally, all control gains were fine-tuned through simulations considering load step transients, nonlinear load conditions, and grid voltage disturbances. The adopted parameters are summarized in Table 1.

The DC-link voltage balancing strategy, illustrated in the flowchart of Fig. 3(b), relies on a proportional-integral (Control) controller that generates a modulation factor μ based on the DC-link voltage error. The corrective balancing action is governed by the polarity of the grid current i_g. Specifically, if the current is positive ($i_g > 0$), the resulting factor is set as $\mu^* = \mu$; conversely, for a negative ($i_g < 0$), the factor is defined as $\mu^* = 1 - \mu$.

TABLE 1. Controller Parameters

Controller	Type	Parameters
PLL	PI	$K_p = 0.25$, $K_i = 2.5$
Average DC-link voltage (PI)	PI	$K_p = 0.3$, $K_i = 25$
DC-link voltage balancing (μ)	PI	$K_p = 0.3$, $K_i = 25$
Grid current (PR)	PR	$K_p = 3$, $K_r = 1000$

B. DC-Link Capacitor Design

Following the procedure presented in [20], the DC-link capacitor is designed based on the second-harmonic power oscillation inherent to single-phase converters. Since the proposed converter operates at unity power factor, the instantaneous grid power consists of a dc component and a second-harmonic component. Moreover, as the converter is composed of two identical single-phase converter cells, each cell processes half of the total active power, yielding

$$P_A = P_B = \frac{P_o}{2} = \frac{E_g I_g}{2}, \tag{35}$$

where E_g and I_g are the rms values of the grid voltage and current, respectively.

Thus, the instantaneous power processed by converter A is

$$p_A(t) = P_A\left(1 - \cos(2\omega t)\right), \tag{36}$$

where the average term is transferred to the load, while the oscillating component is absorbed by the DC-link capacitor,

$$P_A \cos(2\omega t) = \frac{C_a}{2}\frac{dv_{Ca}^2}{dt}. \tag{37}$$

Considering

$$v_{Ca}(t) = v_{Ca}^* + \tilde{v}_{Ca}(t), \tag{38}$$

and assuming $v_{Ca}^* \gg |\tilde{v}_{Ca}|$, (37) can be approximated by

$$P_A \cos(2\omega t) \simeq C_a v_{Ca}^* \frac{d\tilde{v}_{Ca}}{dt}, \tag{39}$$

whose integration gives

$$\tilde{v}_{Ca}(t) = \frac{P_A}{2\omega C_a v_{Ca}^*}\sin(2\omega t). \tag{40}$$

Defining the peak-to-peak DC-link voltage ripple as

$$\Delta v_{Ca} = 2|\tilde{v}_{Ca}|_{\max}, \tag{41}$$

the minimum required capacitance is obtained as

$$C_a \geq \frac{P_A}{\omega v_{Ca}^* \Delta v_{Ca}} = \frac{E_g I_g}{2\omega v_{Ca}^* \Delta v_{Ca}}. \tag{42}$$

Since both converter cells are identical,

$$C_a = C_b. \tag{43}$$

It should be noted that the proposed sizing procedure assumes ideal power sharing between the converter cells. In practice, the balancing controller adjusts the modulation factor μ according to the DC-link voltage error, redistributing the instantaneous power between the converter cells. Therefore, C_a and C_b may present different voltage ripple amplitudes, although the proposed first-order capacitor sizing method remains valid.

V. COMPARISON OF CONFIGURATIONS

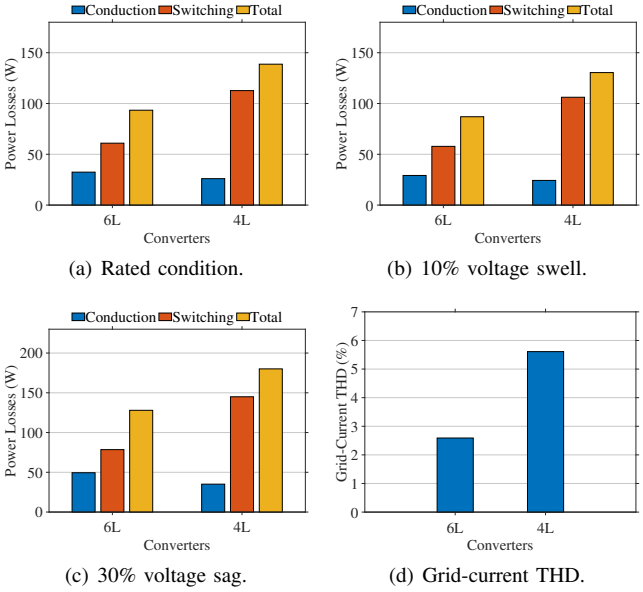
The 4L and 6L converters were simulated in PSIM, and the resulting data were subsequently processed in MATLAB under equal and balanced load conditions. The operational parameters applied in the comparative analysis for both the proposed and conventional topologies are detailed in Table 2. The load Z_{12} was not considered in this analysis. Semiconductor power losses were evaluated considering the Mitsubishi Electric CM1000HA-24H IGBT module.

TABLE 2. Parameters Considered for Comparative Analysis

Parameters	Description	Values
E_g	Grid voltage	155 V
v_{l1}^*, v_{l2}^*	Load voltage	155 V
f_s	Switching carrier frequency	10 kHz
v_{Ca}, v_{Cb}	DC-link reference voltage (Proposed)	164 V
v_C	DC-link reference voltage (Conventional)	328 V
L_g	Grid inductance	7 mH
R_{lj}	Load resistance	24 Ω
L_{lj}	Load inductance	7 mH
C_a, C_b	DC-link capacitance (Proposed)	2.2 mF
C	DC-link capacitance (Conventional)	2.2 mF

Figs. 4(a), 4(b) and 4(c) compare the semiconductor power losses of the proposed 6L converter and the conventional 4L topology under rated and 10% voltage swell, and 30% voltage sag conditions, respectively. The results include conduction (P_{cd}), switching (P_{sw}), and total losses (P_{to}). Although the proposed converter employs a larger number of power switches, each device is subjected to a lower blocking voltage, which significantly reduces the switching losses. Consequently, the reduction in switching losses compensates for the slightly higher conduction losses, resulting in lower total semiconductor losses.

Under rated operation, the total semiconductor losses decrease from 138.71 W to 93.39 W, corresponding to a reduction of approximately 32.7%. Similarly, under a 10% voltage swell, the total losses decrease from 130.43 W to 86.97 W, representing a reduction of approximately 33.3%. Under a 30% voltage sag, the total losses decrease from



(a) Rated condition. (b) 10% voltage swell.

(c) 30% voltage sag. (d) Grid-current THD.

FIGURE 4. Comparison of semiconductor power losses under rated, 10% voltage swell, and 30% voltage sag conditions, and grid-current THD for the 6L and 4L converters.

180.09 W to 127.97 W, corresponding to a reduction of approximately 28.9%. Therefore, the proposed converter consistently achieves lower total semiconductor losses than the conventional topology, mainly due to the significant reduction in switching losses.

The total semiconductor losses are calculated as:

$$P_{to} = \sum_{f=1}^{N} \left(P_{cd,f} + P_{sw,f} \right), \tag{44}$$

where N is the total number of semiconductor switches, while $P_{cd,f}$ and $P_{sw,f}$ denote the conduction and switching losses of the f-th switch, respectively.

Fig. 4(d) compares the total harmonic distortion (THD) of the grid current for the proposed 6L converter and the conventional 4L topology under rated operating conditions. The proposed converter achieves a grid-current THD of 2.59%, whereas the conventional topology presents a THD of 5.61%, corresponding to a reduction of approximately 53.8%.

The THD is defined as the ratio of the root mean square (RMS) value of all harmonic components to the RMS value of the fundamental component, and is given by

$$\mathrm{THD}(\%) = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \times 100, \tag{45}$$

where I_1 is the RMS value of the fundamental component and I_h is the RMS value of the harmonic component of order h.

VI. SIMULATION RESULTS

To evaluate the performance of the proposed converter, simulations were executed in PSIM and post-processed using MATLAB. The key system parameters applied during this analysis are summarized in Table 3.

TABLE 3. Parameters Considered for Simulation and Experimental Results

Parameters	Description	Values
e_g	Grid voltage	155 V
v_{l1}^*, v_{l2}^*	Load line voltage	155 V
f_s	Switching frequency	10 kHz
f_g, f_l	Grid and load frequency	60 Hz
v_{Ck}	DC-link voltage	164 V
L_g	Grid inductance	7 mH
R_l	Load resistance	94 Ω
L_l	Load inductance	7 mH
$\cos(\phi)$	Load power factor	0.99
C	DC-link capacitance	2200 μF

The loads Z_1, Z_2, Z_{12} are defined by the load parameters R_l and L_l, where $Z_1 = Z_2 = Z_{12}$.

Fig. 5 depicts the steady-state performance, where the grid current (i_g) remains in phase with the grid voltage (e_g), ensuring high power factor operation. In addition, the DC-link voltages stay well-regulated at their respective references. The balanced load profile is confirmed by i_{l1} and i_{l2} displaying identical magnitudes and frequencies, 180 degrees out of phase.

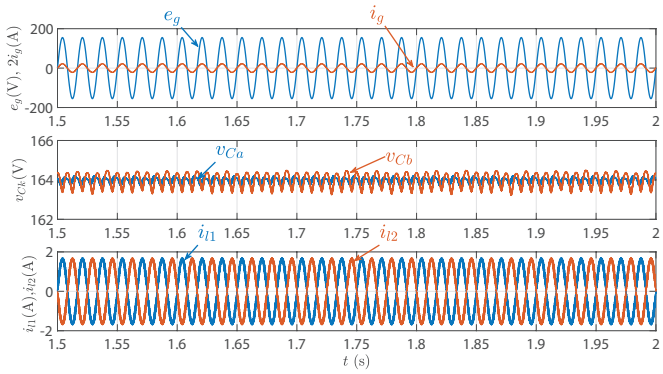


FIGURE 5. System behavior in steady state under a balanced load condition: grid parameters (e_g, i_g), DC-link voltages (v_{Ck}), and load currents (i_{l1}, i_{l2}).

In Fig. 6, the same variables with the same parameters as in Fig. 5 are shown, but now the current i_{12} is presented. Note that this current is approximately twice the currents i_{l1} and i_{l2}, which occurs because the voltage v_{l12} is the sum of v_{l1} and v_{l2}.

An unbalanced operation scenario is evaluated in Fig. 7, caused by attaching a nonlinear load Z_2 and leaving Z_{l12} disconnected. Consequently, current harmonic levels reach roughly 37% THD in i_{l2} and 9.7% THD in i_{l1}. Nevertheless, the controller maintains reliable performance, keeping e_g and

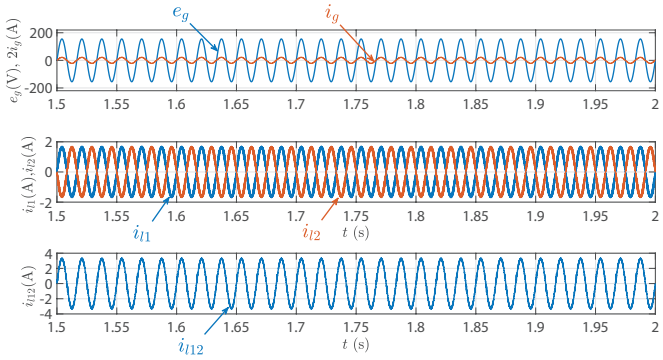


FIGURE 6. Steady-state performance under balanced load conditions: waveform dynamics for grid voltage (e_g), grid current (i_g), DC-link voltages (v_{Ck}), and load currents (i_{l1}, i_{l2}, i_{l12}).

i_g synchronized and preserving DC-link voltage regulation at the desired setpoints (their reference values).

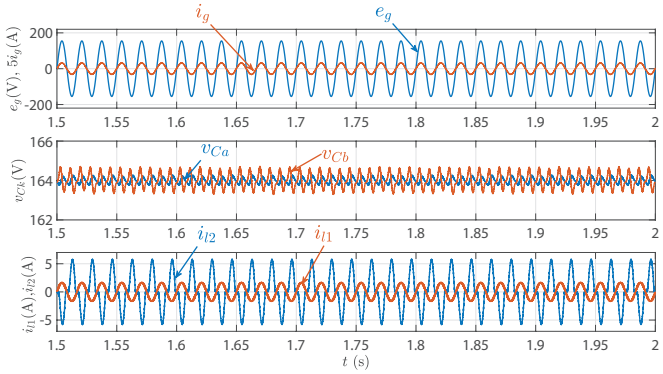


FIGURE 7. Steady-state behavior under nonlinear load: grid voltage (e_g), grid current (i_g), DC-link voltages (v_{Ck}), and load currents (i_{lj}).

A voltage swell of 30% is applied at $t = 1.7$ s, as illustrated in Fig. 8. It can be observed that the control strategy was robust enough to keep the load voltage unchanged, as the currents maintained the same amplitude and frequency values, and the DC-link control responded quickly to regulate the grid voltage variation, within approximately 0.1 s. These results confirm that the proposed topology is reliable.

The PWM-generated switched voltage waveforms and their corresponding average values ($\bar{v}$) are depicted in Fig. 9. Both v_{l1} and v_{l2} exhibit three-level switched profiles with identical magnitudes and a phase displacement of 180 degrees. Due to the combined addition of v_{l1} and v_{l2}, the resulting v_{l12} waveform features five levels.

In Fig. 10, a voltage sag of 30% is applied at ($t = 1.7$ s). It can be observed that the DC-link controller is once again robust enough to maintain the load voltages at the same levels as before the sag event. The DC-link voltages remain regulated at their reference values, and the controller requires approximately (0.15 s) to restore steady-state operation.

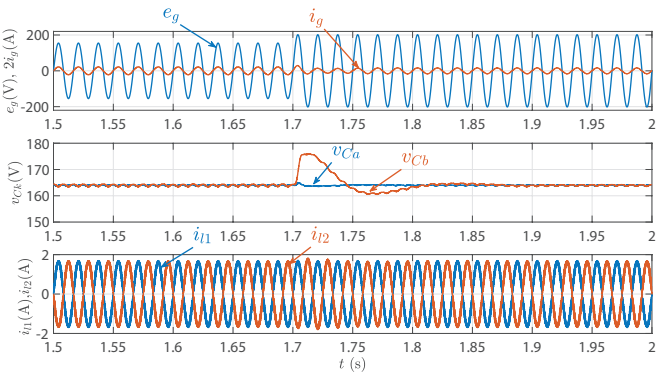


FIGURE 8. Waveforms of grid voltage (e_g), grid current (i_g), DC-link voltages (v_{Ck}), and load currents (i_{l1}, i_{l2}) under a swell condition with a balanced load configuration.

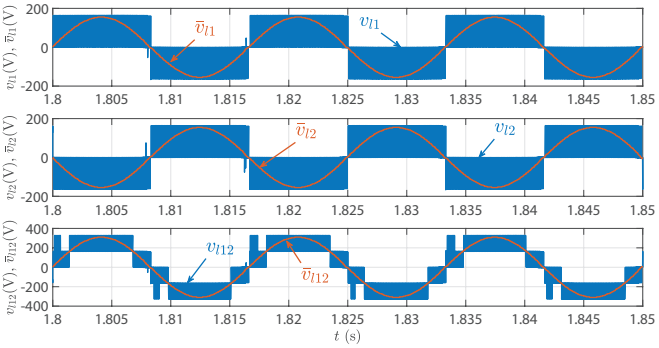


FIGURE 9. Simulation in steady state: generated load voltages and their mean values for the proposed converter topology.

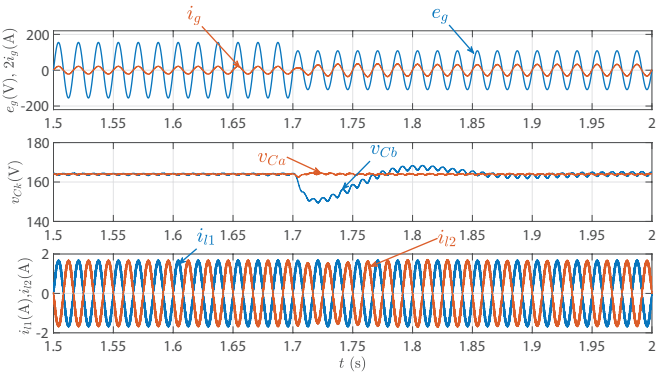


FIGURE 10. Waveforms of grid voltage (e_g), grid current (i_g), DC-link voltages (v_{Ck}), and load currents (i_{l1}, i_{l2}) under a sag disturbance with a balanced load configuration.

VII. EXPERIMENTAL RESULTS

The 6L topology was constructed to validate the system's practical feasibility, with operating parameters summarized in Table 3. The power stage incorporates SEMIKRON SKM50GB12T4 IGBT modules and SKHI23 drivers. A TMDSDOCK28379D digital signal processor executes both the control algorithms and the Pulse-width modulation scheme. Waveform acquisition was performed using an Agilent Technologies InfiniVision DSO-X3014A digital oscilloscope. The converter evaluation encompasses three distinct operational conditions:

The experimental prototype employs IGBT power modules, and the switching frequency was set to 10 kHz, which is within the range commonly used in medium-power IGBT-based converters. Although 10 kHz lies within the audible range, this value was selected as a compromise between harmonic performance and IGBT switching losses. Increasing the switching frequency above the audible range would increase switching losses and thermal stress, whereas a lower frequency would increase switching ripple and filtering requirements.

1) Balanced loads ($R_l = 94\ \Omega$ and $L_l = 7$ mH);
2) Swell conditions with balanced loads ($R_l = 94\ \Omega$ and $L_l = 7$ mH);
3) Unbalanced loads ($R_{l1} = 94\ \Omega$, $L_{l1} = 7$ mH, Z_2 being a nonlinear load and Z_{12} is an open load;
4) A step-load change applied to Z_1 under the operational state of Scenario 3, halving R_{l1} from 94 Ω to 47 Ω.

subjected to a step-load change in Z_1, reducing R_{l1} from 94 Ω to 47 Ω.

Figs. 11(a), 11(b), and 11(c). depict the steady-state experimental response. Grid unity power factor operation is confirmed by the synchronization between i_g and e_g. Furthermore, a 180° phase shift is verified across the load quantities (i_{l1}, i_{l2}, v_{l1}, and v_{l2}), where v_{l12} equals the summation of v_{l1} and v_{l2}, and i_{l12} denotes the line-to-line load current.

The experimental results for scenario 2 are illustrated in Figs. 13(a) and 13(b). To keep the system power constant, the grid-side current (i_g) decreases when the swell of approximately 32% occurs. This ensures that the load voltage remains unchanged in both amplitude and frequency, even under this grid fluctuation, experimentally demonstrating the robustness of the proposed topology.

Scenarios 3 and 4 are illustrated in Figs. 12(a), 12(b), and 12(c), where, in Fig. 12(a), the results without the load step are presented. It can be observed that even with one open phase and the other connected to a nonlinear load, the grid-side voltage e_g and current i_g remain synchronized. Figs. 12(b) and 12(c) capture the system response when subjecting the converter to simultaneous nonlinear loading on one phase and a load step on the other (leading to a rise in i_{l1}). Throughout this transient event, the DC-link voltage levels remain stabilized at their reference values. Correspondingly, Figs. 14(a) and 14(b) show that load voltages remain unaffected, confirming the dynamic robustness of the 6L topology control scheme.

VIII. CONCLUSION

A single-phase to two-phase AC-DC-AC converter based on a proposed six-leg configuration has been thoroughly

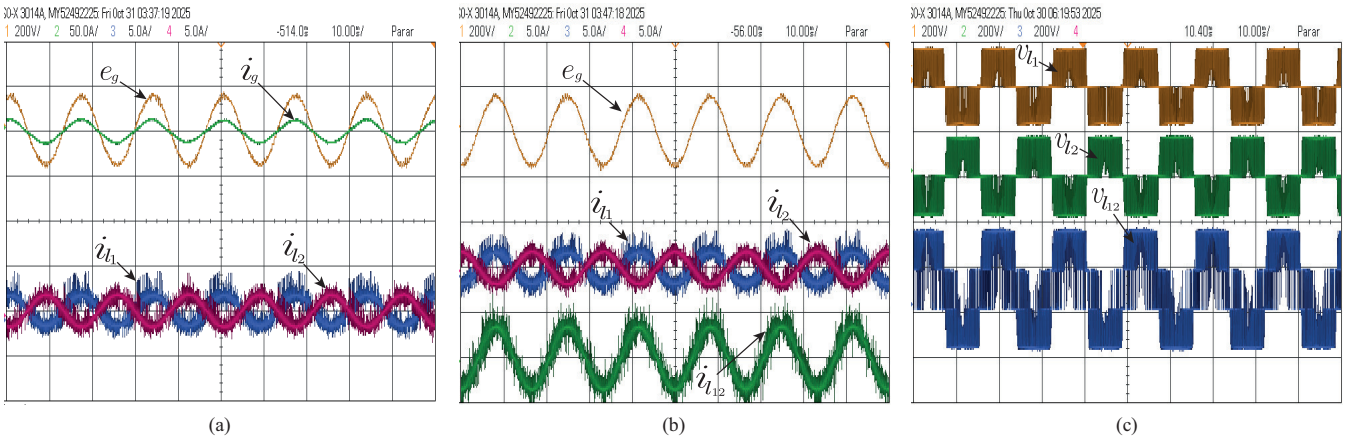


FIGURE 11. Experimental results: (a) Steady-state with balanced loads (e_g, i_g, i_{l1}, i_{l2}, i_{l12}); (b) Steady-state with balanced loads (e_g, i_g, i_{l1}, i_{l2}, i_{l12}); (c) Steady-state with balanced loads (v_{l1}, v_{l2}, v_{l12}).

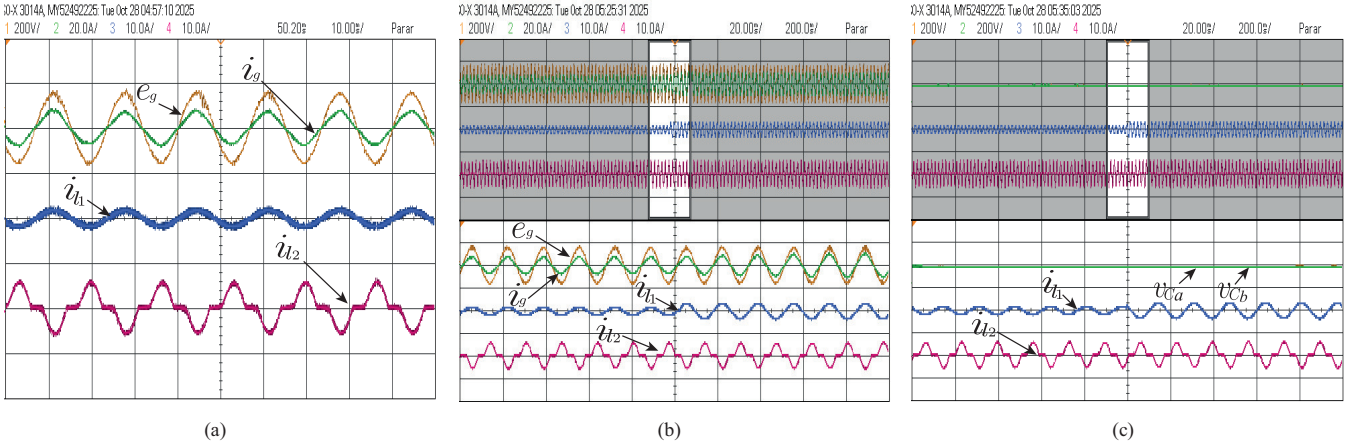


FIGURE 12. Experimental results: (a) Steady-state with a nonlinear load (e_g, i_g, i_{l1}, i_{l2}); (b) Load transient under a nonlinear load (zoom: e_g, i_g, i_{l1}, i_{l2}); (c) Load transient under a nonlinear load (v_{Ck}, i_{l1}, v_{l2}).

investigated. The proposed control and PWM methodologies were verified through simulation and experimental setups, showing robust tolerance to nonlinear/unbalanced loads and power grid anomalies such as voltage swell. DC-link bus regulation remains stable throughout load steps, keeping grid currents sinusoidal and in phase. Loss analysis reveals a 33% reduction in total semiconductor losses for nominal and 10% swell conditions compared to standard topologies, alongside a 28.9% decrease during a 30% sag. Additionally, grid current THD decreases from 5.61% to 2.59%, corresponding to a reduction of approximately 53.8%, demonstrating the improved output power quality. The simulation and experimental results demonstrate the effectiveness of the proposed converter, while the voltage sag performance was verified through simulation.

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AUTHOR'S CONTRIBUTIONS

M.S.O.NETO: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Project Administration, Resources, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **C.B.JACOBINA:** Formal Analysis, Investigation, Methodology, Supervision, Validation. **B.S.GEHRKE:** Software, Supervision, Validation, Visualization. **A.S.FELINTO:** Methodology, Validation. **I.S.D.FREITAS:** Formal Analysis, Supervision. **L.F.M.LUCENA:** Software.

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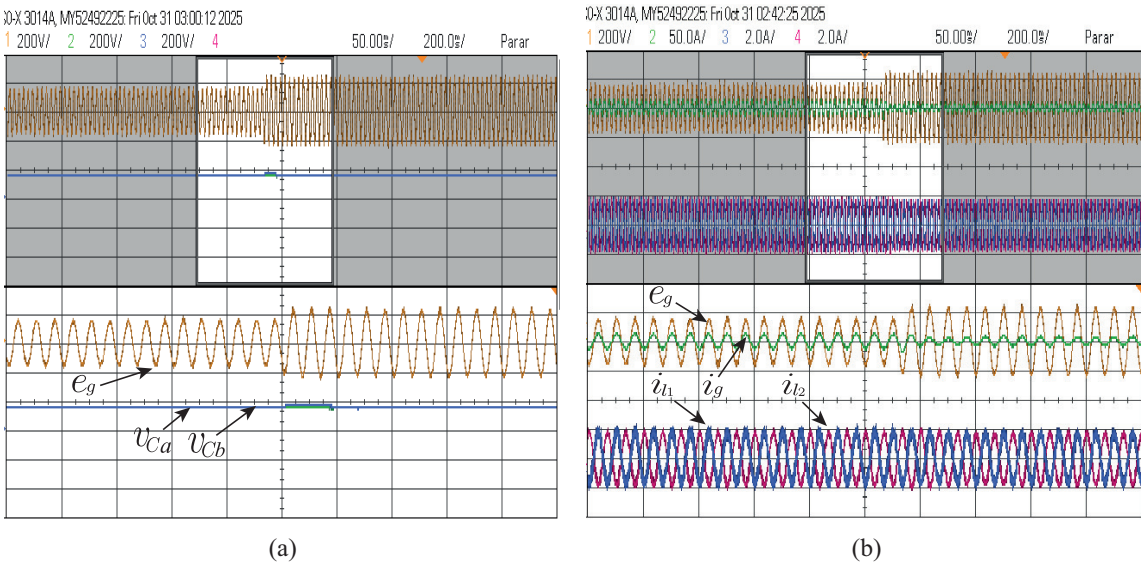

FIGURE 13. Experimental results: (a) Swell with balanced loads (e_g, v_{Ck}); (b) Swell with balanced loads (zoom: e_g, i_g, i_{l1}, i_{l2}, i_{l12}).

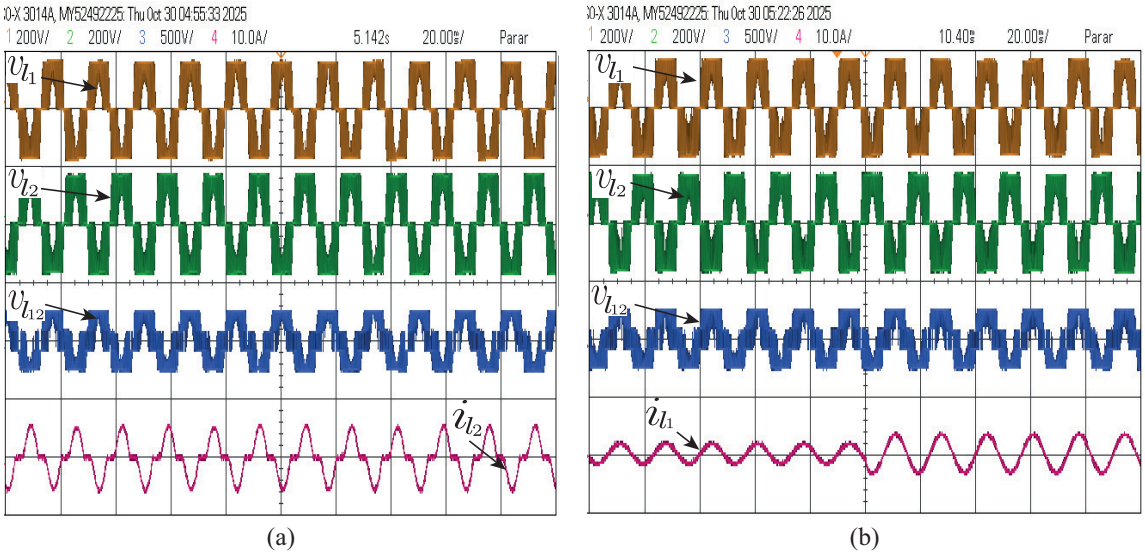

FIGURE 14. Experimental results: (a) Steady-state with a nonlinear load (v_{l1}, v_{l2}, v_{l12}, i_{l2}); (b) Load transient under a nonlinear load (v_{l1}, v_{l2}, v_{l12}, i_{l1}).

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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