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K-Factor Method Approach for Voltage Regulation of CCM Boost Converter

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ABSTRACT This paper presents an approach for the effective control of the output voltage of Boost converters operating in continuous conduction mode, addressing the challenges associated with the presence of a non-minimum phase zero (RHPZ) in their transfer function. The use of a controller designed in the frequency domain using the K-factor method is proposed to compensate for this RHPZ and enhance system stability. The theoretical and practical tests conducted demonstrate that the proposed controller is capable of efficiently mitigating the effects of the RHPZ, resulting in significant improvements in system performance regarding stability and output voltage regulation. This work contributes to the advancement of the field of power converter control, providing an effective solution to the challenges faced in the continuous conduction mode of the Boost converters.

KEYWORDS Boost Converter, Control Systems, Frequency-Domain Control, K-Factor Controller, Non-Minimum Phase Zero, Stability Analysis, Voltage Regulation.

I. INTRODUCTION

Efficient control of power converters is crucial in various applications within power electronics. Among the main topologies, the DC/DC Boost converter stands out due to its capability to increase input voltage, making it widely used in photovoltaic systems, uninterruptible power supplies, LED lighting systems, among other applications and topological variations [1]–[3]. However, controlling this converter, especially in Continuous Conduction Mode (CCM), presents challenges due to the presence of a zero in the right half of the transfer function, resulting in a Non-Minimum Phase (RHPZ) system that can lead to instability [4], [5].

During the initial operation of the Boost converter, there is a drop in output voltage due to the intrinsic operational characteristics of the topology. This behavior results from the time required for the inductor to accumulate sufficient energy to elevate the output voltage to the desired level, adding complexity to the system control, as the output voltage initially tends to move in the opposite direction, potentially affecting stability and regulation [6], [7].

Several studies have addressed this issue, seeking innovative solutions for the effective control of the output voltage of CCM Boost converters.

In this context, [8] investigates the use of a predictive controller with guaranteed nominal stability for regulation, considering small variations in signals and parameters. The results of the study demonstrate the adequate performance of this strategy.

The paper [9] also explores and discusses the aforementioned problem. In this study, different control techniques are applied to mitigate the effects of RHPZ. The results indicate the design of a frequency-domain controller as a satisfactory solution.

Additionally, the study by [10] presents a new topology for the Boost converter that employs a frequency-domain control method to alleviate the effects of RHPZ. As a result, there was an increase in energy efficiency and a reduction in the converter's volume compared to conventional methodologies.

In this context, a promising perspective for regulating the output voltage of Boost converters, even when operating in CCM, is the design of frequency-domain controllers based on the mathematical concept of the K-factor. These controllers are designed to provide phase lead at specific frequencies, thereby compensating for the effects of RHPZ and enhancing system stability [11].

The effectiveness of K-factor based controller design is evidenced in the work of [12], where it was employed to control the output voltage of single-phase inverters. The performance analysis of the controller encompassed scenarios where the inverter powered linear and nonlinear loads, experiencing disturbances in their respective nominal values. Through simulations, the controller's behavior was assessed under various operating conditions, including comparisons with other controllers, demonstrating satisfactory performance and technical feasibility.

The study by [13] highlights that the K-factor method applied to the design of DC/DC converter controllers is a robust and effective approach, which can be easily implemented with operational amplifiers, requiring only the definition of a target crossover frequency and a desired phase margin. The

TABLE 1. Comparative Analysis of Related Works.

Ref.	Approach	Main Objective	Experimental Validation	Main Limitation
[8]	Predictive Control	Improve voltage regulation while ensuring nominal stability	No	Increased implementation complexity and dependence on accurate converter models.
[9]	Comparative Study of Control Techniques	Investigate the effects of the right-half-plane (RHP) zero on controller design	No	Primarily focused on theoretical analysis without practical implementation.
[10]	Modified Boost Topology	Mitigate the effects of the RHP zero through topology modifications	Yes	Requires hardware changes and increases circuit complexity.
[11]	K-factor-based Compensation	Design compensators for Boost converters using frequency-domain techniques	Limited	Focuses mainly on the controller synthesis procedure.
[13]	Fractional-order K-factor Controller	Enhance dynamic performance using fractional-order compensation	Yes	Higher implementation complexity compared with conventional compensators.
This Work	Type III Controller based on the K-factor Method	Provide a unified methodology including modeling, frequency-domain analysis, controller synthesis, analog implementation, and experimental validation	Yes	Restricted to CCM Boost converter applications.

results from mathematical analyses, circuit simulations, and practical experiments demonstrate a consistent correlation, validating the effectiveness and precision of this method in controller design.

Table 1 highlights that previous studies generally focus on specific aspects of the control problem, such as alternative control strategies, topology modifications, or controller synthesis methods. In contrast, the present work provides a unified framework that integrates converter modeling, frequency-domain analysis, controller design, practical analog implementation, and experimental validation, thereby offering a complete design procedure for CCM Boost converters.

Thus, given the complexities faced in regulating the output voltage of the Boost converter, particularly due to the presence of RHPZ, it becomes evident that an advanced approach is necessary to achieve effective control. The technical feasibility of the K-factor based controller design emerges as a promising solution.

Although Type III controllers and the K-factor design methodology are well-established techniques in the literature, there is still a need for comprehensive studies that integrate converter modeling, frequency-domain analysis, controller synthesis, and experimental validation into a unified design framework. In this context, the contribution of this work is not the proposal of a new control strategy, but rather the presentation of a systematic and experimentally validated methodology for the design and implementation of a Type III controller applied to CCM Boost converters affected by the non-minimum phase zero phenomenon. The paper also provides a detailed analytical discussion of the frequency-domain behavior of the converter, supporting the practical implementation of the proposed control solution.

Unlike previous studies that focus either on alternative control strategies, theoretical analyses, or simulation-based evaluations, the present work provides a complete design framework that encompasses converter modeling, frequency-domain characterization of the non-minimum-phase behavior, controller synthesis based on the K-factor method, practical analog implementation, and experimental validation. Therefore, the contribution of this paper lies in the integration of these stages into a unified and reproducible design procedure for CCM Boost converters.

Initially, the challenges faced in controlling Boost converters are explored, emphasizing the presence of RHPZ and its implications. Subsequently, the proposed approach to address these challenges is discussed, utilizing the Type III controller based on the K-factor. A review of the modeling of the Boost converter and the K-factor method is provided, followed by a frequency analysis of the open-loop converter, and finally, the design, simulation, and experimental implementation of the controller. The results obtained in a real test setup confirm the feasibility and effectiveness of the K-factor controller in stabilizing the system, leading to a significant improvement in control performance.

II. BOOST CONVERTER REVIEW

The Boost converter is used in various applications, exhibiting versatility, efficiency and reliability in electric power conversion. The ideal model of the DC/DC Boost converter

is presented in Figure 1, where: V_i is the input voltage; V_o is the output voltage; L is the inductance value; R is the load resistance; C' is the capacitance value; D' is the semiconductor diode and S is the active switch of the topology.

The output voltage regulation of the Boost converter in CCM is necessary to ensure stable operation of the topology. To achieve this, it is essential to establish the structure and parameters of the controller through a transfer function that relates the duty-cycle, which is the input variable, to output voltage. This function $G(s)$ is expressed by (1):

$$G(s) = \frac{\overline{v_o}(s)}{\overline{d}(s)}, \tag{1}$$

where $\overline{d}(s)$ is a duty-cycle disturbance around the operating point and $\overline{v_o}(s)$ is the output voltage small-signal response around an operating point.

Thus, the behavior of the converter can be linearized around an operating point. The small-signal model of the ideal Boost converter is detailed in [14], resulting in the transfer function $G(s)$ defined by (2):

$$G(s) = \frac{\overline{v_o}(s)}{\overline{d}(s)} = K_{gv} \frac{-\frac{L}{R(1-D)^2}s + 1}{\frac{C'L}{(1-D)^2}s^2 + \frac{L}{R(1-D)^2}s + 1}, \tag{2}$$

where D is the duty cycle required to step-up V_i to V_o, calculated by (3).

$$D = 1 - \frac{V_i}{V_o} \tag{3}$$

and K_{gv} is the converter gain, presented in (4).

$$K_{gv} = \frac{V_i}{(1-D)^2} \tag{4}$$

III. K-FACTOR METHOD FOR CONTROLLER DESIGN

The K-factor concept is a fundamental mathematical tool for the design of Type I, II, and III controllers, each providing different phase and attenuation features [15]. In situations that require a phase lead between $+90°$ and $+180°$, the Type III controller, which has two zeros and three poles (one at the origin), is ideal, as it allows for phase adjustment to ensure system stability, even in the presence of non-minimum phase zeros (RHPZ) [16]. The Bode diagram of this controller is shown in Figure 2, where Φ_{cM} represents the maximum phase contribution that should occur at the crossover frequency ω_c.

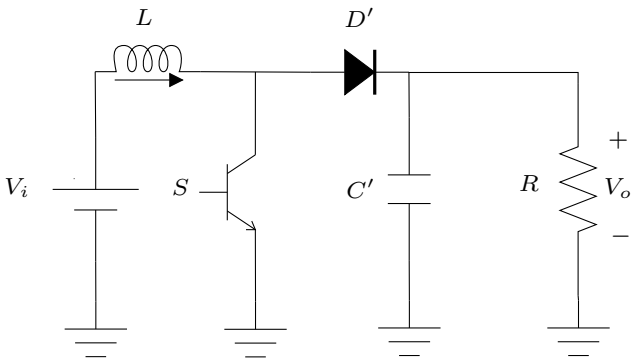


FIGURE 1. Ideal DC/DC Boost converter model.

To optimize the performance of this closed-loop controller, [15] suggests that ω_c should be centered between the frequencies ω_z and ω_p. Thus, the K-factor is a metric that represents the reduction of gain at low frequencies between ω_c and ω_z, and the increase in gain at high frequencies between ω_c and ω_p.

For Type III controllers, which are the focus of this study, the K-factor is calculated using (5):

$$K = (tan^{-1}[0.25(\Phi_c + 180°)])^2. \tag{5}$$

In this way, ω_z is a double zero (6) and ω_p is a double pole (7), which are allocated proportionally to K, with a gain (8), as observed in the transfer function (9).

$$\omega_z = \frac{\sqrt{K}}{K}\omega_c \tag{6}$$

$$\omega_p = \sqrt{K}\omega_c \tag{7}$$

$$\omega_{po} = K_c\frac{\omega_c}{K} \tag{8}$$

$$C(s) = \frac{(1+\frac{s}{\omega_z})^2}{\frac{s}{\omega_{po}}(1+\frac{s}{\omega_p})^2} = \frac{\frac{1}{\omega_z^2}s^2 + \frac{2}{\omega_z}s + 1}{\frac{1}{\omega_{po}\omega_p^2}s^3 + \frac{2}{\omega_{po}\omega_p}s^2 + \frac{1}{\omega_{po}}s} \tag{9}$$

IV. APPROACH USING THE K-FACTOR METHOD APPLIED TO TYPE III CONTROLLERS

This section provides a project overview, presenting the mathematical model of the Boost converter; the frequency domain analysis; the Type III design controller based on the K-factor; and the theoretical and experimental analysis of the controller's performance in a converter prototype. The design parameters are detailed in Table 2.

TABLE 2. Design parameters.

Parameter	Value	Unit
Input Voltage	180	[V]
Output Voltage	400	[V]
Switching Frequency	100	[kHz]
Output Power	975	[W]
Inductance	321.9	[μ H]
Capacitance	165	[μ F]
Duty-Cycle	0.55	-
Load Resistance	164.10	[Ω]
Voltage Sensor Gain	5/400	-
PWM Gain	1	-

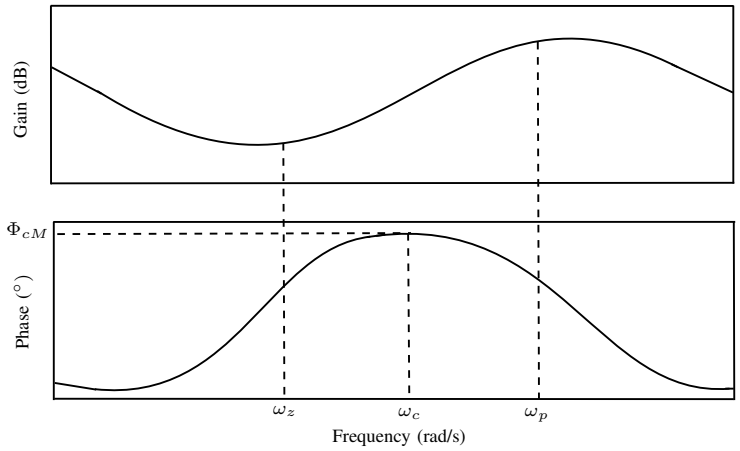


FIGURE 2. Bode diagram of the Type III controller using the K-factor.

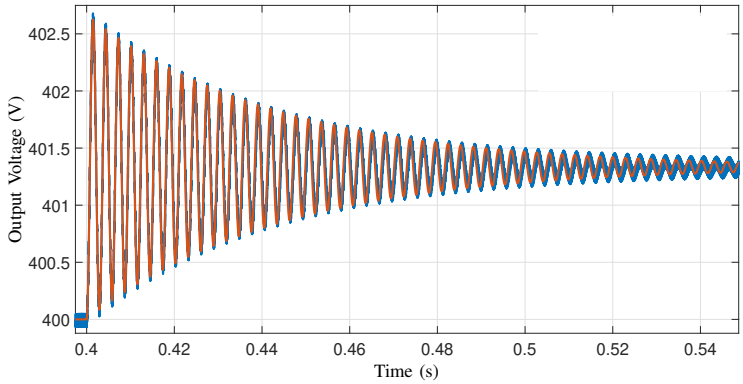


FIGURE 3. Output voltage of the linearized model (red) and the Boost converter (blue) (0.5% of variation in the duty-cycle signal).

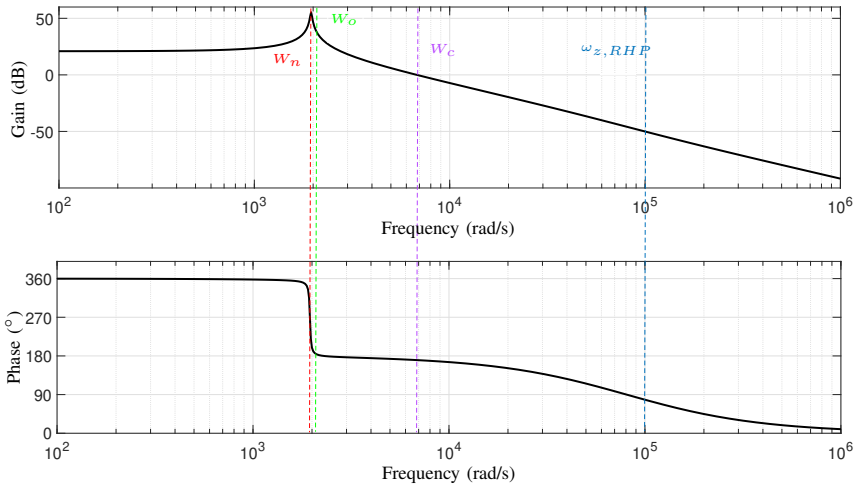


FIGURE 4. Bode diagram of open-loop system.

A. Open-Loop Response and Model Validation

The mathematical model presented in the previous section was linearized around an operating point, and is therefore valid only for small perturbations around this point. Thus, the validation methodology employed is based on applying a small step variation in the duty-cycle. Figure 3 shows the results obtained in open loop configuration. The overlap of the curves indicates a satisfactory correspondence between the theoretical model and the simulated converter response. Additionally, it is observed that the open-loop converter

exhibits oscillatory behavior, which can be attributed to the conjugate complex poles located at $-18 \pm 1952j$ rad/s, according to the parameters presented in the Table 2. It should be noted that the converter presents a non-minimum-phase zero ($\omega_{z,RHP}$ in Figure 4) located at 1.0323×10^5 rad/s. The presence of this right-half-plane zero imposes a fundamental limitation on the achievable control bandwidth, since excessive increases in crossover frequency may lead to instability. Consequently, the controller design must carefully account for this characteristic to ensure adequate transient performance and robustness.

B. Frequency Analysis

The behavior of the open-loop system in the frequency domain must be evaluated, where the gain and phase margins define the stability response.

The open-loop system consists of the PWM gain (G_{pwm}); the voltage sensor gain (H_v); the small-signal model $G(s)$ of the converter; and the model $H(s)$ of the filter that attenuates noise in the measurement, expressed by (10):

$$H(s) = \frac{1}{(\frac{s}{\omega_{co}} + 1)}, \tag{10}$$

where ω_{co} is the cutoff frequency of the filter (rad/s). For simplification, the gains of $G_{ma}(s)$ can be described as a single gain G_K, resulting in (11):

$$G_{ma}(s) = G_K \frac{-\frac{L}{R(1-D)^2}s + 1}{\frac{C'L}{(1-D)^2}s^2 + \frac{L}{R(1-D)^2}s + 1} \frac{1}{(\frac{s}{\omega_{co}} + 1)}, \tag{11}$$

with $G_K = G_{pwm}\ H_v$.

The Bode diagram of $G_{ma}(s)$ is illustrated in Figure 4. A phase-shift of $+360^\circ$ is observed at low frequencies due to the RHPZ. Furthermore, a significant phase transition associated with the complex conjugate pole pair can be observed around the resonant frequency region of the converter. The rate and extent of this phase variation depend on the damping factor and load conditions. Consequently, the phase evolution should be interpreted as a gradual transition over a frequency interval rather than as a discrete phase shift occurring exactly at the natural frequency ω_n.

The ω_n frequency can be obtained using the equation (12), while ω_o is derived through the frequency analysis of the converter by applying the Fourier Transform [16] in open-loop, given by (13).

$$\omega_n = \frac{(1-D)}{\sqrt{LC'}} \tag{12}$$

$$G_{ma}(j\omega) = G_K \frac{-\frac{L}{R(1-D)^2}(j\omega) + 1}{\frac{C'L}{(1-D)^2}(j\omega)^2 + \frac{L}{R(1-D)^2}(j\omega) + 1} \frac{1}{(\frac{j\omega}{\omega_{co}} + 1)} \tag{13}$$

The gain and the phase of $G_{ma}(j\omega)$ are represented, respectively, by equations (14) and (15).

$$|G_{ma}(j\omega)| = G_K\,|G(j\omega)|\,|H(j\omega)| \tag{14}$$

$$\angle G_{ma}(j\omega) = \angle G(j\omega) + \angle H(j\omega) + P \tag{15}$$

Where:

$$|G(j\omega)| = \frac{\sqrt{1 + (\frac{-\omega L}{R(1-D)^2})^2}}{\sqrt{(1 - \frac{C'L\omega^2}{(1-D)^2})^2 + (\frac{L\omega}{R(1-D)^2})^2}} \tag{16}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_{co}})^2}} \tag{17}$$

$$\angle G(j\omega) = tan^{-1}\left(\frac{-\omega L}{R(1-D)^2}\right) - tan^{-1}\left(\frac{\frac{\omega L}{R(1-D)^2}}{1 - \frac{C'L\omega^2}{(1-D)^2}}\right) \tag{18}$$

$$\angle H(j\omega) = -tan^{-1}\left(\frac{\omega}{\omega_{co}}\right) \tag{19}$$

The constant P is an additional phase adjustment that is necessary and characteristic of non-minimum phase systems. Essentially, P must satisfy the following inequalities according to the frequency ω to be analyzed:

$$\left.\begin{array}{lll} P = 2\pi & if & \omega < \omega_o, \\ P = \pi & if & \omega > \omega_o. \end{array}\right\} \tag{20}$$

The frequency ω_o can be obtained by evaluating (15) with $\omega \to \omega_o$ and equating it to π, and its multiples. Considering that $\tan(n\pi) = 0$ for $n = 0, 1, 2...$, the following is obtained:

$$\tan^{-1}\left(\frac{-\omega_o L}{R(1-D)^2}\right) = \tan^{-1}\left(\frac{\frac{\omega_o L}{R(1-D)^2}}{1 - \frac{C'L\omega_o^2}{(1-D)^2}}\right) + \tan^{-1}\left(\frac{\omega_o}{\omega_{co}}\right). \tag{21}$$

Simplifying and rearranging the terms of (21), the equation (22) is obtained.

$$-1 = \frac{(1-D)^2}{(1-D)^2 - \omega_o^2 LC'} + \frac{R(1-D)^2}{\omega_{co}L} \tag{22}$$

Finally, the frequency ω_o is presented by (23).

$$\omega_o = \frac{(1-D)}{\sqrt{LC'}}\sqrt{1 + \frac{\omega_{co}L}{\omega_{co}L + R(1-D)^2}} \tag{23}$$

The crossover frequency ω_c evaluated in Figure 4 is 6.75×10^3 rad/s (or 1.07 kHz) in open-loop situation, where the gain margin and phase margin identified are -29.3 dB and -9.58°, respectively. The fact that both values are negative indicates that the converter is unstable in closed-loop, necessitating an appropriate controller for stabilization.

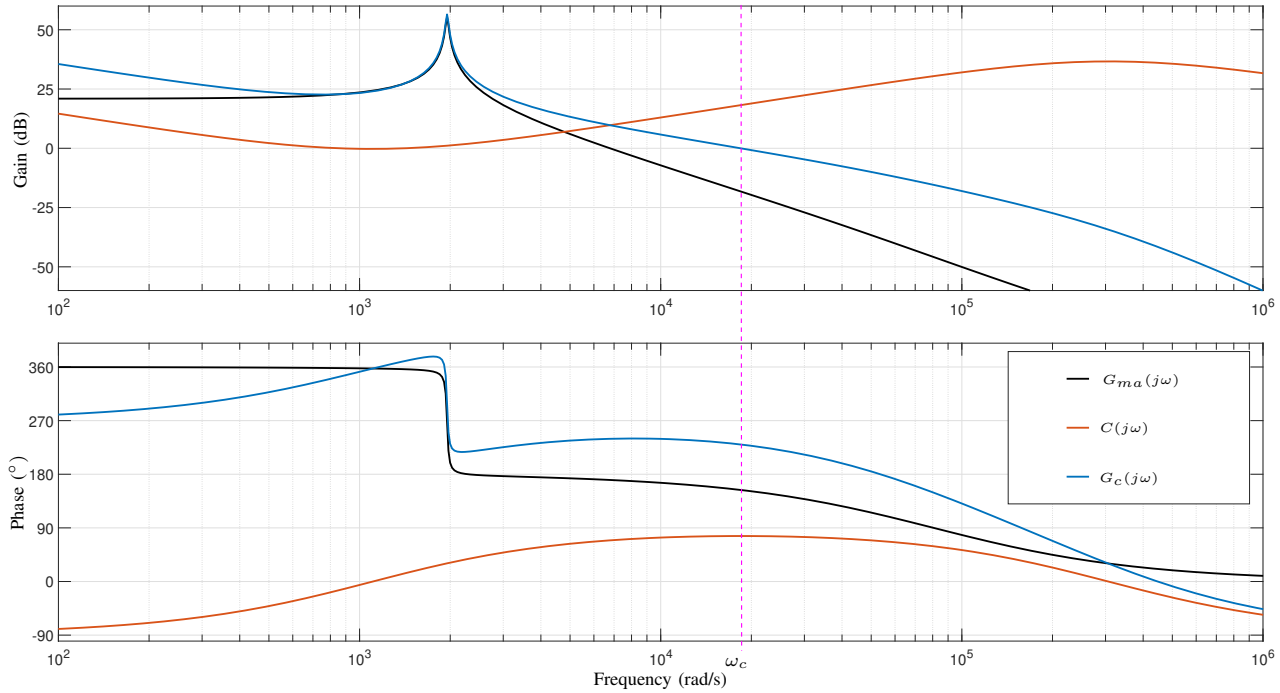


FIGURE 5. Comparison of the frequency responses of $C(j\omega)$, $G_{ma}(j\omega)$ and $G_c(j\omega)$.

C. Controller Design

The controller design (identified as C) essentially aims to provide a necessary phase contribution Φ_c to the converter, such that the phase margin after compensation is positive and within a safe design value.

The first step in the design is the selection of ω_c for the compensated system. The primary constraint for this choice is to limit ω_c to one decade below the switching frequency ω_s of the converter. This ensures that the switching does not influence the gains of the control response. Therefore, $\omega_c < 6.2832 \times 10^4$ rad/s is used for this application.

As suggested by [11] and [17], two additional conditions must be ensured for the design selection. One is that ω_c must be greater than ω_n frequency. Otherwise, there will not be sufficient gain to suppress the effects of resonance, and even with a large phase margin, the system may become unstable. Thus, a plausible choice is $\omega_c > 3\omega_n \therefore \omega_c > 5.8578 \times 10^3$ rad/s.

The other condition is that ω_c must be limited to a maximum of 30% of the converter's zero frequency, which can be expressed as follows:

$$\omega_c < 0.3\frac{R(1-D)^2}{L}, \tag{24}$$

$\therefore \omega_c < 3.0970 \times 10^4$ rad/s. To satisfy the three design conditions, $\omega_c = 1.8414 \times 10^4$ rad/s (or 2930 Hz) is used.

The next step consists of evaluating the gain magnitude and phase of the converter in open-loop at ω_c, that is, in $G_{ma}(j\omega_c)$. Based on (14), (15) and (23), the following relations are obtained:

$$\left.\begin{array}{c} |G_{ma}(j\omega_c)| = -18.1899\ dB, \\ \angle G_{ma}(j\omega_c) = 153.6686^\circ, \therefore \\ \omega_o = 2.2924 \times 10^3\ \text{rad/s}. \end{array}\right\} \tag{25}$$

Thus, to ensure that the converter operates at the specified ω_c after compensation, K_c, as shown in (8), must be calculated to provide a gain contribution of $+18.1899$ dB, resulting in the real gain calculated as follows:

$$K_c = 10^{(\frac{K_{c\_db}}{20})} = 10^{(\frac{18.1899}{20})} = 8.1188. \tag{26}$$

Subsequently, it is necessary to calculate the ϕ_c that must be provided by the controller to ensure that the phase margin of the compensated system meets the design requirements. According to [17], a phase margin of at least 45° is a safe design value that offers robustness. Therefore, a phase margin of 50° is adopted for this application. By definition, MF_d is given by:

$$MF_d = \angle G_c(j\omega_c) - 180^\circ, \tag{27}$$

where $G_c(j\omega_c)$ represents the Fourier Transform of the compensated converter, which can be expressed as follows:

$$G_c(j\omega_c) = G_{ma}(j\omega_c)\ C(j\omega_c). \tag{28}$$

Based on (27) and (28), the desired phase margin can be expressed as:

$$MF_d = \angle G_{ma}(j\omega_c) + \angle C(j\omega_c) - 180^{\circ}, \quad (29)$$

where $\angle C(j\omega_c)$ is calculated using (30).

$$\angle C(j\omega_c) = -90^{\circ} + \phi_c. \quad (30)$$

The -90° phase lag presented in (30) is attributed to the pole at the origin of the controller, which ensures reference tracking for step-type inputs, as previously mentioned. Finally, based on (29) and (30), the ϕ_c can be defined by:

$$\phi_c = MF_d + 270^{\circ} - \angle G_{ma}(j\omega_c) = +166.3314^{\circ}. \quad (31)$$

According to (5), a K-factor of 280.4699 is obtained. Consequently, the other controller parameters are calculated using (6), (7) and (8), resulting in the following transfer function:

$$C(s) = \frac{(8.272 \times 10^{-7})\ s^2 + (0.001819)\ s + 1}{(1.973 \times 10^{-14})\ s^3 + (1.217 \times 10^{-8})\ s^2 + 0.001876\ s}. \quad (32)$$

It should be emphasized that the K-factor-based Type III compensator does not eliminate or relocate the right-half-plane zero of the Boost converter. The non-minimum-phase characteristic remains unchanged, since it is an inherent property of the converter topology. Instead, the controller is designed to operate within the bandwidth limitations imposed by the right-half-plane zero, providing adequate phase margin and robustness. Consequently, the improved dynamic performance is achieved through appropriate loop shaping rather than by modifying the converter intrinsic dynamics.

D. Theoretical Validation of the Proposed Controller

Figure 5 shows the Bode diagrams of $C(j\omega)$, $G_{ma}(j\omega)$ and $G_c(j\omega)$. The crossover frequency is explicitly identified in the magnitude plot by a dashed line located at ω_c is at 1.8414×10^4 rad/s, where the loop gain crosses 0 dB. This increase in bandwidth facilitates faster responses in voltage regulation compared to $G_{ma}(j\omega)$.

The gain contribution of $C(j\omega)$ is added to the gain of $G_{ma}(j\omega)$, resulting in $G_c(j\omega)$ with an increased gain at low frequencies, ensuring reference tracking.

The gain margin of $G_c(j\omega)$ is 10.7 dB. In practice, this value ensures that even with a potential increase of up to 3.427 times in the system gain, the system will still remain stable.

The phase margin of $G_c(j\omega)$ is $+50^{\circ}$, as designed. As expected, $\angle C(j\omega)$ starts at -90° and increases to $\phi_{cM} = +76.33^{\circ}$ at ω_c, resulting in a total contribution of $+166.3314^{\circ}$.

To simulate conditions close to reality, a white noise $N(s)$ with a power of 10×10^{-6} W was added to the output voltage signal. The inclusion of white noise in the voltage feedback signal emulates practical operating conditions. The low-pass filter H(s) attenuates high-frequency noise components, reducing their influence on the control action. Although small fluctuations are introduced in the measured output voltage, the compensated system remains stable and maintains proper voltage regulation. These results demonstrate the robustness of the K-factor-based controller against measurement noise and disturbances.

To evaluate the disturbance-rejection capability of the proposed controller, an external perturbation Q equivalent to 5% of the nominal duty-cycle was injected at the converter input. This perturbation was applied as an additive signal at the plant input, as shown in Figure 6. The variable (V_o') represents the output voltage around the operating point, considering a 400 VDC offset, since the model was linearized.

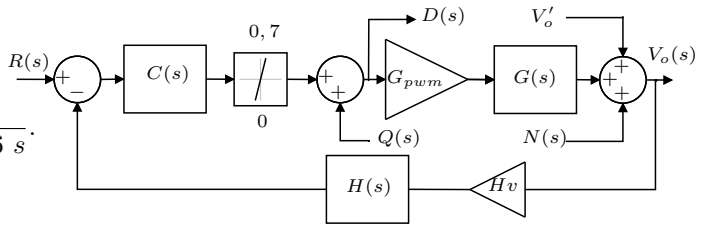


FIGURE 6. Block diagram of the proposed closed-loop control system.

The voltage transient shown in Figure 7(a) (orange) represents the system response to the disturbance and the subsequent regulation process performed by the closed-loop controller. The duty-cycle waveform shown in Figure 7(b) (orange) corresponds to the controller output signal. It is observed that the disturbance is eliminated in approximately 10 milliseconds, reaching a peak voltage of 403.1 V, which corresponds to an overshoot of approximately 0.77% relative to the nominal output voltage of 400 V. This result indicates a significant reduction in settling time compared to the open-loop converter.

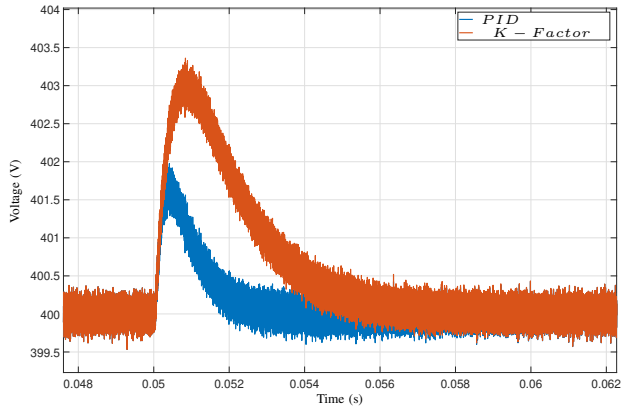
E. Comparative Evaluation with a PID Controller

In order to provide a benchmark against a widely adopted control strategy, a PID controller was designed and evaluated under conditions similar to those employed for the proposed K-factor Type III compensator. The PID parameters were adjusted in the frequency domain to achieve a phase margin close to that obtained with the proposed controller and a similar gain crossover frequency. The resulting controller is described by

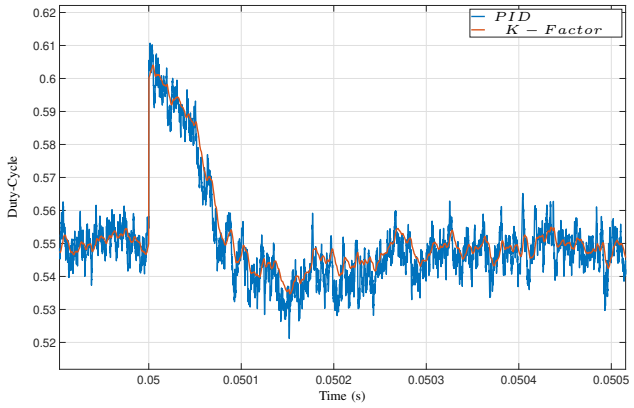
$$C_{PID}(s) = \frac{219.42s^2 + 962117s + 1.0585 \times 10^9}{s(s + 5 \times 10^5)}. \quad (33)$$

The implemented PID controller presents a phase margin of approximately (47.9°) and a crossover frequency of approximately 1.86×10^4 rad/s, which are very close to the values obtained with the proposed K-factor compensator (50°) and 1.8414×10^4 rad/s, respectively. Therefore, both

controllers operate with comparable bandwidth and robustness characteristics, allowing a fair comparison.



(a) Output voltage response.



(b) Duty-cycle response.

FIGURE 7. Closed-loop response under a 5% duty-cycle disturbance injected at the converter input - Comparison between the proposed K-factor Type III compensator and the PID controller.

Figure 7 presents the control signal and the regulated output voltage obtained with both controllers.

It can be observed that the PID controller exhibits a slightly faster transient response and a reduced settling time (Figure 7(a)). However, the proposed K-factor compensator produces a significantly smoother control action, with lower high-frequency oscillations in the duty-cycle signal Figure 7(b). This behavior is directly related to the additional high-frequency pole present in the Type III compensator structure. While both controllers employ a double-zero configuration and an integrator pole, the proposed controller incorporates a double high-frequency pole, resulting in stronger attenuation of high-frequency components.

Consequently, the K-factor compensator provides improved filtering of switching noise and measurement disturbances, reducing the ripple observed in the control signal. This characteristic is particularly relevant in power electronic converters, where switching harmonics and measurement noise are inherently present.

1) PID Controller with Additional High-Frequency Pole

To further investigate the influence of high-frequency filtering on the control performance, a second PID configuration was considered by introducing an additional high-frequency pole into the controller structure. The controller retains the double-zero configuration and the integrator pole of the previous PID, while the additional pole provides increased attenuation of high-frequency components. The controller parameters were adjusted in the frequency domain to maintain a crossover frequency and phase margin comparable to those of the proposed K-factor Type III compensator.

The resulting controller is given by

$$C_{PID,3p}(s) = \frac{2.1878\times10^{8}s^{2}+7.4074\times10^{11}s+6.2699\times10^{14}}{s^{3}+1.5\times10^{6}s^{2}+5\times10^{11}s} \tag{34}$$

The controller presents two coincident zeros, one pole at the origin, and two high-frequency poles located at 5×10^5 rad/s and 1×10^6 rad/s. The resulting crossover frequency is approximately 1.84×10^4 rad/s, with a phase margin close to $50°$, thus maintaining frequency-domain specifications comparable to those of the proposed K-factor compensator.

Figure 8 presents the closed-loop responses of the K-factor compensator and the PID controller with the additional high-frequency pole under the same duty-cycle disturbance considered previously.

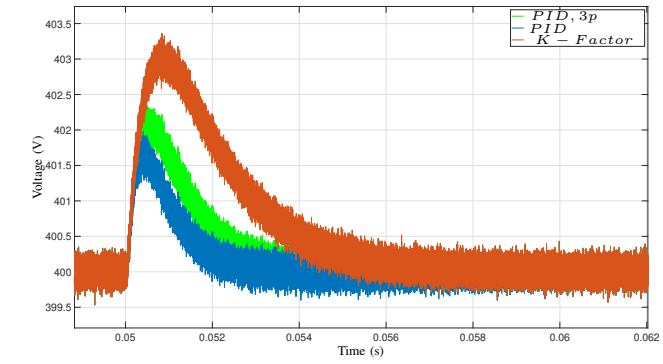
The additional high-frequency pole modifies the transient response while providing further attenuation of high-frequency components in the control signal. Nevertheless, the proposed K-factor compensator maintains a smoother duty-cycle response with lower high-frequency oscillations, as observed in Figure 8(b). A quantitative comparison of the three controllers under different RHPZ conditions is presented in the following subsection.

2) Performance Evaluation under a Reduced RHPZ Frequency

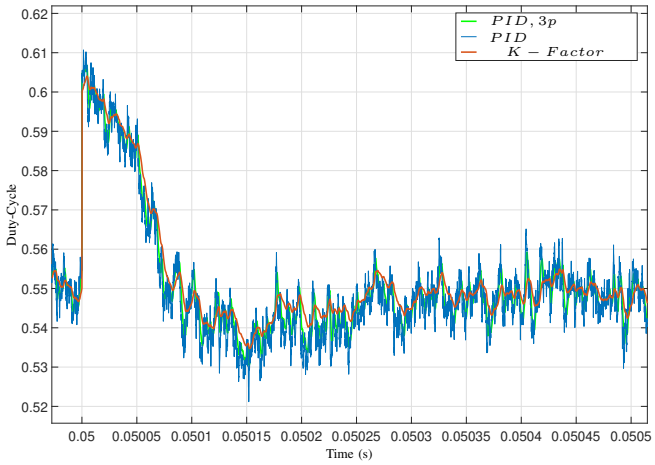
To further investigate the influence of the non-minimum-phase characteristic of the Boost converter, an additional simulation study was performed by progressively increasing the converter output power while keeping the remaining converter parameters unchanged. Since the output voltage is maintained approximately constant, the increase in output power is obtained by reducing the load resistance according to

$$P_o = \frac{V_o^2}{R}. \tag{35}$$

For a Boost converter operating in CCM, the right-half-plane zero frequency is given by



(a) Output voltage response.



(b) Duty-cycle response.

FIGURE 8. Closed-loop response under a 5% duty-cycle disturbance injected at the converter input: comparison between the proposed K-factor Type III compensator and the PID controller with an additional high-frequency pole.

$$\omega_{z,RHP} = \frac{R(1-D)^2}{L}. \tag{36}$$

Therefore, reducing the load resistance progressively shifts the RHPZ toward lower frequencies, making its influence on the closed-loop dynamics increasingly significant. This procedure provides a more demanding simulation scenario without modifying the inductance, capacitance, input voltage, output voltage, or switching frequency of the converter. The three controllers previously designed, namely the proposed K-factor Type III compensator, the PID controller with one high-frequency pole, and the PID controller with two high-frequency poles, were maintained unchanged throughout the analysis.

Four load conditions were considered: $R = 164.1\ \Omega$, $75\ \Omega$, $50\ \Omega$, and $40\ \Omega$, corresponding to output powers of approximately 975 W, 2.13 kW, 3.20 kW, and 4.00 kW, respectively. The corresponding RHPZ frequencies are approximately 103.2, 47.2, 31.5, and 25.2 krad/s. Thus, the ratio between the RHPZ frequency and the crossover frequency is progressively reduced as the load resistance decreases. In particular, for $R = 40\ \Omega$, the RHPZ is located at approximately 25.2 krad/s, which is close to the crossover frequency of the controllers. This condition represents a substantially more challenging non-minimum-phase scenario than that associated with the nominal experimental operating point.

Table 3 summarizes the frequency-domain results obtained for the three controllers. As the load resistance decreases, a progressive reduction in the phase margin is observed for all control strategies. For the proposed K-factor compensator, the phase margin decreases from approximately 50° at the nominal condition to 10.8° for $R = 40\ \Omega$. Similar degradation is observed for both PID controllers, confirming that the progressive approach of the RHPZ toward the crossover frequency imposes an increasingly severe limitation on the achievable closed-loop performance.

TABLE 3. Frequency-domain performance under reduced load resistance.

R	P_o	$\omega_{z,RHP}$	K-factor		PID 2-pole		PID 3-pole	
Ω	W	krad/s	ω_c (krad/s)	PM (°)	ω_c (krad/s)	PM (°)	ω_c (krad/s)	PM (°)
164.1	975	103.2	18.42	50.0	18.60	47.9	18.41	50.0
75	2133	47.2	19.48	36.8	19.64	35.2	19.48	37.2
50	3200	31.45	21.55	22.9	21.72	22.4	21.54	24.1
40	4000	25.2	24.26	10.8	24.49	11.5	24.26	12.9

The temporal response was also evaluated for the same load conditions. A reference step from 400 V to 401 V was applied to the closed-loop system to evaluate the tracking performance of the three controllers while keeping the response close to the nominal operating point around which the converter model was linearized. The overshoot was calculated relative to the final value, while the settling time was determined according to the 2% criterion. The results are presented in Table 4.

At the nominal operating point, the K-factor compensator exhibits the lowest overshoot among the three controllers, with an overshoot of approximately 22.56%. The PID with one high-frequency pole presents an overshoot of approximately 28.2%, while the PID with two high-frequency poles results in approximately 24.0%. As the load resistance is reduced and the RHPZ approaches the crossover frequency, the overshoot increases significantly for all controllers. For $R = 40\ \Omega$, the overshoot reaches approximately 138.6%, 150.1%, and 139.0% for the K-factor, PID with one high-frequency pole, and PID with two high-frequency poles, respectively. These results demonstrate the strong impact of the RHPZ when its frequency becomes comparable to the control-loop bandwidth.

The results reveal a clear trade-off between transient speed and overshoot among the evaluated controllers. The PID controllers consistently provide shorter settling times than the K-factor compensator. However, the proposed compensator generally exhibits lower overshoot than the PID with

TABLE 4. Temporal performance under reduced load resistance.

R	K-factor		PID 2-pole		PID 3-pole	
Ω	OS (%)	t_s (ms)	OS (%)	t_s (ms)	OS (%)	t_s (ms)
164.1	22.56	3.295	28.21	1.312	23.99	1.832
75	46.34	3.276	50.46	1.290	45.59	1.812
50	86.81	3.257	92.23	1.267	85.30	1.792
40	138.56	3.242	150.13	1.381	138.99	1.807

one high-frequency pole, while its overshoot remains very close to that obtained with the PID incorporating two high-frequency poles. The difference between the K-factor and the three-pole PID becomes particularly small as the RHPZ approaches the crossover frequency.

The disturbance-rejection performance was further evaluated by applying a perturbation to the duty-cycle. The resulting output-voltage deviation increases as the RHPZ approaches the crossover frequency, particularly under the most severe load conditions. The PID controllers provide a smaller voltage deviation for the considered disturbance, indicating their advantage in terms of disturbance rejection for the specific operating conditions evaluated. Nevertheless, the K-factor structure presents a distinct characteristic in the high-frequency region that is relevant to switching power converters.

In particular, at the switching frequency of 100 kHz, corresponding to

$$\omega_s = 2\pi f_s = 6.283 \times 10^5 \ \mathrm{rad/s}, \tag{37}$$

the magnitude of the K-factor controller is lower than that of both PID implementations. The resulting gains are approximately 34.6 dB for the K-factor compensator, 44.7 dB for the PID with one high-frequency pole, and 43.2 dB for the PID with two high-frequency poles. Therefore, even after the addition of a second high-frequency pole to the PID structure, the K-factor compensator maintains a lower gain at the switching frequency.

This characteristic is relevant to the implementation of switching converters because high-frequency measurement noise and switching-related components may propagate through the feedback loop and affect the control signal. The lower high-frequency gain of the K-factor compensator consequently results in a lower sensitivity of the control action to high-frequency components. Thus, while the PID controllers exhibit advantages in terms of settling time and, for the considered disturbance, disturbance rejection, the proposed K-factor compensator provides a more attenuated high-frequency control action. The results therefore demonstrate that the main advantage of the proposed structure is not necessarily a faster transient response, but rather the trade-off between dynamic performance and high-frequency attenuation provided by its pole-zero structure, particularly under the non-minimum-phase conditions investigated in this study.

F. Parametric Robustness Analysis

Practical DC–DC converters are subject to component tolerances, aging effects, and operating-point variations that may introduce discrepancies between the nominal model and the physical system. Therefore, an additional simulation-based robustness analysis was performed to evaluate the sensitivity of the proposed controller to variations in the main converter parameters.

The inductance (L), capacitance (C), and load resistance (R) were individually varied around their nominal values while maintaining the controller parameters unchanged. Variations of $\pm 20\%$ were applied to L and C, whereas the load resistance was varied by $\pm 50\%$ in order to represent significant changes in the converter operating conditions. For each case, the open-loop frequency response was evaluated and the resulting crossover frequency and phase margin were recorded. Table 5 summarizes the obtained results.

TABLE 5. Parametric robustness analysis of the proposed controller.

Condition	ω_c (rad/s)	PM (°)
Nominal Model	1.84×10^4	50.0
$L = -20\%$	2.25×10^4	46.6
$L = +20\%$	1.56×10^4	52.1
$C = -20\%$	2.26×10^4	44.0
$C = +20\%$	1.55×10^4	53.8
$R = -50\%$	1.92×10^4	39.1
$R = +50\%$	1.83×10^4	53.5

The results demonstrate that the proposed controller maintains adequate stability margins for all tested operating conditions. Although variations in the converter parameters modify both the crossover frequency and phase margin, the closed-loop system remains stable in every evaluated scenario. The minimum phase margin observed was $39.1°$, obtained for a 50% reduction in the load resistance, which still indicates satisfactory robustness against significant operating-point variations.

The inductance and capacitance variations produced the largest changes in crossover frequency, ranging from 1.55×10^4 rad/s to 2.26×10^4 rad/s . This behavior is expected since both parameters directly affect the location of the converter resonant poles. In contrast, load resistance variations had a stronger influence on the phase margin, particularly under heavy-load conditions, due to their effect on the converter dynamics and the location of the right-half-plane zero.

Overall, the results indicate that the proposed K-factor Type III compensator preserves closed-loop stability and acceptable robustness levels despite substantial variations in the main converter parameters, demonstrating low sensitivity to practical modeling uncertainties and component tolerances.

G. Experimental Validation of the Proposed Controller

To validate the performance of the proposed control strategy, an experimental prototype of a Boost converter was devel-

oped, and a series of tests were conducted on it, as discussed in the following subsections.

Figure 9 shows the experimental prototype used to validate the proposed control strategy. The setup consists of the CCM Boost converter, the analog control circuit based on the K-factor design methodology, the voltage sensing stage, and the PWM generation circuitry used during the experimental tests.

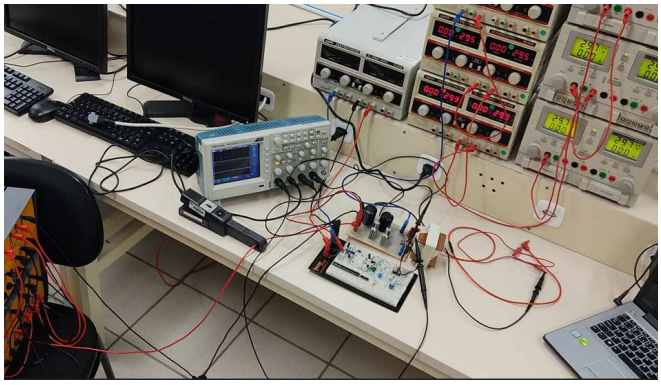


FIGURE 9. Experimental prototype of the Boost converter and analog control platform used for validation of the proposed controller.

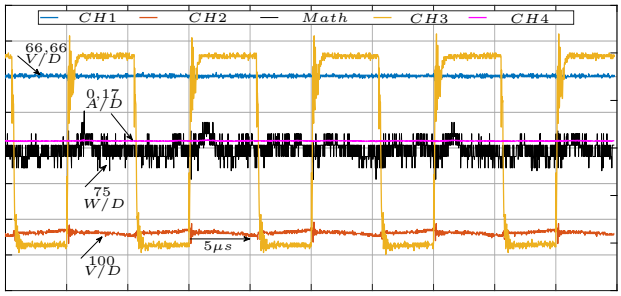
1) Open-Loop Behavior of the Boost Converter

The model presented in Figure 1 and represented in (2) does not consider converter non-idealities. In practice, one of the consequences of these non-idealities is the drop in the output voltage of the converter, which requires the controller to increase the duty-cycle to achieve the control objective.

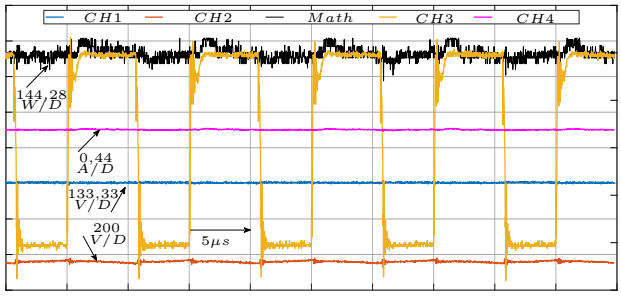
In order to evaluate the impact of converter non-idealities on the duty-cycle predicted by the ideal model, a set of open-loop tests was performed. During these tests, the duty-cycle was initially kept constant while the output power was progressively increased by reducing the load resistance. The objective was to determine the operating range over which the theoretical duty-cycle remained valid and to quantify the additional duty-cycle required to compensate for converter losses at higher power levels.

In Figure 10(a), the converter delivers a power of 298 W (approximately 30% of the nominal power) with $D = 0.55$. At this power level, the voltage drop at the output due to losses is negligible, as, according to (3), for $V_i = 181\ V \rightarrow V_o \approx 401\ V$. This duty-cycle was maintained until the power reached approximately 767 W (about 78% of nominal power). It was then increased to $D = 0.564$ (Figure 10(b)).

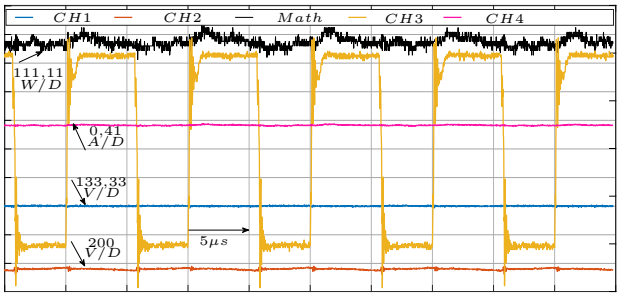
The value of $D = 0.564$ was maintained until the nominal load of 975 W was obtained, as illustrated in Figure 10(c). Thus, it can be concluded that a small increase of 2.54% in the ideal duty-cycle is necessary to compensate for the losses of the converter at full load. Specifically, according to (3), for $D = 0.564$, $V_i = 180\ V \rightarrow V_o = 412\ V$, indicating



(a) $CH1 = 401$ V, $CH2 = 181$ V, $CH3 = 0.55$, $CH4 = 0.742$ A, $Math = 298$ W.



(b) $CH1 = 402$ V, $CH2 = 180$ V, $CH3 = 0.565$, $CH4 = 1.91$ A, $Math = 767$ W.



(c) $CH1 = 401$ V, $CH2 = 180$ V, $CH3 = 0.565$, $CH4 = 2.43$ A, $Math = 974$ W.

FIGURE 10. Open-loop output power tests to evaluate the impact of non-idealities on the duty-cycle of the converter. $CH1$: Output voltage - [RMS]; $CH2$: Input voltage- [RMS]; $CH3$: Gate signal; $CH4$: Output current - [RMS]; $Math$: Output power - [Average].

a voltage drop of 11 V that needs to be compensated by the controller. This value represents a relative error of 2.74%, confirming the effective approximation of the ideal model compared to the experimental circuit.

2) Control Loop Using Operational Amplifiers

Figure 11 presents the complete control loop implemented using operational amplifiers. In this application, the sensor Hv is a simple voltage divider followed by a buffer for impedance elevation and isolation. For a gain of $5/400$, the resistor values are $R4 = 55.300 \times 10^6\ \Omega$ and $R5 = 700 \times 10^3\ \Omega$. The filter $H(s)$ is represented by:

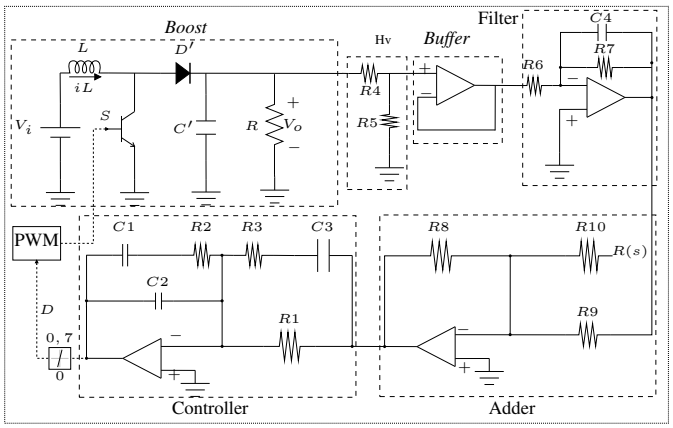


FIGURE 11. Control loop of the system using operational amplifiers.

$$H(s) = -\frac{R_7}{R_6}.\frac{1}{(C_4R_7)s+1}. \tag{38}$$

To achieve the defined ω_{co}, $C_4 = 15.915 \times 10^{-9}$ F and $R_7 = 1000\ \Omega$. For unity gain, the resistor $R_6 = 1000\ \Omega$. Since the amplifier is inverting, the output signal of the filter is negative, and it needs to be summed with reference voltage $R(s)$ to calculate the error. As the gain of the summing amplifier must be unity, then resistors $R_{8-9-10} = 1000\ \Omega$.

Finally, for the controller components design, $R_1 = 10000\ \Omega$ is chosen arbitrarily, and the remaining values are calculated as follows:

$$C_2 = \frac{1}{\omega_c R_1 K_c} = 668.90 \times 10^{-12}\ F, \tag{39}$$

$$C_1 = C_2(K-1) = 186.94 \times 10^{-9}\ F, \tag{40}$$

$$R_2 = \frac{\sqrt{K}}{\omega_c C_1} = 4.8652 \times 10^{3}\ \Omega, \tag{41}$$

$$R_3 = \frac{R_1}{K-1} = 35.7820\ \Omega, \tag{42}$$

$$C_3 = \frac{1}{\omega_c R_3 \sqrt{K}} = 90.625 \times 10^{-9}\ F. \tag{43}$$

3) Disturbance Rejection of the Controlled Boost Converter

Figure 12 shows the closed-loop response of the Boost converter under different operating disturbances. During the entire test, the output voltage reference was maintained at 400 V and the load remained at its nominal value of approximately 975 W. At time t_1, a disturbance equivalent to 5% of the nominal duty-cycle was applied. This resulted in an overshoot of 405.4 V (1.35%) in V_o, which was rejected after 10 milliseconds. The overshoot was 2.3 V higher than that shown in Figure 7, a fact justified by the non-idealities not represented in the model and the approximation of the resistor and capacitor values compared to the calculated ones.

Additionally, at time t_2, the input voltage was changed from 180 V to 210 V and subsequently, at t_3, from 210 V to 190 V, while maintaining the nominal load and the 400 V output voltage reference unchanged. In all cases, the system quickly returned to the operating point. The transient responses reached peak values of 405.63 V and 395.7 V, corresponding to deviations of approximately $+1.41\%$ and -1.08% relative to the nominal output voltage, respectively.

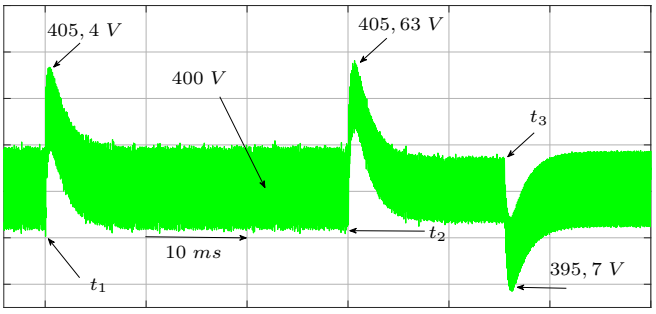


FIGURE 12. Regulation of the output voltage in closed loop with small disturbances.

The experimental results are consistent with the theoretical predictions obtained during the controller design stage. In all tested conditions, the output voltage remained close to its nominal value, presenting limited overshoot and fast recovery after disturbances. The observed transient responses confirm that the selected crossover frequency and phase margin provide adequate robustness and stability. Furthermore, the close agreement between the simulation and experimental results demonstrates that the proposed K-factor-based design methodology is effective for practical implementation in CCM Boost converters.

V. CONCLUSION

In this study, an advanced control system was developed and validated for regulating the output voltage of CCM Boost converters, using the K-factor method applied to Type III controllers. The experimental results confirmed the effectiveness of the control strategy in stabilizing the output voltage in the presence of disturbances.

The analysis of the dynamic responses and validation through a physical prototype demonstrated that the proposed controller not only efficiently compensated for the non-minimum phase zero, but also improved the overall stability of the system, reducing settling time and minimizing overshoot. These results reinforce the feasibility of the K-factor method as a robust and effective solution for applications in Boost converters. Although the K-factor methodology and Type III compensation are well-established techniques, the present work contributes by providing a detailed analytical and experimental framework for their application to CCM Boost converters affected by non-minimum-phase behavior. The proposed methodology integrates converter modeling, frequency-domain analysis, controller design, and

experimental validation into a unified procedure, offering a practical reference for the implementation of voltage control systems in power electronics applications.

As a natural extension of this work, future research will focus on a more comprehensive experimental validation of the proposed controller under dynamic operating conditions, including load-step and reference-step tests, to further evaluate its transient response and robustness.

AUTHOR'S CONTRIBUTIONS

E.B.MARTINS: Investigation, Validation. **F.W.BRANCO:** Investigation, Validation. **T.H.MOMBACH:** Methodology. **R.SILVA:** Funding Acquisition, Supervision. **D.F.KLOTZ:** Conceptualization, Writing – Original Draft. **J.FRAYTAG:** Supervision, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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