Original Paper

Eletrônica de Potência
Open Journal of Power Electronics



Received July 13, 2026; Received in revised form August 26, 2026; Accepted September 29, 2026; Date of publication October 16, 2026.
The review of this paper was arranged by Associate Editor Riccardo Mandrioli and Editor-in-Chief Allan F. Cupertino.
Digital Object Identifier http://doi.org/10.18618/REP.e202633

Comparison of 2-, 3-, and 5-Level Topologies for Medium-Voltage Grid-Tied Converters: Trade-offs in Efficiency, Cost, and Power Density

Magno O. Schneider[1,*], **Gustavo V. Barbosa**[1], **Gabriel A. Fogli**[1,2], **Thiago R. de Oliveira**[1,2], **Lenin M. F. Morais**[1,2].

[1]Universidade Federal de Minas Gerais, Graduate Program in Electrical Engineering, Belo Horizonte - Minas Gerais, Brazil.
[2]Universidade Federal de Minas Gerais, Department of Electronic Engineering, Belo Horizonte - Minas Gerais, Brazil.

e-mail: magnotton@ufmg.br*; gustavovbarbosa@ufmg.br; gabrielfogli@gmail.com; troliveira@cpdee.ufmg.br; lenin@cpdee.ufmg.br.
*Corresponding author.

ABSTRACT The increasing integration of distributed energy resources, renewable generation, and electric vehicles is reshaping modern distribution networks, introducing challenges such as voltage regulation issues, bidirectional power flows, and reduced system inertia. In this context, microgrids and clustered microgrids rely on bidirectional interlinking converters (BICs) to enable controlled power exchange, provide ancillary services, and improve system flexibility. This paper presents a multiobjective design methodology for BICs based on transformer-coupled back-to-back converter architectures. The proposed framework evaluates two-, three-, and five-level topologies under low- and medium-voltage DC-link configurations using SiC and IGBT semiconductor technologies. The solution space is analyzed in terms of efficiency, power density, and cost, enabling a comparison of competing solutions. The results demonstrate that the optimal design is strongly dependent on voltage level and semiconductor selection. For low-voltage DC-link, two-level converter topologies using SiC devices at 10 kHz switching frequency provide the best trade-off among the considered figures of merit. For medium-voltage systems, three-level NPC topologies with hybrid SiC/IGBT implementations achieve higher efficiency and power density while maintaining low cost levels.

KEYWORDS Multiobjective Converter Design, Bidirectional Interlinking Converter, DC-Link Voltage.

I. INTRODUCTION

The growing integration of distributed generation (DG), energy storage systems (ESSs), and electric vehicles (EVs) has introduced new operational challenges in modern distribution networks, such as voltage regulation, bidirectional power flows, increased fault current levels, and reduced system inertia [1]. In this context, microgrids have emerged as an effective framework for the coordinated operation of local generation, ESSs, and controllable loads [2]. As the number of microgrids continues to increase, the concept of clustered microgrids has emerged as a natural evolution of conventional distribution systems [3]. In these architectures, power exchange among neighboring microgrids is achieved through a bidirectional interlinking converter (BIC) [4]. Acting as bidirectional and controllable power-flow interfaces, the BIC regulates energy transfer between interconnected microgrids while providing ancillary services such as voltage support, fault current limitation, and power quality improvement [5]. Their deployment enables coordinated operation of multiple microgrids and supports the development of more flexible distribution networks, as illustrated in Fig. 1.

Despite their growing importance, most reported BIC implementations remain focused on low-voltage (LV) and low-power (LP) applications. In contrast, medium-voltage (MV) and high-power (HP) systems impose additional challenges associated with semiconductor voltage and current ratings, thermal management, and converter scalability. However, they also enable the direct interconnection of feeders and microgrid clusters at power levels ranging from hundreds of kilowatts to several megawatts [4]. Among the various design parameters, the DC-link voltage plays a critical role, as it directly influences the selection of semiconductor devices and passive components. Higher DC-link voltages enable

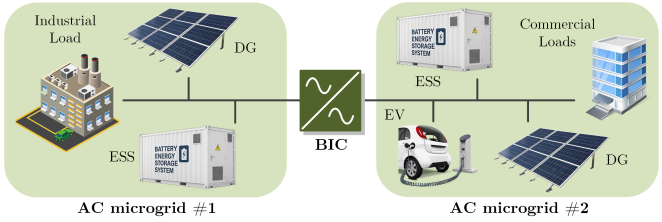


FIGURE 1. Connection of two microgrids via a BIC.

CC BY

the use of MV-rated devices, reducing current stress and conduction losses, whereas lower voltages allow the adoption of advanced LV-rated devices with superior switching performance and potentially lower costs. As a result, the DC-link voltage introduces a fundamental trade-off among efficiency, cost, and power density.

Several BICs architectures have been proposed for MV microgrid interconnection, differing mainly in the way MV conversion and galvanic isolation are achieved, each presenting different trade-offs as illustrated in Fig. 2. One of the most established solutions consists of transformer-coupled back-to-back voltage-source converters (VSCs) employing low-frequency transformers (LFTs), as shown in Fig. 2(A). This architecture exploits the technological maturity of conventional two-, three-, and five-level VSCs, straightforward control implementation, and galvanic isolation provided by the LFT [6]. Furthermore, the transformer turns ratio allows the DC-link voltage to be selected over a wide range, enabling either LV- or MV-based converter implementations according to the application requirements [7].

An alternative approach is the use of Modular Multilevel Converters (MMCs), as shown in Fig. 2(B), which enable direct MV operation through the series connection of multiple submodules [8]. MMCs offer excellent output waveform quality, reduced filtering requirements, modular construction, and high scalability. Nevertheless, these advantages are achieved at the expense of a significantly larger number of semiconductor devices, increased control complexity, and additional challenges associated with capacitor voltage balancing and submodule (SM) management. Furthermore, the classical MMC topology does not inherently provide galvanic isolation, often requiring an additional LFT in applications where electrical isolation is mandatory [9].

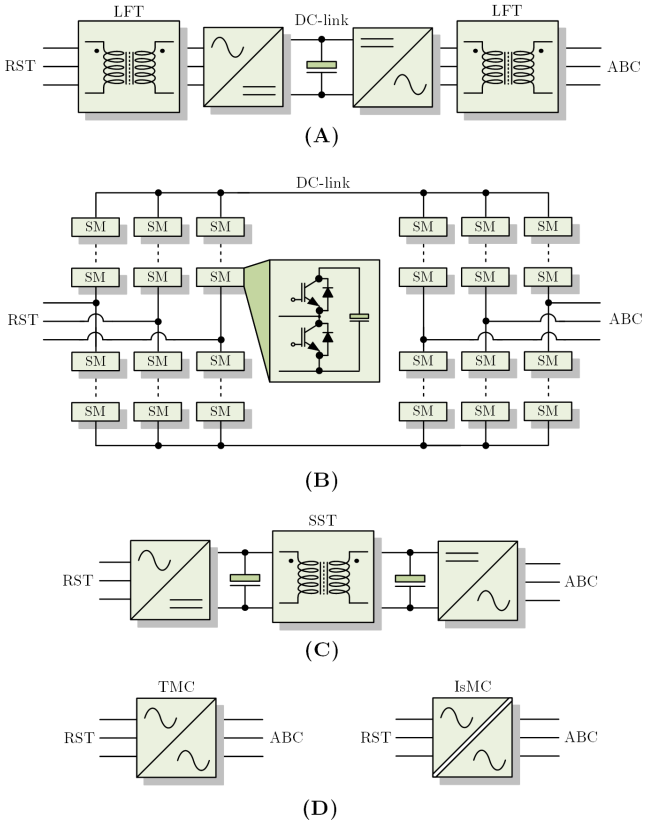


FIGURE 2. Representative medium-voltage interlinking converter architectures for microgrid interconnection: (A) transformer-coupled back-to-back VSC with LFTs, (B) MMC-based interface, (C) SST-based interface, and (D) matrix-converter-based interfaces, including TMC and IsMC.

Another possibility is the Solid-State Transformer (SST) architecture depicted in Fig. 2(C), which replaces the LFT with a high-frequency isolated stage [10]. SSTs can achieve higher power density while providing galvanic isolation through high-frequency transformers (HFT). In addition, their architecture is extended to multiport configurations, enabling the integration of multiple feeders, distributed generators, and energy storage systems through a common conversion stage, thereby enhancing system scalability and flexibility. [11]. However, they typically require multiple conversion stages, resulting in increased complexity, higher component count, and potentially lower efficiency depending on the operating conditions [12].

Matrix-converter-based solutions, illustrated in Fig. 2(D), represent a further alternative [13]. Depending on the application requirements, they are implemented either as a Transformerless Matrix Converter (TMC) or as an Isolated Matrix Converter (IsMC). Their main advantages include the elimination of bulky DC-link capacitors, inherent bidirectional power flow capability, and high power density. However, the absence of a DC-link limits the maximum output voltage to a fraction of the input voltage under conventional modulation strategies, resulting in a more restrictive voltage transfer ratio. In addition, matrix converters require complex commutation schemes and more sophisticated modulation and protection techniques to ensure safe and reliable operation [14].

Among the available alternatives, transformer-coupled back-to-back VSCs remain particularly attractive because they combine the maturity of conventional converter technology with the flexibility provided by the LFT. This topology has been widely adopted in medium- and high-power applications, including variable-speed motor drives, wind energy conversion systems, railway traction systems, and asynchronous AC grid interconnections, demonstrating its reliability and versatility [15], [16]. Moreover, compared with MMC-, SST-, and matrix-converter-based solutions, back-to-back converters rely on well-established topologies and commercially available semiconductor modules, resulting in lower implementation risk and facilitating scalable megawatt-level microgrid interconnection systems.

Although studies have investigated the control, operation, and topology selection of BICs, comparatively little attention has been devoted to their hardware design [6], [17], [18]. Consequently, hardware decisions are often based on isolated

design criteria or empirical choices, leading to suboptimal compromises among efficiency, cost, and power density. This limitation becomes increasingly critical as the growing diversity of semiconductor technologies, converter topologies, and other hardware components considerably expands the solution space, making intuitive design decisions impractical. Therefore, a multi-criteria design methodology capable of simultaneously evaluating these competing objectives is essential to identify well-balanced hardware configurations and support informed design decisions [19].

To address this gap, this paper proposes a multiobjective hardware design methodology for HP transformer-coupled BICs. Unlike most previous studies [17], [18], the proposed approach focuses on the converter hardware design stage by evaluating conventional two-, three-, and five-level converter topologies implemented with both LV- and MV-rated semiconductor devices. Depending on the selected converter topology and transformer turns ratio, the DC-link voltage is established at either the LV or MV level, enabling different hardware configurations to be explored. By systematically evaluating the resulting trade-offs among efficiency, cost, and power density, the proposed methodology identifies balanced and practically feasible design solutions, providing quantitative support for hardware selection in HP BIC applications.

This paper is organized as follows. Section II presents the converter design assumptions and boundary conditions, followed by the description of the investigated converter topologies, the selection of semiconductor devices, the design procedures for the LCL filters, DC-link capacitors, and flying capacitors. Section III describes the proposed multiobjective hardware design methodology, including the design workflow and the models adopted for evaluating efficiency, power density, and specific cost. Section IV presents and discusses the optimization results for the low and medium voltage DC-link configurations. Finally, Section V presents the conclusions of this paper.

II. CONVERTER DESIGN

A. Design Assumptions and Boundary Conditions

Most parameters in converter design, such as switching frequency, device type and technology, capacitors, and gate-drive circuits, are not linearly independent. The choice of a single parameter directly affects other aspects of the design, even if indirectly, with varying levels of influence. Consequently, although converter design involves a large number of degrees of freedom, practical implementations must satisfy application-specific requirements, technical standards, and other design constraints. Even in multiobjective design studies, such as [17], [18], [20], where several parameters are simultaneously optimized, a set of design assumptions and boundary conditions must be established to ensure a consistent and practically feasible evaluation.

The design specifications adopted in this work represent a HP BIC intended for the interconnection of MV microgrids through a LFT. A rated power of 1 MW is selected as a representative operating point for this application, while the DC-link and converter AC-side voltage levels are chosen to enable a comparison between LV- and MV-based converter implementations. Although the selected switching-frequency range may be considered relatively low for SiC technology, it was limited to account for the high power level and the switching-loss and thermal constraints of the selected high-voltage devices. Similar lower-kilohertz operation has been reported for megawatt-scale converters using high-voltage SiC devices [21], [22]. Therefore, a maximum frequency of 10 kHz was considered representative of the target application.

TABLE 1. Design specifications and operating conditions.

Parameter	Symbol	Value
Rated active/apparent power	P_n/S_n	1 MW/MVA
Grid frequency	f_g	60 Hz
Switching frequency	f_{sw}	2.5, 5, and 10 kHz
DC-link voltage	V_{dc}	900 V and 2 kV
Converter AC-side voltage	V_g	380 V and 1.2 kV
Heatsink temperature	T_h	80°C
Grid filter	–	LCL
Semiconductor technology	–	Si IGBT and SiC MOSFET
LFT voltage ratio	–	0.38/13.8 kV or 1.2/13.8 kV

In this work, two DC-link voltage levels are considered: 900 V and 2000 V, associated with 1700 V and 3300 V semiconductor devices, respectively. The corresponding AC voltage levels are 380 V and 1200 V, selected to be adequately synthesized from the respective DC-link voltages while maintaining an appropriate voltage margin. Due to the LFT, other AC voltage levels can also be accommodated by adjusting the transformer turns ratio. Although insulation requirements increase with voltage, their specific impact on cost was not considered in this work, as it would require a dedicated insulation-system design. The remaining assumptions correspond to common design choices for this class of converters and are maintained throughout the analysis to ensure a consistent comparison among the evaluated hardware configurations.The adopted design specifications and operating conditions are summarized in Table 1.

B. Two-Stage Converter Topologies

The converter is composed of two main stages. The first stage is an AC/DC converter, and the second stage is a DC/AC converter, connected through a DC-link. Both the input and output sides include LCL filters to ensure compliance with power quality requirements, as illustrated in Fig. 3. Since the system operates on a MV grid with restricted access, direct connection at this voltage level is not feasible, leading to the adoption of transformer-based topologies.

This paper evaluates representative two-, three-, and five-level converter topologies for MV/LV BICs. The investigated configurations include the two-level Full-Bridge (FB) converter and the three-level Neutral-Point-Clamped (NPC),

CC BY

TABLE 2. Selected semiconductor components.

Device	Type	Packaging	Current	Voltage	Price [US$]
FZ2400R17HE4P_B9	IGBT	Discrete	2400 A	1.7 kV	1,427.51
2×(MSCSM170AM029CT6LIAG)	SiC	HB	2×538 A	1.7 kV	3,649.90
DIM1200FSM17-A000	IGBT	Discrete	1200 A	1.7 kV	1,244.92
FF2600UXTR33T2M1	SiC	HB	720 A	3.3 kV	4,827.27
MSCSM170AM029CT6LIAG	SiC	HB	538 A	1.7 kV	1,824.95
FZ800R33KF2C	IGBT	Discrete	800 A	3.3 kV	1,760.01
FF1800R12IE5	IGBT	Discrete	1800 A	1.2 kV	674.95
4×BSM600D12P3G001	SiC	HB	4×576 A	1.2 kV	7,326.80
DZ3600S17K3_B2	Diode	3 Discrete	3600 A	1.7 kV	518.00
DFM1200NXM33	Diode	2 Discrete	1200 A	3.3 kV	343.35

Flying Capacitor (FC), and T-Type NPC (T-NPC) topologies, each evaluated under both LV and MV DC-link configurations. In addition, the five-level NPC (5L-NPC) and five-level Active Neutral-Point-Clamped (5L-ANPC) topologies are investigated exclusively under MV conditions. The evaluated topologies are depicted in Fig. 4, and the corresponding operating conditions are summarized in Table 1.

C. Semiconductors

This work considers commercially available IGBT and SiC MOSFET power modules suitable for medium- and HP converter applications, as summarized in Table 2. The selected devices are chosen to cover the voltage and current ratings required by the converter specifications presented in Table 1. Preference is given to industrial-grade modules from established manufacturers, including both LV- and MV-rated devices, enabling a consistent comparison of alternative converter topologies and DC-link voltage levels. Depending on the converter requirements, single modules or parallel-connected modules are considered to satisfy the required current ratings.

Although IGBTs remain an attractive solution due to their lower cost and widespread industrial adoption, SiC MOSFETs offer superior switching performance and higher efficiency, particularly in HP, high-frequency, and high-power-density applications [23]. While both SiC and GaN technologies generally outperform Si-based IGBTs, GaN devices are not considered because high-voltage, high-current modules suitable for the investigated power levels are not yet widely available commercially.

The selected devices comprise both conventional discrete-packaged modules and half-bridge (HB) power modules. For high-current operating conditions, multiple devices connected in parallel are considered when a single commercially available module could not satisfy the required current rating.

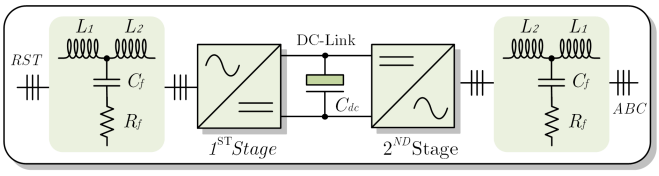


FIGURE 3. Back-to-back structure with two VSCs, common DC-link, and LCL filters at the AC connection.

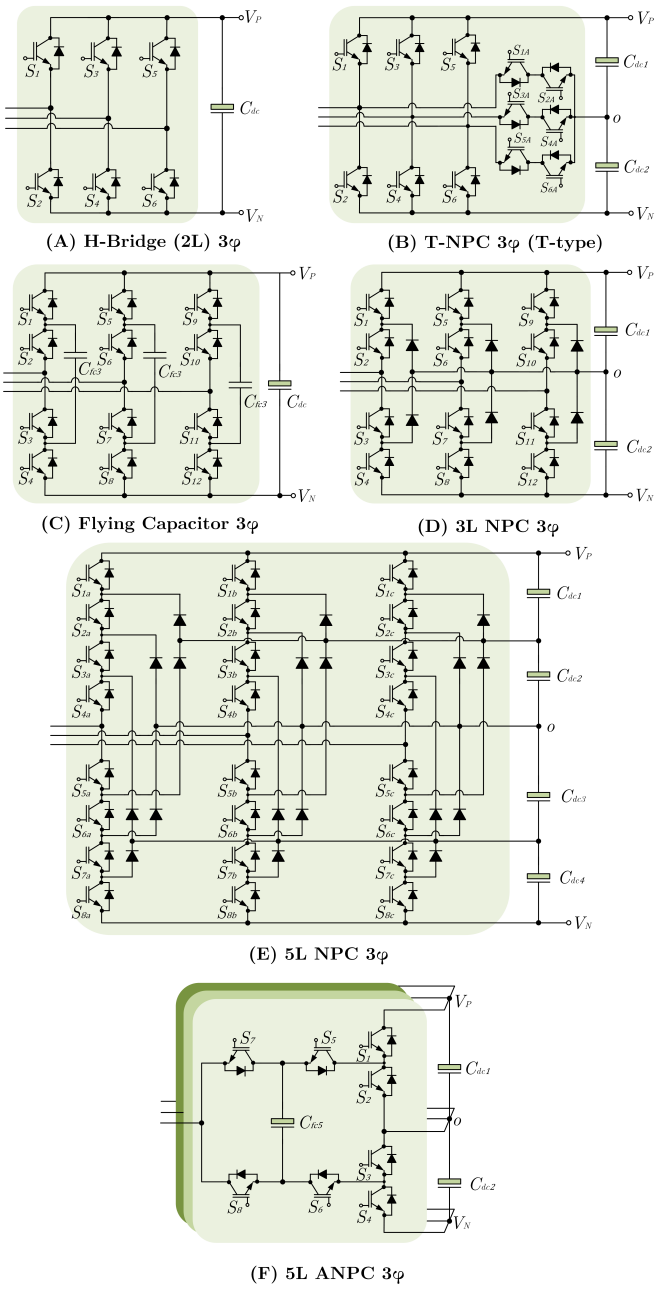


FIGURE 4. Power converter topologies evaluated for each stage of the back-to-back converter. (A) three-phase 2L-FB, (B) three-phase 3L-T-NPC, (C) three-phase 3L-FC, (D) three-phase 5L-NPC, and (E) three-phase 5L-ANPC.

The component prices reported in Table 2 correspond to quotations obtained on August 2025 and are used exclusively for comparative cost evaluation within the proposed design methodology [24].

D. Output Filter Design

LCL filters are adopted at both AC terminals of the converter to minimize the high-frequency harmonic content injected into the interconnected microgrids. For stable operation,

the LCL filter is designed according to the methodology proposed in [25], which defines the resonance frequency and the associated design constraints to ensure stable operation without active damping. Additionally, the filter capacitor is limited by the maximum allowable reactive power, typically below 5% of the rated power. The capacitor C_f is constrained by the reactive power limit, such as,

$$C_f \leq \frac{0.05 \cdot P_n}{2\pi f_g V_g^2}. \tag{1}$$

The converter-side inductor L_1 is determined according to the switching frequency, DC-link voltage, and allowable current ripple, according to,

$$L_1 = \frac{V_{dc}}{6 \cdot f_{sw} \cdot \Delta i \cdot (N-1)}, \tag{2}$$

where Δi is the current ripple and N is the number of voltage levels of the converter. The grid-side inductor L_2 is defined as a fraction of L_1, as given by:

$$L_2 = a \cdot L_1, \tag{3}$$

where a is the inductance ratio between the grid-side and converter-side inductors. This parameter is obtained from (4), which relates the attenuation of the current ripple in L_2 with respect to the current ripple in L_1,

$$a = \frac{\left(\frac{\Delta I_{L1}}{\Delta I_{L2}} - 1\right)}{|1 - 4\pi^2 f_{sw}^2 L_1 C_f|}, \tag{4}$$

where ΔI_{L1} and ΔI_{L2} are the peak-to-peak current ripples in the converter-side and grid-side inductors, respectively. In practical applications, values of a typically range from 0.1 to 0.5, providing a suitable compromise between harmonic attenuation and filter size. In this work, a value of $a = 0.5$ is adopted for all designs. As the component values depend on the chosen topology and switching frequency, each configuration requires a distinct filter design. Consequently, a dedicated filter design is carried out for every case study. The design of EMI and common-mode filters is not addressed in this study.

E. DC-link Bus

The proposed design methodology assumes balanced three-phase operation and neglects low-order harmonics. Under these assumptions, the DC-link does not exhibit second-order power oscillations. Although voltage unbalance or unequal power transfer may introduce low-frequency power oscillations in practical applications, these operating conditions are beyond the scope of this work. Therefore, the DC-link capacitor is sized considering the switching-frequency and allowed voltage ripple, which directly influences converter performance, harmonic distortion, and power quality. The minimum required capacitance C_{dc} is determined according to (5), following the methodology presented in [26].

$$C_{dc} \geq \frac{S_n}{(V_{dc}\Delta V_{dc} \pm \Delta V_{dc}^2) f_{sw}}. \tag{5}$$

From a DC-link voltage ripple perspective, all investigated topologies are comparable in terms of the required equivalent capacitance, since it depends only on the converter rated power, allowable voltage ripple, DC-link voltage, and switching frequency. However, differences in DC-link voltage levels (900 V and 2 kV) lead to variations in the required equivalent capacitance. Moreover, the arrangement of the DC-link capacitors depends on the converter topology. The 2L and FC converters employ a single capacitor bank, whereas the 3L-NPC, 3L-T-type, and 5L-ANPC topologies require two capacitors connected in series to split the DC-link voltage. In contrast, the 5L-NPC topology employs four series-connected capacitors, increasing the required capacitance of each individual capacitor while maintaining the same equivalent DC-link capacitance. Table 3 summarizes the capacitance calculations considering the converter topology, switching frequency, DC-link voltage, and component prices, using the Mouser Inc. catalog as a benchmark. The calculated equivalent and individual capacitances correspond to the capacitors denoted as C_{dc} and C_{dcx} in Fig. 4 for the respective converter structures.

TABLE 3. DC-link capacitor bank for evaluated converters.

Capacitance for 2L and FC topologies						
Voltage [V]	Fsw [Hz]	ΔV_{dc}	C_{eq} [μF]	C_{cap} [μF]	Model	Price [US$]
900	2500	2%	24207	24207	B25620B1108K203	187.12
2000	2500	2%	4902	4902	B25690C2367K803	219.82
900	5000	2%	12103	12103	B25620B1108K203	187.12
2000	5000	2%	2451	2451	B25690C2367K803	219.82
900	10000	2%	6052	6052	B25620B1108K203	187.12
2000	10000	2%	1225	1225	B25690C2367K803	219.82
Capacitance for NPC and T-type topologies						
Voltage [V]	Fsw [Hz]	ΔV_{dc}	C_{eq} [μF]	C_{cap} [μF]	Model	Price [US$]
900	2500	2%	24207	48414	C44UHGT7210M87K	195.00
2000	2500	2%	4902	9804	B25620B1108K203	187.12
900	5000	2%	12103	24206	C44UHGT7210M87K	195.00
2000	5000	2%	2451	4902	B25620B1108K203	187.12
900	10000	2%	6052	12104	C44UHGT7210M87K	195.00
2000	10000	2%	1225	2450	B25620B1108K203	187.12
Capacitance for 5L ANPC topology						
Voltage [V]	Fsw [Hz]	ΔV_{dc}	C_{eq} [μF]	C_{cap} [μF]	Model	Price [US$]
2000	2500	2%	4902	9804	B25620B1108K203	187.12
2000	5000	2%	2451	4902	B25620B1108K203	187.12
2000	10000	2%	1225	2450	B25620B1108K203	187.12
Capacitance for 5L NPC topology						
Voltage [V]	Fsw [Hz]	ΔV_{dc}	C_{eq} [μF]	C_{cap} [μF]	Model	Price [US$]
2000	2500	2%	4902	19608	B25620B1108K203	187.12
2000	5000	2%	2451	9804	B25620B1108K203	187.12
2000	10000	2%	1225	4900	B25620B1108K203	187.12

F. Flying Capacitor - 3L FC Topology

The 3L-FC topology requires an additional flying capacitor (C_{fc3}) in each converter leg besides the DC-link capacitor [27]. The minimum required capacitance is determined from the allowable voltage ripple across the flying capacitor and is given by:

$$C_{fc3} = \frac{2 i_{cap}}{f_{sw}\, \Delta V_{cf3}}, \tag{6}$$

where i_{cap} is the capacitor RMS current, and ΔV_{cf3} is the allowable voltage ripple of the flying capacitor. Applying (6) to DC-link voltages of 900 V and 2 kV, assuming an allowable flying-capacitor voltage ripple of 10%, yields the capacitance values presented in Table 4 for each switching frequency and DC-link voltage.

G. Flying Capacitor - 5L APCN Topology

For the 5L-ANPC topology, the floating capacitor C_{fc5} is sized according to the methodology proposed in [28]. The minimum required capacitance is given by:

$$C_{fc5} = \frac{I_m}{8\Delta V_{fc5} f_{sw}} \frac{V_{dc}}{V_m}, \tag{7}$$

where I_m is the peak phase current, V_m is the peak phase output voltage, and ΔV_{fc} is the allowable voltage ripple (10% in this case study). The selected capacitor must satisfy the minimum capacitance requirement, withstand a voltage rating higher than $V_{dc}/4$, and support the expected ripple current. Multiple capacitors connected in parallel may be required to meet the current rating specification. Table 4 presents the capacitor sizing results for each operating condition. In some cases, the required capacitance is lower than that of the selected capacitor bank, since the capacitor bank is sized by its RMS current rating rather than by the capacitance requirement.

TABLE 4. Calculation of capacitors for the flying capacitor topology.

3L - Flying Capacitors						
Voltage [V]	**Fsw [Hz]**	**Model**	C_{fcx} [μF]	**Qty.**	**Eq. Cap. [μF]**	**Price**
900	2500	B25647A1887K003	6755	8	7040	555.94
2000	2500	B25645A2367K003	960	3	1050	447.68
900	5000	B25647A1887K003	3378	5	4400	555.94
2000	5000	B25645A2367K003	480	2	700	447.68
900	10000	B25647A1887K003	1689	5	4400	555.94
2000	10000	B25645A2367K003	240	2	700	447.68
5L - Flying Capacitors						
2000	2500	B25645A2367K003	201	2	700	447.68
2000	5000	B25645A2367K003	100	2	700	447.68
2000	10000	B25645A2367K003	50	2	700	447.68

III. PROPOSED DESIGN METHODOLOGY

A. Design Workflow

Fig. 5 summarizes the proposed multiobjective hardware design methodology. Starting from the application specifications and design assumptions, the algorithm generates feasible converter configurations by selecting the converter topology, semiconductor technology, DC-link voltage, switching frequency, and passive components. For each feasible solution, electrical, thermal, volumetric, and economic models are evaluated to estimate the converter efficiency, power density, and cost, excluding the identical LFT. Finally, all feasible designs are compared through Pareto optimization to identify the best trade-offs among the figures of merit.

To identify a representative optimal design from the Pareto-optimal solutions, a normalized multiobjective score was calculated considering the figures of merit. Each metric was normalized using the 5th and 95th percentiles of the evaluated solutions, reducing the influence of extreme values. The normalized metrics are then combined using a weighted average, with weights of 25% for efficiency, 25% for power density, and 50% for cost. The solution achieving the highest score was selected as the representative optimal design.

B. Efficiency

The losses of the main converter components, including semiconductors, inductors, and capacitors, are considered in the efficiency (η) evaluation. Semiconductor losses are divided into conduction and switching losses, where conduction losses depend on the device current, voltage drop, temperature, and operating conditions, while switching losses are obtained from the switching energy characteristics provided in the device datasheets. The semiconductor loss estimation follows the methodology presented in [20], using the PSIM thermal module based on manufacturer data.

Inductor losses are evaluated considering copper and core losses. Copper losses account for the winding resistance and the frequency-dependent effects, such as skin and proximity effects, while core losses are estimated according to the magnetic material characteristics and Steinmetz-based models, following the methodology described in [23]. Capacitor losses are analyzed for DC-link, flying capacitors, and LCL filter capacitors, considering aluminum electrolytic and film capacitor technologies. The losses are calculated based on the capacitor RMS current spectrum, equivalent series resistance (ESR), operating temperature, and leakage current, according to the approach presented in [20]. These models provide the basis for estimating the total converter losses and comparing different component technologies and converter configurations.

C. Power Density

The volume estimation of the main converter components is performed considering inductors, capacitors, and heatsinks. The inductor volume is estimated using an analytical approach based on the magnetic characteristics of the core and the operating conditions, considering parameters such as flux density, permeability, inductance, and current. This methodology provides a physically consistent approximation of the magnetic component volume without requiring a detailed geometric model, making it suitable for preliminary design stages and multi-objective optimization studies [17]. The estimated volume also enables further evaluations of power density (ρ) of the converter.

The capacitor volume is determined based on the physical dimensions provided in manufacturer datasheets, considering the required capacitance, current ripple capability, and thermal limitations. For the heatsink volume estimation, the Cooling System Performance Index (CSPI) approach proposed in [29] is adopted, relating the dissipated semiconductor losses to the required cooling volume and allowable temperature rise. This methodology allows a consistent

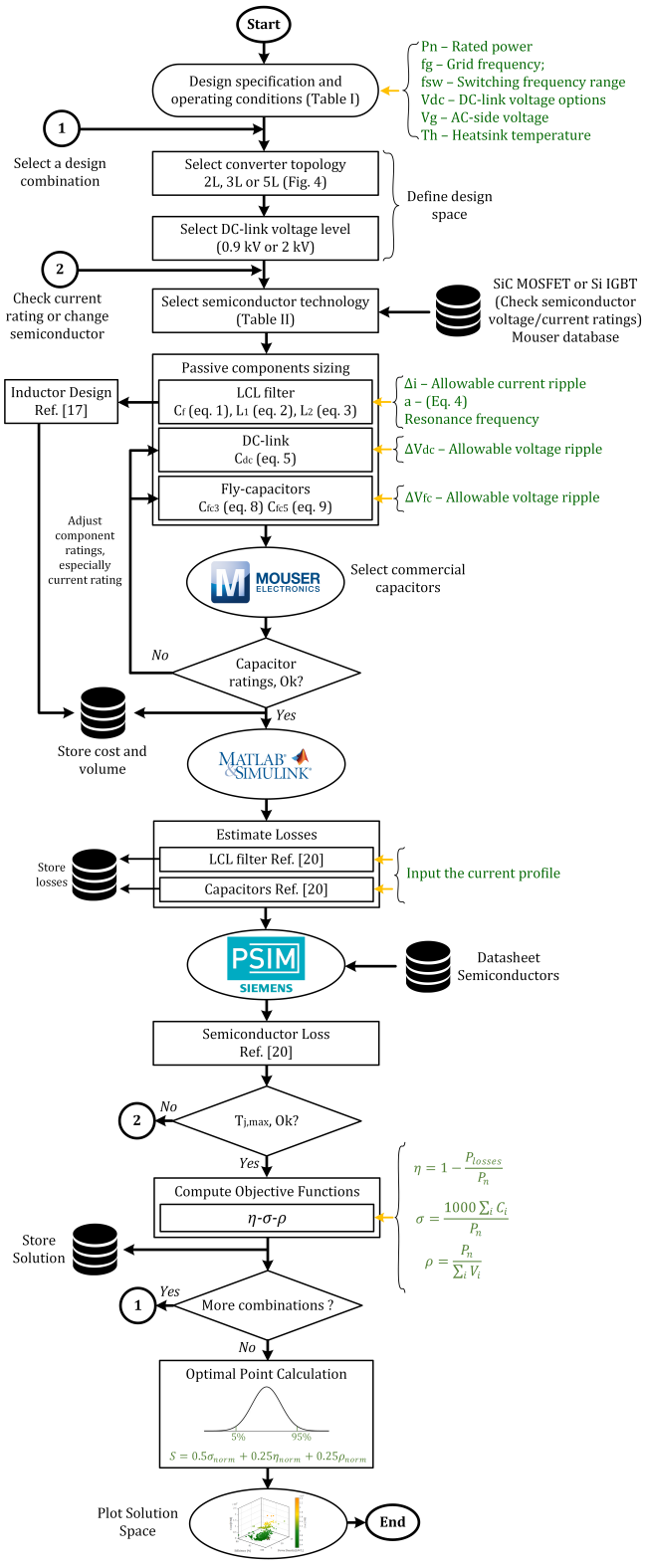


FIGURE 5. Flowchart of the proposed multiobjective hardware design methodology.

estimation of the thermal management requirements and supports the comparison of different converter configurations in terms of power density and component integration.

D. Specific Cost

The specific cost (σ) is defined to evaluate the economic impact of the converter components by normalizing the total component cost according to the converter rated power. The prices of semiconductors and capacitors were obtained from commercially available components listed by Mouser. Since the cost of inductors and heatsinks is closely related to their physical dimensions and material requirements, their costs were estimated based on the calculated component volumes, following the approach commonly adopted in multiobjective converter design studies [30]. The specific cost metric allows a direct comparison between different converter configurations by expressing the total investment in terms of US$/kW. Since the inductor cost is strongly related to its physical size and magnetic material requirements, its cost is estimated based on the calculated inductor volume, establishing a direct relationship between the component dimensions and its economic impact. The cost model considers both component-specific catalog prices and estimated costs based on production volume, depending on the component, which may result in different levels of accuracy across the evaluated designs. This aspect is considered as a limitation of the proposed cost estimation methodology.

It should be noted that the estimated component costs may vary depending on the manufacturer, purchase quantity, supplier, and prevailing market conditions. Therefore, the cost values presented in this work should be interpreted primarily as comparative indicators rather than absolute costs. The economic analysis aims to provide a consistent basis for assessing the relative cost trends among the evaluated converter configurations under the assumptions adopted in this study.

IV. RESULTS

The simulation setup is defined to ensure a fair comparison among all converter topologies by selecting semiconductor devices according to their voltage and current ratings, as shown in Table 5. Each topology is implemented using commercially available switches whose voltage blocking capability matches the DC-link voltage level, while the current rating is chosen based on the nominal operating current. Two-level converters require devices rated for the full DC-link voltage, whereas three-level and five-level structures distribute the voltage stress among multiple devices, enabling the use of lower-voltage semiconductors

A. Low voltage DC-Link

Fig. 6 presents the trade-offs among efficiency, cost, and power density for the LV DC-link designs operating at 2.5, 5, and 10 kHz. Although the most efficient solutions, reaching approximately 97.3% as shown in Fig. 6(A), are generally associated with costs exceeding 100 US$/kW, the efficiency gain obtained by increasing the investment is limited. The selected design (2L-SiC) achieves nearly 96% efficiency at a cost of only 27.1 US$/kW, representing a reduction of

CC BY

TABLE 5. Power semiconductor devices used in each converter topology and voltage level.

Device	NPC-LV	NPC-MV	2L-LV	2L-MV	FC-LV	FC-MV	T-LV	T-MV	5L-NPC	5L-ANPC
FZ2400R17HE4PB9			×					×		×
2x(MSCSM170AM029CT6LIAG)			×				×			×
DIM1200FSM17-A000		×		×		×	×			
FF2600UXTR33T2M1				×				×		
MSCSM170AM029CT6LIAG		×		×		×	×			
FZ800R33KF2C				×				×		
FF1800R12IE5	×				×		×		×	
4xBSM600D12P3G001	×				×		×		×	
DZ3600S17K3-B2	×									
DFM1200NXM33-F 000		×							×	

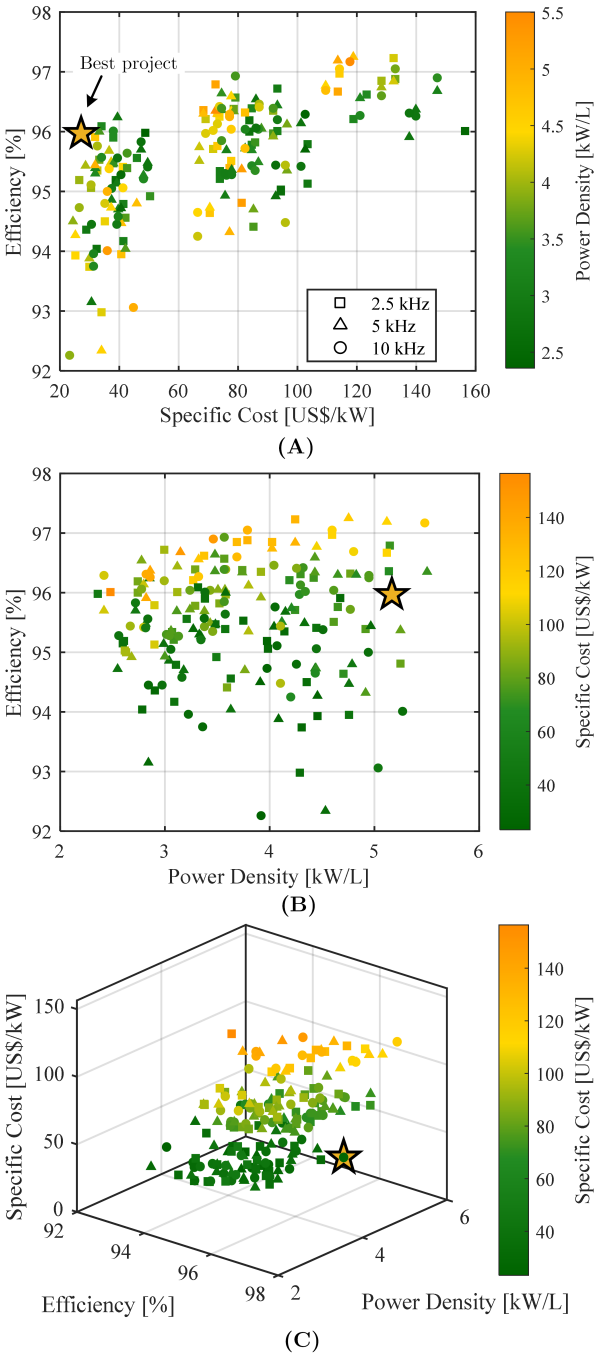


FIGURE 6. Performance comparison of the optimized LV DC-link converter designs at 2.5, 5, and 10 kHz. (a) Efficiency as a function of cost. (b) Efficiency as a function of Power density. (c) Three-dimensional representation of efficiency, cost, and power density. The selected optimal design is highlighted by the star marker.

about 75% compared to the highest-efficiency alternatives. Moreover, converters operating at different switching frequencies exhibit a significant overlap in terms of efficiency and cost, indicating that the switching frequency alone is not the dominant factor governing these metrics.

The influence of switching frequency becomes more evident when power density is considered, as illustrated in Fig. 6(B). The designs operating at 10 kHz attain the highest volumetric performances, reaching values up to 5.5 kW/L.In comparison, the maximum power density achieved at 5 kHz is 4.78 kW/L, while the 2.5 kHz designs are limited to 3.49 kW/L. The selected project belongs to the 10 kHz group and combines a power density of approximately 5.16 kW/L with a competitive efficiency level and one of the lowest implementation costs among all evaluated solutions. The results indicate that employing SiC devices in simpler (2L) topologies is an effective approach to improve efficiency and power density with a moderate increase in cost. In contrast, although multilevel converters with a larger number of semiconductor devices can further enhance performance, their implementation cost rises significantly due to the higher number of SiC modules required. Fig. 6(C) complements the two-dimensional analyses by providing a three-dimensional visualization of efficiency, cost, and power density, with the selected optimal design highlighted by the star marker.

Table 6 summarizes the performance of representative LV converter designs employing identical rectifier and inverter stages for switching frequencies of 2.5, 5, and 10 kHz. The results indicate that the use of SiC devices in the 3L-FC topology provides the highest efficiencies at all evaluated frequencies. However, these efficiency gains are achieved at the expense of substantially higher implementation costs, exceeding 117 US$/kW in all cases. Regarding power density, the 3L-FC topology with IGBT devices achieves the highest values at 2.5 and 5 kHz, reaching 3.49 and 5.03 kW/L, respectively, whereas the 3L-FC topology employing SiC devices at 10 kHz attains the overall maximum power density of 5.48 kW/L. It is also noteworthy that the 2L converter employing SiC devices at 10 kHz achieves a competitive power density of 5.16 kW/L while requiring a considerably lower implementation cost of only 27.1 US$/kW. Overall, the results reinforce the trade-off between efficiency, power density, and cost, indicating that the most efficient and compact solutions are not necessarily the most economically attractive.

TABLE 6. Performance comparison of representative LV converter designs employing identical rectifier and inverter stages for switching frequencies of 2.5, 5, and 10 kHz. The best performance achieved for each metric is highlighted.

Topology	Semiconductor	2.5 kHz			5 kHz			10 kHz		
		η (%)	PD (kW/L)	S. Cost (US$/kW)	η (%)	PD (kW/L)	S. Cost (US$/kW)	η (%)	PD (kW/L)	S. Cost (US$/kW)
2L	IGBT	94.36	2.90	28.9	94.50	3.91	24.4	92.26	3.92	23.3
	SiC	94.04	2.78	32.4	95.43	4.04	28.6	95.97	5.16	27.1
3L NPC	IGBT	95.56	3.21	45.9	95.68	4.15	36.6	95.38	4.51	36.6
	SiC	95.72	3.27	118.9	96.13	4.45	109.5	95.76	4.8	109.5
3L FC	IGBT	94.92	**3.49**	50.4	94.80	**5.03**	45.9	93.06	2.20	44.8
	SiC	**96.62**	3.37	123.3	**97.25**	4.75	118.8	**97.17**	**5.48**	117.7
3L T-type	IGBT	95.98	2.36	48.8	96.24	2.85	39.4	95.56	2.84	39.4
	SiC	96.01	2.48	156.4	96.68	3.15	147.1	96.90	3.46	147.1

B. Medium voltage DC-Link

Fig. 7 presents the trade-offs among efficiency, cost, and power density for the MV DC-link designs operating at 2.5, 5, and 10 kHz.

In contrast to the LV case, most solutions achieve efficiencies above 97%, regardless of the switching frequency, indicating that increasing the switching frequency does not significantly penalize the conversion efficiency. Nevertheless, designs operating at 10 kHz are predominantly concentrated in the high-efficiency region, whereas the 2.5 kHz solutions exhibit a larger dispersion and include the lowest-performing designs, with efficiencies below 90%. Although the highest efficiencies, approaching 99.1%, are associated with implementation costs exceeding 200 US$/kW, the selected design attains approximately 98% efficiency at a cost close to 38 US$/kW, corresponding to less than one-fifth of the investment required by the most expensive alternatives.

The influence of switching frequency becomes more pronounced when power density is considered, as illustrated in Fig. 7(B). While most 2.5 kHz designs remain below 6 kW/L, the solutions operating at 5 kHz achieve power densities close to 11 kW/L, and the 10 kHz designs reach values as high as 14.6 kW/L. The selected project belongs to the 10 kHz group and combines a power density of approximately 7.25 kW/L with a high efficiency level and a low implementation cost, positioning it near the upper performance boundary. Therefore, the optimization procedure favors a design that exploits the volumetric advantages of higher switching frequencies while avoiding the substantial cost increase associated with marginal improvements in efficiency. Fig. 7(C) complements the two-dimensional analyses by providing a three-dimensional visualization of efficiency, cost, and power density, with the selected optimal design highlighted by the star marker.

The results presented in Table 7 reveal a clear influence of switching frequency, converter topology, and semiconductor technology on the overall performance of the evaluated designs. For all topologies, increasing the switching frequency generally improves power density, particularly for multilevel converters employing SiC devices. The two-level converter exhibits the lowest efficiencies and power densities, especially when implemented with IGBT modules at

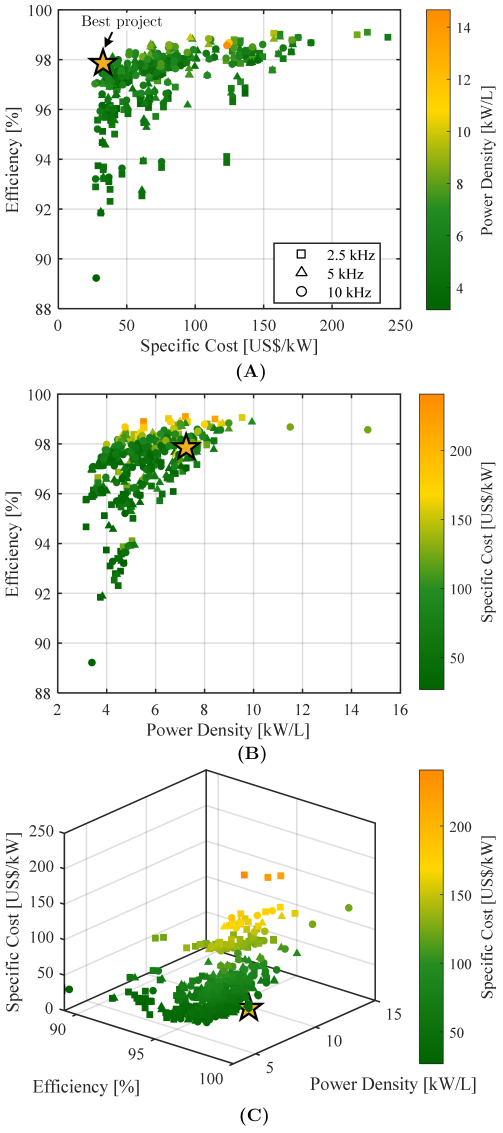


FIGURE 7. Performance comparison of the optimized MV DC-link converter designs at 2.5, 5, and 10 kHz. (a) Efficiency as a function of cost. (b) Efficiency as a function of Power density. (c) Three-dimensional representation of efficiency, cost, and power density. The selected optimal design is highlighted by the star marker.

10 kHz, where the efficiency decreases to 89.2%. In contrast, multilevel topologies maintain efficiencies above 97% over the entire frequency range, demonstrating their suitability for high-power applications. The 5L NPC topology employing SiC devices achieves the highest efficiencies, reaching 99.10% at 2.5 and 5 kHz, while also providing the high power density. However, these performance gains are accompanied by implementation costs exceeding 218 US$/kW, substantially higher than those of alternative solutions. The 3L NPC converter based on SiC/IGBT devices represents a more balanced compromise, attaining 97.86% efficiency and 7.25 kW/L power density at 10 kHz with a cost of 38.2 US$/kW. Overall, the results indicate that increasing the switching frequency and adopting SiC devices enhance volumetric performance with only a marginal impact on efficiency, whereas higher-level topologies provide superior efficiency at the expense of increased implementation cost.

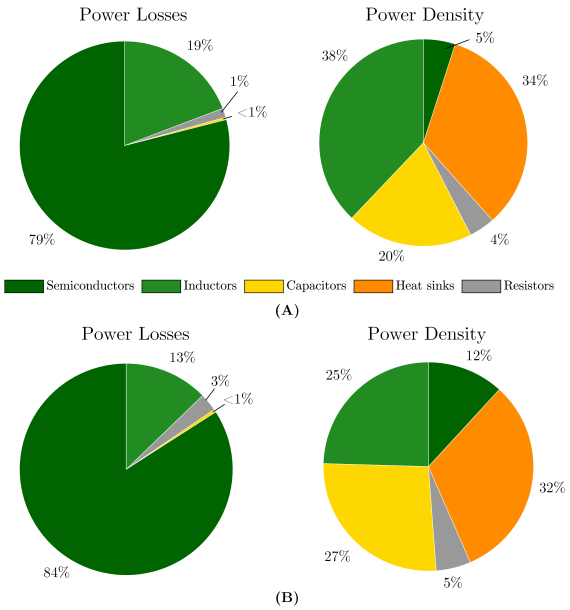


FIGURE 8. Per-unit losses and power density of the optimized converter designs. (A) LV converter; (B) MV converter.

C. Comparison of Medium and Low Voltage DC-Link

Table 8 compares the optimal converter designs selected for the LV and MV DC-link applications.

The comparison highlights the distinct design requirements of the LV and MV DC-link applications. The selected LV solution is based on a 2L converter employing SiC devices in both conversion stages, achieving a balanced combination of high efficiency (95.97%), high power density (5.16 kW/L), and low implementation cost (27.15 US$/kW). In contrast, the optimal MV design adopts a 3L NPC topology with a hybrid semiconductor configuration, combining SiC devices in one conversion stage and IGBT devices in the other. This solution achieves higher efficiency (97.86%) and power density (7.25 kW/L) while maintaining a relatively low implementation cost (38.2 US$/kW). These results indicate that, as the operating voltage increases, multilevel topologies combined with a hybrid semiconductor implementation provide a more favorable trade-off between efficiency, power density, and cost than conventional two-level solutions.

Fig. 8(A) shows the per-unit losses and volume breakdown by component for the LV design, while Fig. 8(B) provides the corresponding breakdown for the MV design. When comparing LV and MV converters, it is observed that in low-voltage applications the inductor contributes a higher percentage of the total losses, mainly due to the increased current levels. In contrast, the losses in the remaining components remain comparable between both voltage levels. Regarding power density, the medium-voltage design exhibits a reduction in inductor volume, while the capacitor volume increases, along with the semiconductor volume, as a consequence of the transition from two-level (2L) to three-level (3L) topologies. Meanwhile, the heat sink volume remains approximately constant in relative terms across both voltage classes.

V. CONCLUSION

The use of the optimal design tool proved essential for the technical and economic evaluation of different converter topologies. By simultaneously considering the criteria of efficiency, power density, and cost, it is possible to identify balanced, high-performance solutions, many of which would not have been evident if only one of the criteria had been analyzed in isolation. The results show that the optimal solution strongly depends on the operating voltage level, with distinct trade-offs between LV and MV applications.

For LV systems, the best performance is achieved with a 2L topology using SiC devices at high switching frequency, providing a balanced compromise between cost and performance. For MV systems, multilevel structures combined with a hybrid SiC/IGBT implementation become more advantageous, enabling higher efficiency and power density at acceptable cost levels. Overall, the study confirms that SiC devices and increased switching frequency improve power density, while topology selection is the dominant factor for efficiency at higher voltage levels. The proposed framework effectively identifies balanced solutions across competing design objectives.

From a practical design perspective, the proposed methodology provides a systematic basis for selecting between LV and MV DC-link architectures in high-power converter applications. By evaluating efficiency, cost, and power density under consistent design conditions, the framework allows designers to identify the trade-offs associated with different voltage levels, converter topologies, semiconductor technologies, and switching frequencies. Therefore, rather than indicating a universally superior architecture, the proposed approach can be used as a preliminary design tool

TABLE 7. Complete performance comparison of converter topologies and semiconductor technologies for switching frequencies of 2.5, 5, and 10 kHz. The best performance achieved for each metric is highlighted.

Topology	Semiconductor	2.5 kHz			5 kHz			10 kHz		
		η (%)	PD (kW/L)	S. Cost (US$/kW)	η (%)	PD (kW/L)	S. Cost (US$/kW)	η (%)	PD (kW/L)	S. Cost (US$/kW)
2L	IGBT	94.67	3.16	32.1	93.74	3.98	29.0	89.23	3.40	27.7
	SiC	97.11	3.65	42.3	98.03	5.68	39.2	97.84	7.13	37.9
3L NPC	IGBT	97.45	4.27	32.0	97.07	5.50	28.3	97.03	7.24	26.8
	SiC	97.53	4.19	43.8	97.96	6.05	40.0	97.87	7.25	38.5
3L FC	IGBT	96.94	3.39	38.8	96.11	4.00	35.7	94.57	4.26	34.4
	SiC	97.09	3.44	50.5	97.57	4.66	47.4	97.31	5.45	46.1
3L T-type	IGBT	97.42	4.41	53.1	97.29	6.10	49.4	95.99	6.27	47.9
	SiC	98.35	4.81	101.7	98.82	7.52	98.0	98.88	9.93	96.5
5L NPC	IGBT	98.12	5.29	72.8	98.12	6.31	65.3	98.01	7.14	65.3
	SiC	**99.10**	5.51	225.8	**99.10**	7.22	218.3	**99.00**	8.42	218.3
5L ANPC	IGBT	97.38	4.45	96.0	96.18	5.76	94.5	96.18	6.07	94.5
	SiC	98.68	**7.72**	124.6	98.57	**11.50**	123.1	98.57	**14.67**	123.1

TABLE 8. Comparison between the selected optimal low- and medium-voltage converter designs.

Parameter	LV design	MV design
Topology	2L	3L NPC
Semiconductor	SiC	SiC/IGBT
Switching frequency (kHz)	10	10
Efficiency (%)	95.97	97.86
Power density (kW/L)	5.16	7.25
S. Cost (US$/kW)	27.15	38.2

to identify the most suitable LV or MV configuration according to the specific requirements and priorities of the application. The final design decision should, however, also account for application-dependent aspects such as insulation requirements, thermal management, load profile, and system integration.

ACKNOWLEDGMENT

This work was carried out with the support of the Graduate Program in Electrical Engineering of Universidade Federal de Minas Gerais (PPGEE-UFMG) and the Coordination for the Improvement of Higher Education Personnel - Brazil (CAPES) - Financing Code 001, through the Academic Excellence Program (PROEX) of the National Council for Scientific and Technological Development (CNPQ).

AUTHOR'S CONTRIBUTIONS

M.O.SCHNEIDER: Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **G.V.BARBOSA:** Data Curation, Software, Visualization, Writing – Review & Editing. **G.A.FOGLI:** Conceptualization, Methodology, Project Administration, Supervision, Validation, Writing – Review & Editing. **T.R.OLIVEIRA:** Conceptualization, Methodology, Supervision, Validation, Writing – Review & Editing. **L.M.F.MORAIS:** Conceptualization, Methodology, Supervision, Validation, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

REFERENCES

[1] J. A. Guzmán-Henao, R. I. Bolaños, O. D. Montoya, L. F. Grisales-Noreña, H. R. Chamorro, "On Integrating and Operating Distributed Energy Resources in Distribution Networks: A Review of Current Solution Methods, Challenges, and Opportunities", *IEEE Access*, vol. 12, pp. 55111–55133, 2024, doi:10.1109/ACCESS.2024.3387400.

[2] P. Tenti, T. Caldognetto, S. Buso, D. I. Brandao, "Control of Utility Interfaces in Low-Voltage Microgrids", *Eletrônica de Potência*, vol. 20, no. 4, pp. 373–382, Nov. 2015, doi:10.18618/REP.2015.4.2556.

[3] D. Saha, N. Bazmohammadi, J. C. Vasquez, J. M. Guerrero, "Multiple Microgrids: A Review of Architectures and Operation and Control Strategies", *Energies*, vol. 16, no. 2, p. 600, 2023, doi:10.3390/en16020600.

[4] R. P. Kandula, A. Prasai, H. Chen, R. Mayor, F. Lambert, T. Heidel, C. Schauder, D. Divan, "Design considerations and experimental results for a 12.47-kV 3-phase 1 MVA power router", *in 2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5000–5007, 2015, doi:10.1109/ECCE.2015.7310365.

[5] B. Tamimi, C. A. Cañizares, "Modeling and Application of Hybrid Power Flow Controller in Distribution Systems", *IEEE Transactions on Power Delivery*, vol. 33, no. 6, pp. 2673–2682, 2018, doi:10.1109/TPWRD.2018.2862153.

[6] V. S. Fiuza, T. R. Oliveira, "Interlinking Converters for Hybrid AC/DC Microgrids: A Systematic Literature Review", *IEEE Access*, vol. 13, pp. 184775–184791, 2025, doi:10.1109/ACCESS.2025.3625440.

[7] M. R. Islam, Y. Guo, J. Zhu, *Power Converters for Medium Voltage Networks*, Green Energy and Technology, Springer, Berlin, Heidelberg, 2014, doi:10.1007/978-3-662-44529-7.

[8] A. Lesnicar, R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range", *in 2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, pp. 6 pp. Vol.3–, 2003, doi:10.1109/PTC.2003.1304403.

[9] A. Christe, D. Dujic, "Galvanically isolated modular converter", *IET Power Electronics*, vol. 9, no. 12, pp. 2318–2328, 2016, doi:10.1049/iet-pel.2015.0747.

[10] J. E. Huber, J. W. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts", *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 19–28, set. 2016, doi:10.1109/MIE.2016.2588878.

[11] Y. Kado, D. Shichijo, K. Wada, K. Iwatsuki, "Multiport power router and its impact on future smart grids", *Radio Science*, vol. 51, no. 7, pp. 1234–1246, 2016, doi:10.1002/2016RS006041.

[12] D. K. Mishra, M. J. Ghadi, L. Li, M. J. Hossain, J. Zhang, P. K. Ray, A. Mohanty, "A review on solid-state transformer: A breakthrough technology for future smart distribution grids", *International Journal of Electrical Power & Energy Systems*, vol. 133, p. 107255, 2021, doi:10.1016/j.ijepes.2021.107255.

[13] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, A. Weinstein, "Matrix converters: a technology review", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 276–288, 2002, doi:10.1109/41.993260.

[14] D. Varajao, R. E. Araujo, "Modulation Methods for Direct and Indirect Matrix Converters: A Review", *Electronics*, vol. 10, no. 7, p. 812, 2021, doi:10.3390/electronics10070812.

[15] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galván, R. C. P. Guisado, M. A. M. Prats, J. I. León, N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey", *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002–1016, 2006, doi:10.1109/TIE.2006.878356.

[16] R. Teodorescu, M. Liserre, P. Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*, IEEE Press and John Wiley & Sons, 2011, doi:10.1002/9780470667057.

[17] M. O. Schneider, G. V. Barbosa, G. A. Fogli, T. R. de Oliveira, L. M. F. Morais, "Multicriteria Optimization of High-Power Converter Topologies: Efficiency, Cost, and Power Density Trade-Offs", *in 2025 Brazilian Power Electronics Conference (COBEP)*, pp. 01–08, 2025, doi:10.1109/COBEP66423.2025.11231517.

[18] M. Schneider, G. Barbosa, G. Fogli, T. Oliveira, S. Silva, "Comparison of 13.8 kV Grid-tied Converters Cost and Efficiency", *in Proceedings SBAI-SBSE 2025*, Aug. 2025, doi:10.29327/1842969.1-68.

[19] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, S. D. Round, "PWM Converter Power Density Barriers", *IEEJ Transactions on Industry Applications*, vol. 128, no. 4, pp. 468–480, 2008, doi:10.1541/ieejias.128.468.

[20] R. M. BURKART, *Advanced Modeling and Multi-Objective Optimization of Power Electronic Converter Systems*, Ph.D. thesis, ETH Zurich, https://www.research-collection.ethz.ch/handle/20.500.11850/155815, Aug. 2016, phd Thesis.

[21] R. Ding, Z. Dou, Y. Qi, W. Mei, G. Liu, "Analysis on characteristic of 3.3-kV full SiC device and railway traction converter design", *IET Power Electronics*, vol. 15, no. 10, pp. 978–988, 2022, doi:10.1049/pel2.12280.

[22] Y. Li, *et al.*, "A highly efficient power block with series connection of power SiC MOSFETs—design, characterization and assessment in MV converters", *IET Power Electronics*, 2022, doi:10.1049/pel2.12253.

[23] M. O. Schneider, T. R. De Oliveira, E. M. Vicente, "High Efficiency Single-Phase AC/DC Converter for DC Distribution Systems", *in 2023 15th IEEE International Conference on Industry Applications (INDUSCON)*, pp. 1402–1409, 2023, doi:10.1109/INDUSCON58041.2023.10374725.

[24] Mouser Electronics, "Mouser Electronics: Electronic Components Distributor", Component prices accessed in August 2025, 2025, URL: https://www.mouser.com/.

[25] M. Liserre, F. Blaabjerg, S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier", *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281–1291, 2005, doi:10.1109/TIA.2005.853373.

[26] R. Lai, F. Wang, R. Burgos, Y. Pei, D. Boroyevich, B. Wang, T. A. Lipo, V. D. Immanuel, K. J. Karimi, "A Systematic Topology Evaluation Methodology for High-Density Three-Phase PWM AC-AC Converters", *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2665–2680, 2008, doi:10.1109/TPEL.2008.2005381.

[27] C. B. Barth, P. Assem, T. Foulkes, W. H. Chung, T. Modeer, Y. Lei, R. C. N. Pilawa-Podgurski, "Design and Control of a GaN-Based, 13-Level, Flying Capacitor Multilevel Inverter", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2179–2191, 2020, doi:10.1109/JESTPE.2019.2956166.

[28] Y. Kashihara, J. ichi Itoh, "Design Optimization of a Five-level Active NPC Inverter", *in IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–8, 2011.

[29] J. Biela, U. Badstuebner, J. W. Kolar, "Impact of Power Density Maximization on Efficiency of DC–DC Converter Systems", *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288–300, 2009, doi:10.1109/TPEL.2009.2006355.

[30] R. Burkart, J. W. Kolar, "Component Cost Models for Multi-Objective Optimizations of Switched-Mode Power Converters", *in Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2139–2146, IEEE, 2013, doi:10.1109/ECCE.2013.6646971.

BIOGRAPHIES

Magno O. Schneider received the B.Sc. degree in electrical engineering from the Federal University of São João del-Rei (UFSJ) in 2021 and the M.Sc. degree in electrical engineering from the Federal University of Minas Gerais (UFMG) in 2023, where he is currently pursuing the Ph.D. degree. He is also a member of the Power Electronics Research Group (GEP/UFMG). His research interests include multi-objective design of power converters and active power decoupling techniques.

Gustavo V. Barbosa received the B.Sc. degree in Control and Automation Engineering from the Federal University of Minas Gerais (UFMG) in 2025, graduating with the gold medal of his class. He is currently pursuing the M.Sc. degree in electrical engineering at UFMG and is a member of the Power Electronics Research Group (GEP/UFMG). His research interests include microgrids, with emphasis on control structures, state observers applied to microgrid systems, and communication architectures for microgrids.

Gabriel A. Fogli received the B.S. degree in electronics and telecommunication engineering from Pontifícia Universidade Católica of Minas Gerais, Brazil, in 2011, and the M.Sc. and Ph.D. degrees in electrical engineering from the Universidade Federal de Juiz de Fora, Brazil, in 2014 and 2018, respectively. Since 2019, he has been a Professor with the Universidade Federal de Minas Gerais, Brazil. His research interests include modeling and control of power electronic converters and distributed generation applications.

Thiago R. Oliveira received the Ph.D. degree in electrical engineering from the Federal University of Minas Gerais (UFMG) in 2016. He is currently an Assistant Professor with the Electronic Engineering Department, UFMG, and a member of the Power Electronics Research Group (GEP/UFMG). His research interests include power electronics application in hybrid AC/DC microgrids, distributed energy storage, uninterruptible power supply (UPS), and optimized design of power converters.

Lenin M. F. Morais received the bachelor's degree, the master's degree, and the doctor's degree, all in electrical engineering from the Federal University of Minas Gerais, Belo Horizonte, Brazil, in 2000, 2002, and 2007, respectively. He is currently a Full Professor with the Electronics Engineering Department, Federal University of Minas Gerais. He was a Postdoctoral Intern with the Laboratoire Plasma et Conversion d'Energie - LAPLACE, Université Toulouse III Paul Sabatier, Toulouse, France, and with the Institut de Recherche Technologique - IRT Saint Exupéry, Toulouse, France. He has experience in the field of electrical engineering, with emphasis on power electronics, industrial electronics, and electronic systems and controls. His research interests mainly include the following: projects of converters with high density of power/high performance, electronic reactors for high intensity discharge lamps, power LEDs, circuits for power factor correction, repetitive control, control based on passivity, PWM methods. IEEE Senior Member and member of the IEEE Power Electronics Society, and Member of SOBRAEP (Brazilian Power Electronics Society) since 2005.