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Self-Supported Transformerless Series Active Power Filter for Wide-Range Load Voltage Compensation

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ABSTRACT This paper investigates a three-phase transformerless series active power filter based on open-end connections. The studied system was designed to mitigate power quality issues, including voltage harmonics, as well as balanced and unbalanced voltage sags and swells. The topology operates with the fourth wire connected through an additional leg. The developed control strategy eliminates the need for phase jumps in the load voltage, operates independently of the load power factor, and does not require fixed DC sources at the DC-link, making it a simpler and more efficient solution when compared with conventional approaches. The system model, the pulse-width modulation (PWM) scheme, and the design of the controllers and passive components are presented, while the overall control methodology is discussed in detail. In addition, a comparative analysis among the considered topologies is carried out. Finally, simulation and experimental results are presented to validate the feasibility and effectiveness of the proposed system.

KEYWORDS Power Quality, Series Active Filter, Transformerless.

I. INTRODUCTION

In recent years, the expansion of nonlinear loads has intensified Power Quality (PQ) problems, making them a significant concern in modern electrical systems [1]–[3]. Among the main disturbances that affect PQ are harmonics, voltage sags, and voltage swells, which can compromise the operation of sensitive equipment [4]. Voltage harmonics consist of distortions in the sinusoidal waveform and may cause malfunction of protection devices as well as transformer overheating [5]. Voltage sags and swells, in turn, are short-duration disturbances characterized, respectively, by the reduction of the RMS voltage to values between 0.1 and 0.9 p.u. and by the increase to values between 1.1 and 1.8 p.u. [6]. These disturbances may lead to failures in automated and communication systems, resulting in significant economic losses [7].

In this context, several solutions based on power electronics have been developed to mitigate power quality problems. Dynamic Voltage Restorers (DVRs) and Series Active Power Filters (SAPFs) are devices capable of protecting sensitive loads from disturbances originating from the electrical grid [14], [15]. The DVR is connected in series between the grid and the load and operates by injecting a controlled compensating voltage which, when added to the grid voltage, restores the load voltage to a sinusoidal waveform at its nominal value and fundamental frequency, thereby protecting

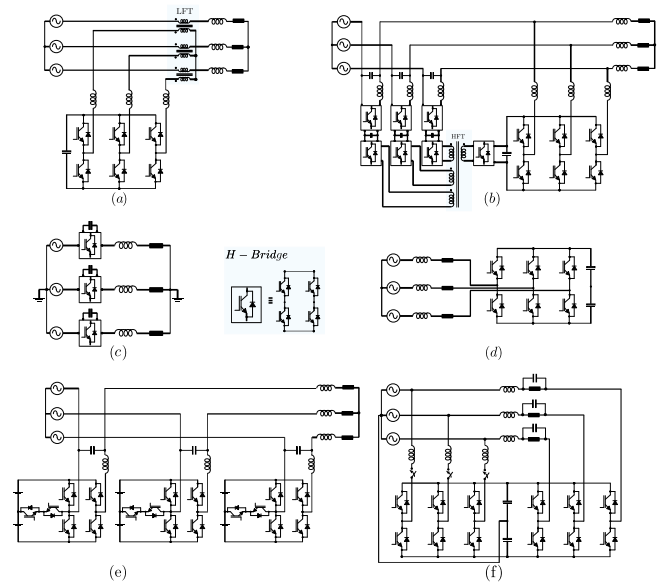


FIGURE 1. Existing series compensator topologies reported in the literature: (a) Conventional structure with line-frequency transformers (LFT) [8]. (b) Structure with high-frequency transformers (HFTs) [9]. (c) Transformerless SAPF with one H-bridge per phase (2L-SAPF) [10]. (d) Transformerless topology based on a three-phase converter [11]. (e) Transformerless five-level T-type DVR with independent DC sources [12]. (f) Transformerless SAPF with shunt and series converters (6L-SAPF) [13].

the load from grid disturbances [16]. Its typical topology consists of a Voltage Source Inverter (VSI), filter inductors, DC-link capacitors, a control system, low-frequency transformers for voltage injection, and an isolated DC source [6]. For this reason, the SAPF is generally a solution that does not require dedicated circuits to supply the DC-link, providing better cost-effectiveness while ensuring the supply of a regulated fundamental voltage to the load [17], [18]. In [8], the conventional SAPF topology (see Fig. 1(a)), is employed for power quality improvement. These devices are employed in several applications related to power quality improvement [19], [20]. The main drawback associated with their use is the presence of transformers operating at grid frequency, since they exhibit high manufacturing costs, which limits large-scale applications. In addition, these transformers are bulky and occupy considerable physical space, while also being susceptible to magnetic saturation, which may impair the compensation performance [7].

To address these issues, several topologies employing high-frequency transformers (HFTs) have been proposed in the literature [21]–[23]. In [9], a structure employing an isolated DC–DC converter with a high-frequency transformer, illustrated in Fig. 1(b), is proposed to provide galvanic isolation between the series converters without using bulky line-frequency injection transformers. However, the overall structure is relatively complex, comprising a three-phase shunt converter, an isolated DC–DC stage, three single-phase H-bridge series converters, multiple DC-link capacitors, and an HFT with one primary and three secondary windings. Considering the semiconductor devices employed in the complete structure, a total of 34 IGBTs is required. Furthermore, the compensation strategy adopted is based on in-phase compensation, which may result in a phase jump in the load voltage, making it undesirable for certain types of loads [24]. These topologies replace the injection transformer operating at line frequency with one operating at high frequency, resulting in a significant reduction in weight, volume, and costs [22], [25]. However, high-frequency transformers introduce challenges such as increased losses and design complexity due to parasitic effects and high-frequency phenomena [26], [27]. Motivated by this, transformerless topologies have been discussed in the literature [28], [29]. To reduce size, weight and costs, [10] proposed a transformerless SAPF using an H-bridge module per phase (2L-SAPF, see Fig. 1(c)). However, it does not compensate for unbalanced disturbances and requires a quadrature between voltage and current, causing phase jumps in the load voltage and making the voltage requirement and the possibility of compensation dependent on the load power factor. In [30], a control strategy applied to a DVR is developed to mitigate voltage sags and phase jumps; however, injection transformers are still used. In [11], a transformerless topology (see Fig. 1(d)) based on an open-end configuration and employing a three-phase series inverter compensates for unbalanced voltage sags with fewer com-

ponents compared with the topology shown in Fig. 1(c), but requires a higher DC-link voltage while still operating under quadrature control. In [12], a transformerless structure based on a T-type converter, illustrated in Fig. 1(e), is employed to increase the power density of the system. However, the topology requires multiple DC voltage sources, which are considered ideal in the study.

In this context, [13] proposed an open-end-based three-phase transformerless series active filter (6L-SAPF, see Fig. 1(f)), which was first introduced in [31] for applications as uninterruptible power supply. The investigated system is designed to compensate for harmonics, voltage sags, and swells, whether balanced or unbalanced, without relying on low-frequency transformers or additional isolated DC sources. Also, compared with the conventional counterpart, the control system proposed here operates independently of the load power factor and does not require phase jumps in the load voltage for proper operation. However, since the employed load is unbalanced, the neutral current is nonzero, requiring the system to operate in a four-wire configuration by using split capacitors in the DC-link to provide the fourth-wire connection. In this configuration, the neutral current may circulate through the DC-link capacitors and, depending on its magnitude, can lead to unbalanced capacitor voltages, increased voltage ripple, and the need for capacitors with higher capacitance and larger volume, consequently increasing the overall system cost [32], [33]. Furthermore, the topology presents three bidirectional switches connected in series with the interface inductors, which are responsible for disconnecting the shunt unit from the circuit during voltage swell conditions. As a consequence, the implementation cost may increase. In addition, since these switches are connected in series with the inductors, the abrupt interruption of the inductor currents during the switching process may generate high voltage spikes across the switches, potentially causing device failure. In such cases, an additional protection circuit would be required, increasing both the system cost and complexity.

This article presents a three-phase transformerless series active power filter based on an open-end connection, capable of operating independently of the load power factor and without requiring an isolated DC source at the DC-link (7L-SAPF, see Fig. 2). In addition, the proposed system avoids phase jumps in the load voltages. This work introduces several improvements over the system previously presented in [13]. In addition to the proposed topology, the PWM strategy, system modeling, controller design, passive component design, and control system are discussed in detail. A more comprehensive comparative analysis of the topologies is also included. Furthermore, simulation and experimental results are presented to validate the performance and feasibility of the proposed system. The main contributions and extensions of this work are summarized as follows:

- 1) A modified control strategy is proposed, eliminating the need for bidirectional switches.

TABLE 1. Comparison of the main features of series voltage compensators.

Article	[7]	[8]	[10]	[11]	[13]	[12]	[9]	Proposed
Number LFTs	0	3	0	0	0	0	0	0
Number HFTs	0	0	0	0	0	0	1	0
DC-link capacitors	2	1	3	2	2	0 [†]	4	1
Number of IGBTs	24	6	12	6	12	18	34	14
Balanced voltage sag	✓	✓	✓	✓	✓	✓	✓	✓
Unbalanced voltage sag	✓	✓	*	✓	**	✓	✓	✓
Balanced voltage swell	✓	✓	**	*	✓	✓	✓	✓
Unbalanced voltage swell	*	**	*	*	**	✓	✓	✓

**Capability reported in the work, although no results were presented. *Not reported in the work. [†]Six ideal DC voltage sources are considered instead of DC-link capacitors.

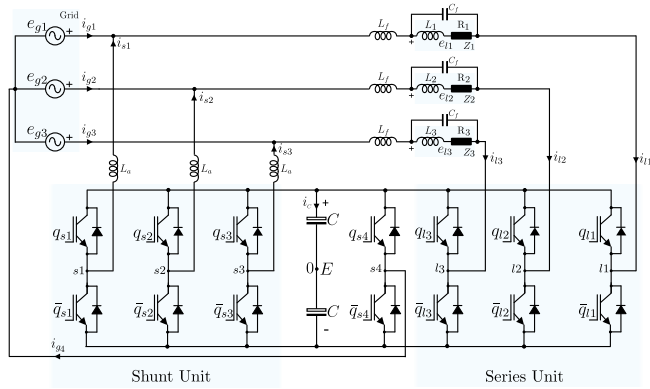


FIGURE 2. Proposed converter.

- 2) The fourth wire of the system is implemented through an additional converter leg, avoiding the issues associated with a split DC-link capacitor configuration. This arrangement reduces the DC-link voltage ripple, enables the use of a single DC-link capacitor, and provides an additional degree of freedom for voltage synthesis.
- 3) The comparative analysis is extended to include the 2L-SAPF and 6L-SAPF topologies. The comparison considers the total harmonic distortion (THD) of the load voltages, number of components, minimum DC-link voltage, DC-link stored energy and voltage ripple, and semiconductor power losses under different grid conditions.
- 4) Additional experimental results are presented to validate the proposed converter under different grid conditions.
- 5) A steady-state analysis is included, addressing the DC-link power flow and the design of the passive components.
- 6) The design procedure of the control system is presented in detail.

Table 1 presents a comparison between the proposed topology and selected structures reported in the literature.

The topology in [8] employs low-frequency transformers, whereas the solutions in [7], [10]–[13] are transformerless, and the topology in [9] employs a high-frequency transformer. Although some of these topologies reduce the number of semiconductor devices, their reported compensation capabilities are limited to a narrower range of grid disturbances. In this context, the proposed topology provides a favorable trade-off between the number of semiconductor devices and compensation capability. It is able to compensate for balanced and unbalanced voltage sags and swells without requiring transformers, while employing a single DC-link capacitor.

II. SYSTEM MODEL

Fig. 2 illustrates the proposed series active power filter, which operates with the fourth wire connected to an additional leg (q_{s4}). This configuration eliminates the need to connect the fourth wire to the DC-link, thereby avoiding issues associated with the circulation of zero-sequence components through the DC-link capacitors.

The load is linear and inductive, with an open-end connection, and is represented by Z_j per phase, consisting of a resistor R_j and an inductor L_j , where $j = \{1, 2, 3\}$. Its connection is implemented as illustrated in Fig. 2. Furthermore, the topology consists of a series unit, whose objective is to maintain the load voltage at its reference value, and a shunt unit, which is responsible for regulating the DC-link voltage. The system is supplied by a three-phase grid with voltages e_{gj} , while the load voltages are denoted by e_{lj} . The DC-link consists of a capacitor (C) with a total voltage E . In addition, the topology includes the coupling inductor of the shunt unit (L_a), which filters the high-frequency components generated by the converter switching, as well as the LC low-pass filters on the load side, consisting of the inductors L_f and capacitors C_f . The topology employs the switches $q_{sj} - \bar{q}_{sj}$ and $q_{lj} - \bar{q}_{lj}$.

Fig. 3 illustrates the equivalent circuit of the proposed topology. Based on this representation, the variables v_{lj0} , v_{sj0} , and v_{s40} represent the pole voltages of the series unit, the shunt unit, and the fourth leg, respectively. The

voltages generated by the shunt unit (v_{shj}) and the series unit (v_{sej}), as well as the corresponding pole voltages, can be defined. The currents i_{gj} , i_{lj} , and i_{sj} correspond to the

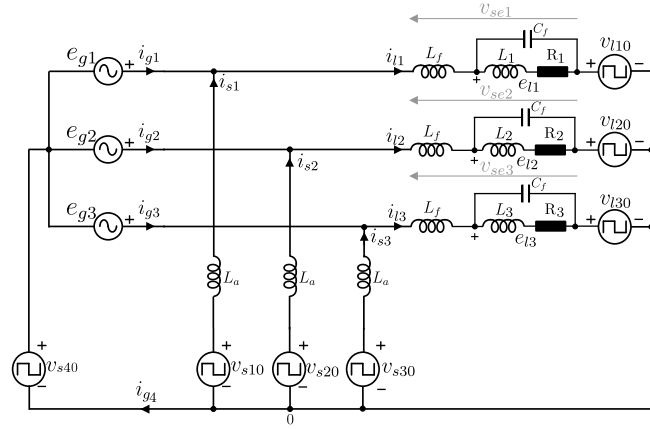


FIGURE 3. Equivalent circuit

currents flowing through the grid, the load, and the shunt unit, respectively. The current i_{g4} corresponds to the current flowing through the fourth wire. The DC-link current i_c is determined by the switching states of q_{sj} and q_{lj} , and depends on the shunt-unit currents (i_{sj}) and the load currents (i_{lj}), in addition to depending on the current i_{g4} and the switching state of q_{s4} . Thus:

$$i_c = \sum_{j=1}^3 (q_{lj}i_{lj} - q_{sj}i_{sj}) - q_{s4}i_{g4} = C \frac{dE}{dt}. \quad (1)$$

where C is the DC-link capacitance and E corresponds to the instantaneous voltage across the DC-link. The equivalent circuit of the proposed system is analyzed in order to derive the equations that describe the converter behavior, as well as to determine the voltages v_{shj} and v_{sej} and the relationships among the currents. Applying Kirchhoff's Laws to the equivalent circuit shown in Fig. 3, the following equations are obtained:

$$e_{gj} + L_a \frac{di_{sj}}{dt} + R_a i_{sj} = v_{sj0} - v_{s40}. \quad (2)$$

where R_a is the intrinsic resistance of the inductor L_a . The shunt-unit voltage is defined by (3).

$$e_{gj} + L_a \frac{di_{sj}}{dt} + R_a i_{sj} = v_{shj}. \quad (3)$$

The voltages e_{gj} are defined at the grid connection terminals of the proposed system. Therefore, the upstream feeder impedance is not explicitly included in the local shunt-branch equation, which relates the converter voltage to the terminal voltage through L_a and R_a . For the controller design and simulation analysis, these terminal voltages are treated as prescribed external disturbances. This assumption neglects the dynamic interaction between the feeder impedance and the converter currents. Consequently, the results establish the compensation performance under the evaluated terminal-voltage disturbances, while operation over a range of feeder

impedances is outside the scope of the present analysis. Therefore (2) can be rewritten as

$$v_{shj} = v_{sj0} - v_{s40}. \quad (4)$$

The voltages v_{sej} and the relationship between the currents are defined as follows:

$$v_{sej} = e_{gj} - v_{lj0} + v_{s40}. \quad (5)$$

$$i_{gj} = i_{lj} - i_{sj}. \quad (6)$$

$$i_{g4} = i_{g1} + i_{g2} + i_{g3}. \quad (7)$$

III. PULSE WIDTH MODULATION

The switching signals of the investigated converter were generated using a scalar pulse-width modulation (PWM) technique. For the investigated topology, the adopted PWM method includes third-harmonic injection. Considering the symbol $*$ denotes that the variables represent the desired reference values, from (4) and (5), the desired reference poles voltages are given by:

$$v_{sj0}^* = v_{shj}^* + v_{s40}^*. \quad (8)$$

$$v_{lj0}^* = e_{gj} - v_{sej}^* + v_{s40}^*. \quad (9)$$

Equations (8) and (9) form a linear system composed of six equations and seven variables. Therefore, the voltage v_{s40}^* can be freely defined, provided that it respects the voltage limits imposed by the converter. Hence, it is necessary to determine its maximum and minimum values according to the voltages generated by the converter and the maximum DC-link voltage. The maximum (v_{s4M}^*) and minimum (v_{s4m}^*) values that v_{s40}^* can assume are defined as (10) and (11), respectively.

$$v_{s4M}^* = \frac{E^*}{2} - \max(v_{sh1}^*, v_{sh2}^*, v_{sh3}^*, u_{l1}^*, u_{l2}^*, u_{l3}^*). \quad (10)$$

$$v_{s4m}^* = -\frac{E^*}{2} - \min(v_{sh1}^*, v_{sh2}^*, v_{sh3}^*, u_{l1}^*, u_{l2}^*, u_{l3}^*). \quad (11)$$

$$u_{lj}^* = e_{gj} - v_{sej}^*. \quad (12)$$

With these equations, the voltage v_{s40}^* can be determined using (13).

$$v_{s40}^* = \mu^* v_{s4M}^* + (1 - \mu^*) v_{s4m}^*. \quad (13)$$

Once v_{s40}^* is calculated, the pole voltages are obtained from (8) and (9). The resulting reference voltages are then compared with a high-frequency carrier signal to generate the switching commands for the semiconductor devices.

A. Influence of the μ^* parameter on PWM

To determine the pole voltage v_{s40}^* in (13), the variable μ^* must first be defined. This variable can be freely selected within the range $0 \leq \mu^* \leq 1$ and directly affects the reference pole voltages in (8) and (9). Although different values of μ^* are possible, its selection influences the harmonic distortion of the generated voltage. Fig. 4 illustrates the normalized pole voltage of phase 1 of the series unit and its reference for $\mu^* = 0$, $\mu^* = 1$, and $\mu^* = 0.5$ in

Fig. 4(a), (b), and (c), respectively. The same behavior can be observed for the other phases and for the shunt unit pole voltages. For $\mu^* = 0$ and $\mu^* = 1$, the pole voltage waveforms are asymmetric and exhibit intervals in which no switching occurs. Although this behavior may contribute to reducing switching losses, it results in higher harmonic distortion.

In addition, the total harmonic distortion (THD) of the load voltages was evaluated for the three considered values of μ^* . The obtained THD values were 1.015%, 1.021%, and 0.38% for $\mu^* = 0$, $\mu^* = 1$, and $\mu^* = 0.5$, respectively. Therefore, $\mu^* = 0.5$ provides a symmetrical pole-voltage waveform and reduces the THD of the load voltage. Based on these results, $\mu^* = 0.5$ is adopted throughout this work.

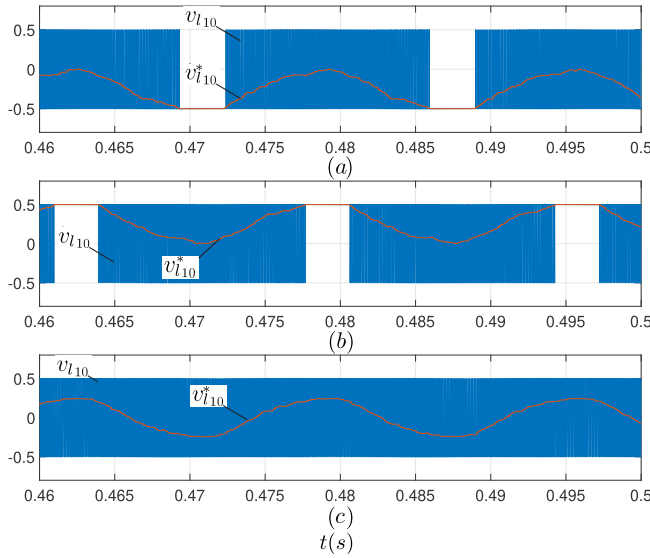


FIGURE 4. Pole voltage waveforms of the series unit for different values of μ^* . (a) $\mu^* = 0$. (b) $\mu^* = 1$. (c) $\mu^* = 0.5$.

IV. DC-LINK VOLTAGE SPECIFICATIONS

This section determines the minimum DC-link voltage required for the steady-state operation of the 7L-SAPF. From (8) and (9), considering that the pole voltages are limited to the interval $[-\frac{E^*}{2}, \frac{E^*}{2}]$, the following conditions must be satisfied:

$$E^* \geq |v_{shj}^*|, \quad (14)$$

$$E^* \geq |e_{gj} - v_{sej}^*|. \quad (15)$$

The condition in (15) shows that the phase angle ϕ between the grid voltage and the series unit reference voltage directly affects the minimum DC-link voltage. For the sinusoidal steady-state analysis, the grid voltage and the series-unit reference voltage can be represented by the phasors $\mathbf{E}_g$ and $\mathbf{V}_{se}^*$, whose magnitudes are E_g and V_{se}^* , respectively. Denoting by ϕ the angular displacement between these two phasors, the phasor diagram (see Fig. 5) can be constructed directly from the voltage difference appearing in (15). Thus,

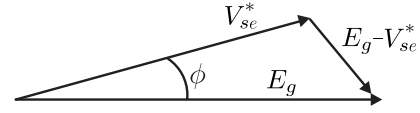


FIGURE 5. Phasor diagram under rated steady-state conditions.

Applying the law of cosines to the phasor diagram in Fig. 5 yields

$$|\mathbf{E}_g - \mathbf{V}_{se}^*| = \sqrt{E_g^2 + (V_{se}^*)^2 - 2E_gV_{se}^*\cos(\phi)}. \quad (16)$$

Substituting (16) into (15) gives

$$E^* \geq \sqrt{E_g^2 + (V_{se}^*)^2 - 2E_gV_{se}^*\cos(\phi)}. \quad (17)$$

In addition, according to (10) and (11), a valid value of v_{s40}^* must simultaneously satisfy the constraints imposed by all three phases and both converter units. Therefore, the upper and lower limits must satisfy $v_{s4M}^* \geq v_{s4m}^*$, resulting in

$$E^* \geq \max(V^*) - \min(V^*), \quad (18)$$

where

$$V^* = \{v_{sh1}^*, v_{sh2}^*, v_{sh3}^*, u_{l1}^*, u_{l2}^*, u_{l3}^*\}. \quad (19)$$

Therefore, the DC-link voltage must simultaneously satisfy (14), (17), and (18). Under rated balanced conditions, using the approximations in (24) and (25) and considering $e_{gj} = e_{lj}$, the maximum voltage excursion in (19) corresponds to the line-voltage amplitude. Thus, the minimum DC-link voltage is given by

$$E^* \geq \sqrt{3}E_{g_{rated}}, \quad (20)$$

where $E_{g_{rated}}$ is the amplitude of the rated phase-to-neutral grid voltage. During voltage sags, the grid-voltage amplitude decreases, and therefore the DC-link voltage defined by (20) remains sufficient. In contrast, voltage swells increase the voltage excursion in (18) and may require a higher DC-link voltage to ensure proper voltage synthesis.

V. OPERATION CONSTRAINTS

Fig. 6(a) presents the series-side behavior of the investigated 7L-SAPF. It can be inferred that the series converter voltage remains constant and equal to 1 p.u., which means that it does not depend on the load power factor.

The conventional 2L-SAPF configuration, operating without a fixed source in the DC-link, i.e., using minimum energy injection or quadrature control, presents some limitations, especially regarding voltage sag compensation. Equation (21) defines the DC-link voltage of the series module for any load power factor θ_l . From (21), it is possible to obtain the graph that describes the behavior of the voltage generated by the series unit for different power factor values while maintaining E_l equal to 1 p.u. (see Fig. 6(b)). During voltage sag disturbances, the topology depends on the load power factor to operate properly and loses its series compensation capability when the power factor is unity. During voltage swell disturbances, the topology presents fewer restrictions

for power factor values closer to zero. There is also a boundary region that defines the proper operating condition of the topology; below this region, the system is unable to compensate for any disturbance. Thus, the proposed system is more suitable for practical applications due to its wide applicability and load power factor independence.

$$V_{se} = E_l \sin(\theta_l) - \sqrt{E_g^2 - [E_l \cos(\theta_l)]^2}. \quad (21)$$

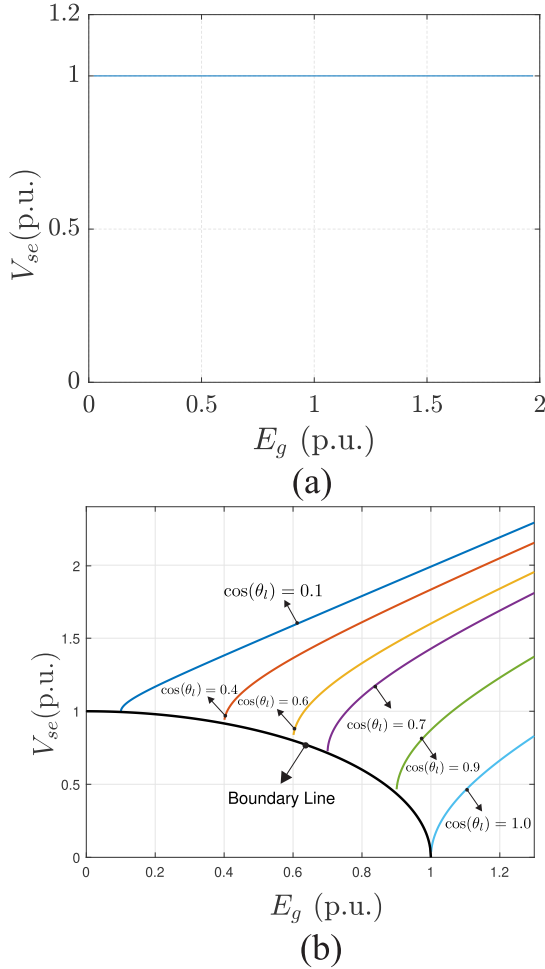


FIGURE 6. Series converter voltage required. (a) Proposed configuration, (b) Conventional 2L-SAPF.

VI. DESIGN OF PASSIVE DEVICES

This section presents the design of the converter passive components, including the filter inductors and capacitors, as well as the DC-link capacitor.

A. DC-link Capacitor

The minimum DC-link capacitance is determined based on the maximum allowable steady-state voltage ripple. The grid voltages are assumed to be balanced, while the shunt-unit currents are defined with equal amplitudes and in phase with the corresponding grid voltages. The load currents may

contain positive-, negative-, and zero-sequence components due to load unbalance and the presence of the fourth wire. In addition, converter losses are neglected. Under these assumptions, the instantaneous power at the DC-link, $p_c(t)$, can be expressed as

$$p_c(t) = \sum_{j=1}^3 v_{lj0} i_{lj} - v_{s40} i_{g4} - v_{sj0} i_{sj}. \quad (22)$$

Substituting (6), (7), (8), and (9) into (22), yields

$$p_c(t) = \sum_{j=1}^3 [(e_{gj} - v_{sej}^*) i_{lj} - v_{shj}^* i_{sj}]. \quad (23)$$

Under steady-state conditions, the series-unit voltages can be approximated by the load voltages, whereas the shunt-unit voltages can be approximated by the grid voltages, as given by (24) and (25).

$$\bar{v}_{shj}^* \approx e_{gj}, \quad (24)$$

$$\bar{v}_{sej}^* \approx e_{lj}. \quad (25)$$

Therefore, (23) can be rewritten in the form given by (26):

$$p_c(t) = \sum_{j=1}^3 [(e_{gj} - e_{lj}) i_{lj} - e_{gj} i_{sj}]. \quad (26)$$

Two important conclusions can be drawn from (26). First, under rated operating conditions, for which the grid and load voltages are approximately equal, the contribution associated with the load currents vanishes. Consequently, the low-frequency DC-link voltage oscillation is minimized, while the remaining ripple is mainly associated with high-frequency switching effects. Second, for a balanced load, the load currents do not contain a negative-sequence component. Therefore, regardless of the grid-voltage magnitude, the load-current-related term does not produce an oscillating power at twice the fundamental frequency, which is the power considered in the design of the DC-link capacitor.

As previously discussed, the load currents may contain positive, negative, and zero-sequence components and can be expressed as

$$i_{lj} = i_{lj}^+ + i_{lj}^- + i_{lj}^0. \quad (27)$$

By substituting these components into the instantaneous power expression and considering the aforementioned assumptions, (28) is obtained, which represents the instantaneous power at the DC-link:

$$p_c(t) = \frac{3}{2}(E_g - E_l)I_l^+ \cos \delta_+ - \frac{3}{2}E_g I_s - \frac{3}{2}(E_g - E_l)I_l^- \cos(2\omega_0 t + \delta_-). \quad (28)$$

here, E_g and E_l denote the amplitudes of the grid and load voltages, respectively. The quantities I_l^+ and I_l^- denote the amplitudes of the positive and negative-sequence components of the load currents, respectively, while δ_+ and δ_- denote their corresponding phase angles. Although a closed

path exists through the neutral conductor, the zero-sequence contribution cancels in the three-phase summation of the instantaneous power. Therefore, it contributes neither to the average power nor to the $2\omega_0$ oscillating component of the total DC-link power $p_c(t)$. The power given by (28) consists of an average component and an oscillating component at twice the fundamental frequency. Under steady-state conditions, the average powers exchanged by the series and shunt units are balanced through the DC-link. Hence, the net power handled by the DC-link capacitor is the oscillating component. As expressed in (29), this oscillating power is absorbed and released by the DC-link capacitor and can be written as

$$p_c(t) = -\frac{3}{2}(E_g - E_l)I_l^- \cos(2\omega_0 t + \delta_-). \quad (29)$$

The DC-link voltage can be decomposed into its average value and an instantaneous ripple component $\tilde{e}(t)$. Assuming a small voltage ripple, i.e., $\tilde{e}(t) \ll E$, the instantaneous DC-link voltage can be approximated by $e(t) \approx E$. Therefore, the instantaneous capacitor power can be approximated as

$$p_c(t) \approx CE \frac{d\tilde{e}(t)}{dt}. \quad (30)$$

Equating (29) and (30) and isolating the derivative of the voltage ripple yields

$$\frac{d\tilde{e}(t)}{dt} = -\frac{3(E_g - E_l)I_l^-}{2CE} \cos(2\omega_0 t + \delta_-). \quad (31)$$

Integrating both sides with respect to time, the instantaneous DC-link voltage ripple is obtained as

$$\tilde{e}(t) = -\frac{3(E_g - E_l)I_l^-}{4\omega_0 CE} \sin(2\omega_0 t + \delta_-). \quad (32)$$

Consequently, the peak amplitude of the DC-link voltage ripple, ΔE_p , is given by

$$\Delta E_p = \frac{3|E_g - E_l|I_l^-}{4\omega_0 CE}. \quad (33)$$

Considering the peak-to-peak voltage ripple, ΔE_{pp} , as twice the peak ripple amplitude, (33) can be rewritten as

$$\Delta E_{pp} = \frac{3|E_g - E_l|I_l^-}{2\omega_0 CE}. \quad (34)$$

Finally, for a specified maximum allowable peak-to-peak DC-link voltage ripple, the minimum required capacitance is determined by (35):

$$C_{\min} \geq \frac{3|E_g - E_l|I_l^-}{2\omega_0 E^* \Delta E_{pp}}. \quad (35)$$

B. Filter Design

The minimum filter inductance can be determined based on the maximum allowable current ripple. During a switching period, the voltage across the inductor assumes two levels, corresponding to its maximum and minimum values. Considering that the average voltage across the inductor must be zero under steady-state conditions, it follows that

$$\int_0^{dT_s} V_{L_{\max}} dt + \int_{dT_s}^{T_s} V_{L_{\min}} dt = 0. \quad (36)$$

In addition, the inductor voltage variation, ΔV , is defined as

$$\Delta V = V_{L_{\max}} - V_{L_{\min}}. \quad (37)$$

Solving (36) and (37), the maximum and minimum inductor voltages can be expressed as functions of the duty cycle as

$$V_{L_{\max}} = \Delta V(1 - d), \quad (38)$$

$$V_{L_{\min}} = -\Delta Vd. \quad (39)$$

Figure 7 illustrates the voltage and current waveforms of the inductor. Considering that the inductor current ripple is

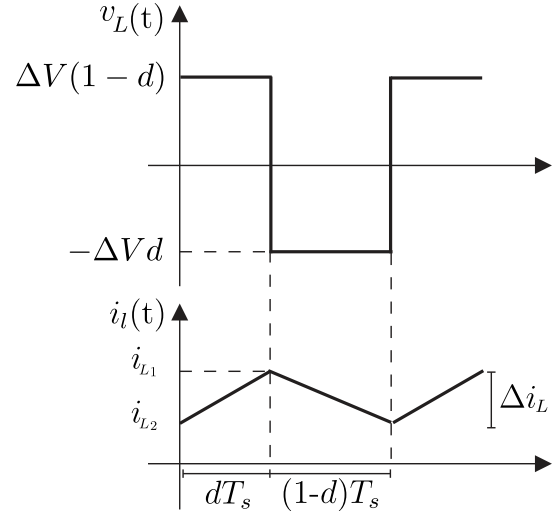


FIGURE 7. Inductor voltage and current waveforms.

defined as

$$\Delta I_L = I_{L1} - I_{L2}, \quad (40)$$

the following expression is obtained:

$$\Delta I_L = \frac{1}{L} \int_0^{dT_s} \Delta V(1 - d) dt = \frac{\Delta V(1 - d)dT_s}{L}. \quad (41)$$

Differentiating (41) with respect to the duty cycle d and setting the resulting expression equal to zero yields the condition for the maximum current ripple:

$$\frac{d(\Delta I_L)}{dd} = \frac{\Delta VT_s}{L}(1 - 2d), \quad (42)$$

$$\frac{\Delta VT_s}{L}(1 - 2d) = 0, \quad (43)$$

which results in

$$d = \frac{1}{2}. \quad (44)$$

Substituting this value into (41), the minimum inductance required to satisfy the maximum allowable current ripple is obtained as

$$L_{\min} \geq \frac{\Delta V}{4f_{sw}\Delta I_{L_{\max}}}. \quad (45)$$

The filter capacitor, denoted by C_f , is designed based on the desired resonant frequency of the LC filter. Considering

that the filter inductance L_f has already been determined, the angular resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_f C_f}}. \quad (46)$$

In terms of the resonant frequency in hertz, it follows that

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}}. \quad (47)$$

Solving for the filter capacitance C_f yields

$$C_f = \frac{1}{(2\pi f_r)^2 L_f}. \quad (48)$$

VII. CONTROL STRATEGY

In this section, the control strategy of the proposed topology is analyzed. The control diagram is presented in Fig. 8 and is divided into five parts, denoted *I*, *II*, *III*, *IV*, *V*.

Before detailing the control diagram, it is important to emphasize that, as previously presented, the 6L-SAPF topology includes bidirectional switches in its structure, which are responsible for disconnecting the shunt unit during grid swell conditions. This operation allows the DC-link voltage to increase until it reaches a value higher than the grid peak voltage during the disturbance. After this condition is achieved, the switches are closed again, allowing the current control strategy to be reestablished. However, the implementation cost and the complexity associated with the operation of these bidirectional switches may increase the overall system complexity and reduce its practical attractiveness. Therefore, for the investigated topology, the removal of these bidirectional switches is proposed in order to simplify the structure and reduce the implementation complexity of the system. The removal of these switches becomes feasible due to the adoption of a specific control strategy capable of increasing the DC-link voltage during grid swell conditions, ensuring values higher than the grid peak voltage.

The new control strategy developed is located in Part *I* of the control diagram. The DC-link voltage (E) is controlled by means of a conventional PI controller (block R_E), in which a constant reference value is defined for the DC-link voltage ($E^* = E_{nom} = 320V$), under rated operating conditions and during voltage sag events. The PI controller processes the DC-link voltage error ($E^* - E$) and, based on this value, provides the reference amplitude for the currents flowing through the shunt path (I_s^*). The transfer function of the PI controller in block R_E , in the frequency domain, is given by:

$$R_E(s) = k_{pC} + \frac{k_{iC}}{s}. \quad (49)$$

Under voltage swell conditions, the proposed strategy modifies the DC-link voltage reference whenever the disturbance is detected. Thus, instead of remaining constant, as defined under rated operating conditions (i.e., $E^* = E_{nom}$, where E_{nom} is the previously defined constant voltage), the reference assumes the form of an increasing ramp,

E_{ramp} , initiated at the instant the disturbance is identified, that is, when the RMS grid voltage E_g becomes greater than or equal to 10% above the rated voltage, i.e., when $E_g \geq 1.1E_{grated}$. The ramp is maintained until the instantaneous DC-link voltage reaches twice the final amplitude of the disturbance, $2A_g$. This procedure ensures that the DC-link voltage becomes sufficiently high for the series unit to properly compensate the load voltage during the swell event. Subsequently, when the grid voltage starts returning to its nominal value, the control system detects this condition and generates a decreasing ramp for the DC-link voltage reference, allowing the system to gradually return to the previously established operating point. The flowchart shown in Fig. 9 illustrates the behavior of the reference voltage for these different operating conditions.

Considering the nominal grid voltage $E_{grated} = 110V$, the nominal peak value is given by (50). The instantaneous peak voltage is estimated from the RMS value E_g , as calculated in (51). Based on these equations, the voltage swell level in p.u. can be determined from (52).

$$A_{nom} = 110\sqrt{2}. \quad (50)$$

$$A_g = E_g\sqrt{2}. \quad (51)$$

$$\Delta v_{swell} = \max\left(0, \frac{A_g - A_{nom}}{A_{nom}}\right). \quad (52)$$

The ramp increment is then defined as

$$k_{ramp} = K_{step}\Delta v_{swell}. \quad (53)$$

where K_{step} is a tuning gain expressed in volts per control step, which was set to 1 in this work. Therefore, k_{ramp} represents the voltage increment or decrement applied to the ramp at each control iteration. In this case, the increment or decrement rate depends on the voltage swell level, such that under more severe swell conditions the ramp becomes faster, whereas under less severe swell conditions the ramp becomes slower. This enables a dynamic ramp adjustment according to the voltage swell level. The ramp is updated according to (54).

$$E_{ramp}^*[k+1] = \min(E_{ramp}^*[k] \pm k_{ramp}, 2A_g). \quad (54)$$

In *II*, grid synchronization is performed using single-phase power-based Phase-Locked Loops (pLLs) based on the structure presented in [34], with one pLL independently implemented for each grid phase. Each pLL estimates the phase angle of the fundamental component of its corresponding grid voltage, which is used to generate the synchronized shunt-unit current i_{sj} . As reported in [34], the pLL can exhibit low sensitivity to voltage harmonic distortion when properly tuned. This behavior is evaluated in Fig. 10, where 5th- and 7th-order harmonics are introduced into the grid voltage at $t = 1s$. The resulting phase-angle error $\Delta\theta$ remains below 0.5° during the transient and returns close

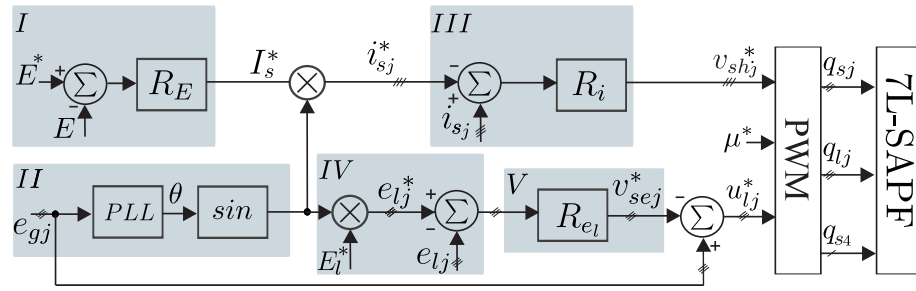


FIGURE 8. Control diagram of the proposed topology.

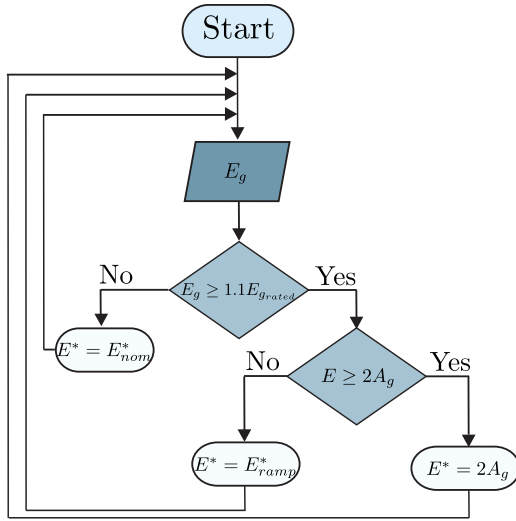


FIGURE 9. Flowchart of the DC-link voltage reference operation.

to zero within approximately 0.13s, while the estimated frequency remains close to 60 Hz. These results indicate that the adopted pPLL maintains synchronization with the fundamental component under the considered harmonic distortion. The synchronized shunt currents provide the active power required for DC-link voltage regulation and converter-loss compensation and, during voltage sags and swells, contribute to maintaining the converter input power. Their references are defined as

$$i_{sj}^* = I_{sj}^* \sin \left[\theta + (1 - j) \frac{2\pi}{3} \right]. \quad (55)$$

In *III*, the Proportional-Resonant (PR) controllers, denoted by blocks R_i , receive the current error ($i_{sj} - i_{sj}^*$) and generate the reference voltage v_{shj}^* . The transfer function of the R_i and R_{el} blocks is :

$$R_i(s) = k_{pi} + \frac{2k_{ii}\omega_b s}{s^2 + 2\omega_b s + \omega_0^2}, \quad (56)$$

where $\omega_0 = 2\pi f$, $f = 60$ Hz, that is, the fundamental frequency of the electrical grid. The parameter ω_b defines the bandwidth around the resonant frequency ω_0 . Its inclusion reduces the controller's sensitivity to small variations in ω_0 and limits the resonant gain to a high but finite value [35].

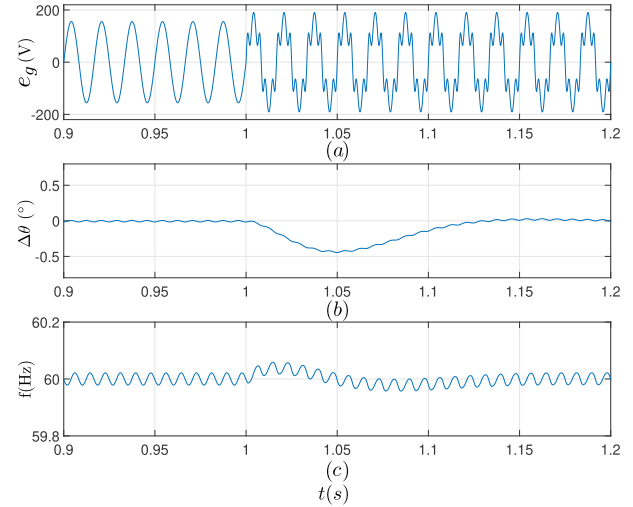


FIGURE 10. Response of the pPLL to harmonic component injection into the input voltage. (a) pPLL input voltage. (b) Phase error. (c) Estimated frequency.

In block *IV*, from the grid voltage angle θ and a reference amplitude for the load voltage (E_l^*), the instantaneous reference voltages for the load (e_l^*) are determined.

Finally, in block *V*, the Proportional-Resonant, denoted as R_{el} , receives the load voltage error ($e_l^* - e_l$) and processes it to determine the voltage that the series unit must generate. Based on this voltage and according to (12), the grid voltage of the corresponding phase is subtracted, resulting in the reference pole voltages of the series converter, denoted as v_{lj0} . The transfer function of this controller is given equivalently as shown in (56).

VIII. CONTROL SYSTEM DESIGN

This section presents the frequency-response-based design of the controllers employed in the converter. The crossover frequency of the current loop is selected approximately one decade below the converter switching frequency to ensure a fast transient response. In contrast, the voltage-loop crossover frequency is chosen significantly lower than that of the current loop, ensuring adequate decoupling between the control loops and a slower voltage-control dynamics [36]. Furthermore, a phase margin of 60° is adopted for both control loops to ensure stability and satisfactory dynamic

performance [37]. The controller design is performed by imposing a crossover frequency ω_c and a desired phase margin (PM). At the crossover frequency, the magnitude condition is given by

$$|R(j\omega_c)G(j\omega_c)| = 1, \quad (57)$$

whereas the open-loop phase condition is

$$\angle R(j\omega_c) + \angle G(j\omega_c) = -\pi + PM. \quad (58)$$

A. Shunt Current Control

The plant used for the shunt current control can be obtained from (3). Considering the grid voltage as a disturbance and R_a as the intrinsic resistance of the filter inductor, the application of the Laplace transform yields

$$G_i(s) = \frac{I_s(s)}{V_{sh}(s)} = \frac{1}{R_a + sL_a}. \quad (59)$$

The controller gains can then be determined from

$$A = \omega_0^2 - \omega_c^2, \quad (60)$$

$$B = 2\omega_b\omega_c, \quad (61)$$

$$M = \sqrt{R_a^2 + (\omega_c L_a)^2}, \quad (62)$$

$$\theta = PM - \pi + \tan^{-1} \left(\frac{\omega_c L_a}{R_a} \right), \quad (63)$$

$$k_{ii} = \frac{M \sin(\theta)(A^2 + B^2)}{AB}, \quad (64)$$

$$k_{pi} = M \cos(\theta) - M \sin(\theta) \frac{B}{A}. \quad (65)$$

B. DC-link Voltage Control

To determine the gains of the PI controller responsible for DC-link voltage regulation, a small-signal transfer function relating the DC-link voltage to the shunt-unit current must first be obtained. As previously discussed, the DC-link power consists of an average component and an oscillating component at twice the fundamental frequency. For the voltage-control plant, only the average power component is considered, since the voltage controller is not designed to compensate for the double-frequency power oscillation. In addition, a resistance R_p connected in parallel with the DC-link capacitor is considered to represent the converter losses. By linearizing the power balance around the operating point, separating the steady-state and small-signal components, and treating the series-unit power as an external disturbance, the DC-link voltage plant is obtained as

$$G_v(s) = \frac{\tilde{E}(s)}{\tilde{I}_s(s)} = -\frac{\frac{3}{2}E_g}{CEs + \frac{2E}{R_p}}. \quad (66)$$

Applying the previously defined magnitude and phase conditions, the PI controller gains are obtained from

$$M = \frac{E \sqrt{\left(\frac{2}{R_p}\right)^2 + (\omega_c C)^2}}{1.5E_g}, \quad (67)$$

$$\theta = PM - \pi + \tan^{-1} \left(\frac{\omega_c C R_p}{2} \right), \quad (68)$$

$$k_{pC} = M \cos(\theta), \quad (69)$$

$$k_{iC} = -\omega_c M \sin(\theta). \quad (70)$$

It should be noted that the negative sign of the plant in (66) is omitted during the controller-gain calculation. In the complete control system, this sign is accounted for by the polarity of the control action.

C. Load Voltage Control

For the control of the load voltages, a proportional-resonant controller was employed and implemented similarly to the current control scheme.

IX. RESULTS

This section presents closed-loop simulation and experimental results validating the proposed 7L-SAPF converter. The experimental tests employed SEMIKRON power devices (SKM50GB123D IGBTs and SKH23 drivers) and a TMS320F28335 DSP. Table 2 lists the parameters adopted in both simulation and experiments. Fig. 11 illustrates the setup used to obtain the simulation and experimental results.

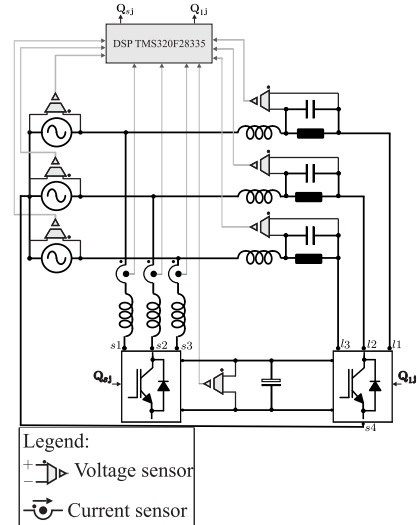


FIGURE 11. Setup for simulation and experimental results.

A. Simulation Results

Fig. 12 illustrates the converter operation when the grid voltage is subjected to significant harmonic distortion. In this test, 5th- and 7th-order harmonic components are added to the grid voltage, resulting in a THD of 35.50%, as shown in Fig. 12(a). Such voltage distortions, if not properly compensated, may adversely affect the connected loads. As shown in Fig. 12(b), the load voltages remain sinusoidal at the nominal amplitude and frequency, with the THD reduced to 0.83%, demonstrating the effectiveness of the proposed compensation.

TABLE 2. Parameters considered for simulation and experimental results.

Parameter	Description	Value
$E_{g_{rated}}$	Grid voltage (rms)	110 V
E_l	Load voltage (rms)	110 V
f_{sw}	Switching frequency	10 kHz
f_0	Grid and load frequency	60/60 Hz
E^*	DC-link voltage reference	320 V
C	DC-link capacitance	2.2 mF
L_f	Filter inductance	2 mH
C_f	Filter capacitance	46 μ F
L_a	Filter inductance	7 mH
R_1	Load resistance	15 Ω
R_2	Load resistance	22.5 Ω
R_3	Load resistance	45 Ω
L_1	Load inductance	21 mH
L_2	Load inductance	21 mH
L_3	Load inductance	21 mH
pf	Power factor	0.93 lagging
Controller Gains		
k_{pC}	Proportional gain of $R_E=R_{el}$	0.8
k_{iC}	Integral gain of $R_E=R_{el}$	22.0
k_{pi}	Proportional gain of R_i	5.0
k_{ii}	Integral gain of R_i	1000.0

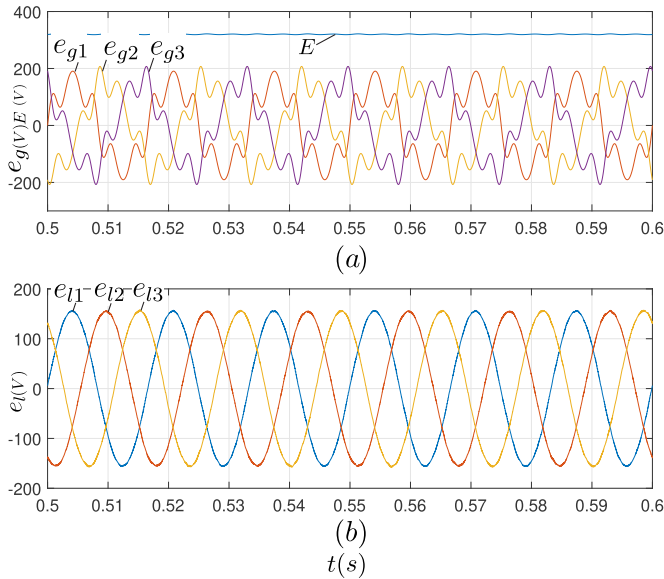


FIGURE 12. Simulation results of the system operating under grid voltage harmonic distortion conditions. (a) Grid voltages with 35.50% THD and DC-link voltage. (b) Load voltages with 0.83% THD.

Fig. 13 illustrates the grid and DC-link voltages, as well as the load currents, under rated operating conditions.

Fig. 14(a) illustrates the converter operating under rated conditions ($t < 0.6$ s) and during a 50% voltage sag ($t > 0.6$ s). It can be observed that the converter exhibits the expected performance, since even during and after the disturbance, the load voltages (e_{lj} , see Fig. 14(b)) remain close to their respective reference values. This demonstrates

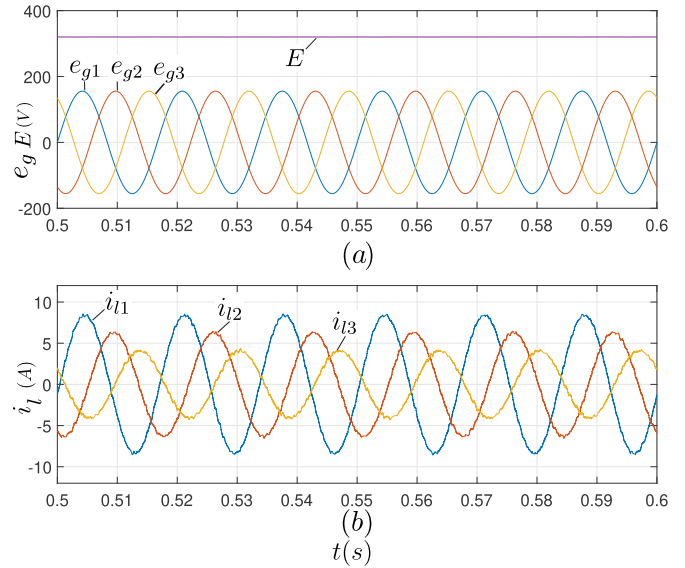


FIGURE 13. Simulation results with the system operating under rated. (a) Grid and DC-link voltages. (b) Load currents.

the effectiveness of the system in mitigating disturbances. Furthermore, it is possible to observe that the DC-link voltage control system operates properly, since even during the voltage sag, the DC-link voltage remains regulated at its respective reference value. This indicates that the control strategy is also capable of rejecting possible disturbances in the system. Fig. 14(c) illustrates the waveform of the phase-1 shunt unit current (i_{s1}). It can be observed that, under rated operating conditions, its RMS value is low. However, during voltage sag conditions, this current increases in order to maintain the input power, as previously discussed.

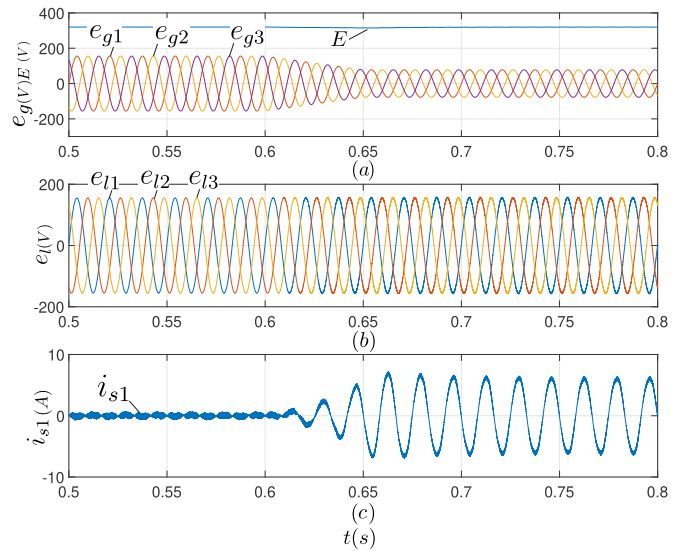


FIGURE 14. Simulation results with the system operating under rated and voltage sag conditions. (a) Grid and DC-link voltages. (b) Load voltages. (c) Phase-1 shunt unit current.

The behavior of the proposed topology operating under a 70% voltage swell condition is illustrated in Fig. 15(a) for

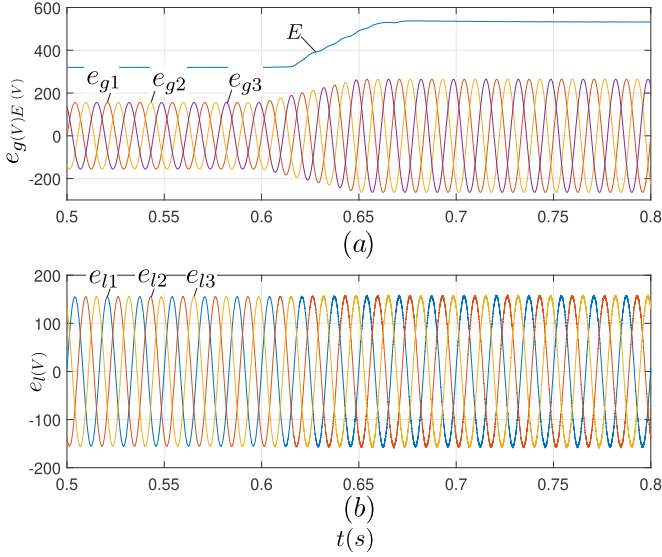


FIGURE 15. Simulation results with the system operating under voltage swell conditions. (a) Grid and DC-link voltages. (b) Load voltages.

$t > 0.6$ s. As previously explained, during the voltage swell condition, the control system changes the DC-link voltage reference to a ramp profile until it reaches twice the peak amplitude of the grid voltage at the instant of the disturbance. According to the presented results, it can be confirmed that the control strategy operates properly, since the DC-link voltage begins to increase following a ramp profile at the initial instant of the voltage swell and stops when the final reference condition is achieved. Furthermore, it can be observed that the system fulfills its purpose, since during the voltage swell, the load voltages (e_{lj} , see Fig. 15(b)) remain close to their defined reference values.

Fig. 16(a) illustrates the grid voltage waveforms under unbalanced disturbance conditions, in which phase 1 undergoes a 70% voltage swell, phase 2 is subjected to a 30% voltage sag, and phase 3 presents a 50% voltage sag. It can be observed in Fig. 16(b) that the load voltages remain properly regulated, indicating that the proposed topology is effective in compensating unbalanced disturbances.

As demonstrated by these results, the proposed topology is feasible, since it is capable of compensating both balanced and unbalanced voltage disturbances, as well as harmonic distortions, thereby ensuring the proper operation of the equipment connected to the grid.

B. Experimental Results

The experimental results are presented in Figs. 17(a)-(f). Fig. 17(a) highlights the waveforms of the grid voltage in phase 1 (e_{g1}), the load voltage in phase 1 (e_{l1}), the load voltage in phase 3 (e_{l3}), and the current of phase 1 of the shunt unit (i_{s1}) under rated operating conditions. As observed in the simulation results, under rated conditions, the current of the shunt unit (i_{s1}) presents a low RMS value, which can be verified in this figure.

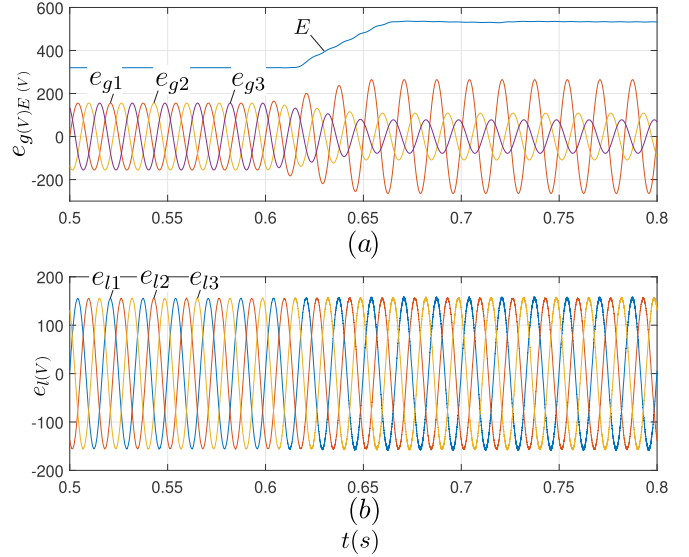


FIGURE 16. Simulation results of the topology operating under unbalanced disturbance conditions. (a) Grid voltages and DC-link voltage. (b) Load voltages.

Figs. 17(b) and (c) show the system behavior during the transient caused by a 50% grid voltage sag. It can be observed that the amplitude of the shunt unit current increases in order to maintain the input power, as previously explained. It can also be observed that the DC-link voltage remains regulated throughout the disturbance.

Fig. 17(d) illustrates the waveforms of the grid voltage in phase 1, the DC-link voltage, and the load voltages when the proposed topology operates under a 70% grid voltage swell condition. It can be observed that, upon detecting the voltage swell, the control system acts on the DC-link voltage by increasing its value, as previously discussed. Fig. 17(e) illustrates the system operating under the steady-state condition of a 70% grid voltage swell.

Finally, Fig. 17(f) illustrates the phase-1 grid voltage, the load voltages in phases 1 and 3, and the DC-link voltage when the grid voltages return to nominal conditions. It can be observed that the DC-link voltage also decreases, returning to the value defined prior to the disturbance.

In all cases, it is evident that the load voltages were not affected by the disturbances, thus ensuring the proper supply of electrical energy to the consumer units or connected equipment.

X. TOPOLOGY COMPARISONS

This section presents a comparative analysis of the 2L-SAPF, 6L-SAPF, and the proposed topology in terms of the number of components, minimum DC-link voltage, semiconductor device losses, and total harmonic distortion (THD) of the load voltage. The comparisons regarding THD and semiconductor losses were carried out through simulations in PSIM using the parameters listed in Table 3. Different load parameters were adopted because the 2L-SAPF is unable to

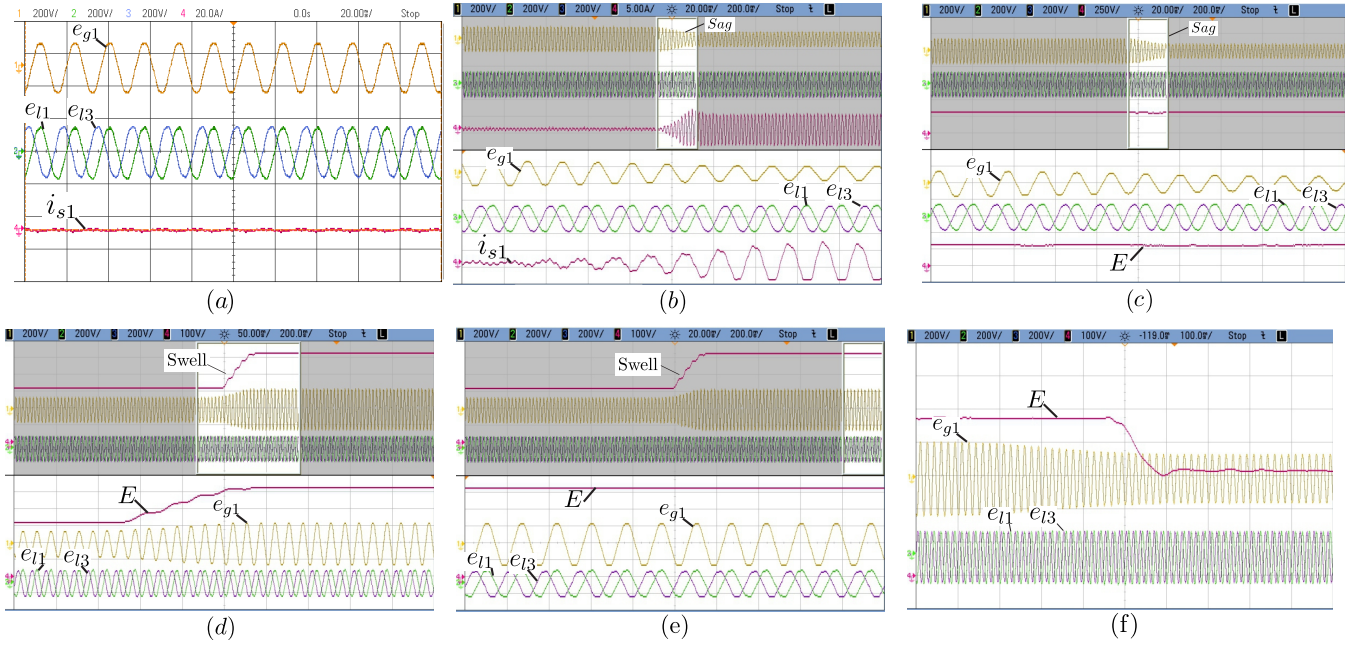


FIGURE 17. Experimental results for the proposed topology under different conditions. (a) Rated operating conditions. (b)-(c) Grid voltage sag. (d)-(e) Grid voltage swell. (f) Grid and DC-link voltages returning to nominal operating conditions.

compensate the disturbances under the load power factor of the previously defined load. All other system parameters are identical to those presented in Table 2.

TABLE 3. Load parameters used in the comparison among the topologies.

Parameter	Description	Value
R_1	Load resistance	8.5 Ω
R_2	Load resistance	10 Ω
R_3	Load resistance	12 Ω
L_1	Load inductance	30 mH
L_2	Load inductance	35 mH
L_3	Load inductance	42 mH
pf	Power factor	0.6 lagging

A. Number of Components and Minimum DC-link Voltage

Table 4 compares the proposed topology with the 6L-SAPF and the conventional 2L-SAPF in terms of the number of power components and the minimum DC-link voltage required by the series converter to synthesize the compensation voltage under the evaluated grid disturbances.

As can be observed, the proposed 7L-SAPF requires 14 IGBTs, whereas the 6L-SAPF and the conventional 2L-SAPF require 12 IGBTs. This increase is a consequence of the additional converter leg introduced in the proposed structure. However, this additional leg provides an extra degree of freedom for voltage synthesis, allowing the converter to achieve the required compensation voltage with a reduced DC-link voltage when compared with the conventional 2L-SAPF.

Another relevant feature of the proposed topology is the reduced number of DC-link capacitors. While the 6L-SAPF

and the 2L-SAPF require two and three DC-link capacitors, respectively, the proposed 7L-SAPF uses only one DC-link capacitor. This simplifies the DC-link structure and avoids the use of multiple split DC-link capacitor groups.

Regarding the minimum DC-link voltage, the proposed 7L-SAPF requires only 1.0 p.u., the same value required by the 6L-SAPF. In contrast, the conventional 2L-SAPF requires 1.25 p.u. to generate the necessary compensation voltage.

TABLE 4. Comparison of component count and minimum DC-link voltage.

1 p.u. = $E^* = 320$ V.

Topology	7L-SAPF	6L-SAPF	2L-SAPF
No. of IGBTs	14	12	12
No. of DC-link Capacitors	1	2	3
DC-link Voltage (p.u.)	1.0	1.0	1.25

B. DC-link Capacitance and Stored Energy Comparison

The topologies were evaluated in terms of the required DC-link capacitance and stored energy to limit the peak-to-peak voltage ripple to 5% of the average DC-link voltage under a 30% voltage sag condition, considering the DC-link voltages defined in Table 4. The comparison results are summarized in Table 5. The proposed 7L-SAPF requires the lowest DC-link capacitance, with 60 μ F, compared with 105 μ F and 300 μ F for the 6L-SAPF and 2L-SAPF, respectively. A similar trend is observed for the stored energy: the proposed topology requires only 3.072 J, whereas the 6L-SAPF and 2L-SAPF require 5.38 J and 24 J, respectively. Therefore, for the same voltage-ripple criterion and operating condition, the proposed 7L-SAPF presents the lowest DC-link energy-storage

requirement. This characteristic can potentially reduce the capacitor volume and passive-component requirements while maintaining the same DC-link voltage-ripple performance.

TABLE 5. DC-link capacitance and stored energy for the evaluated topologies.

Topology	C (μF)	Energy (J)
7L-SAPF	60	3.072
6L-SAPF	105	5.38
2L-SAPF	300	24.00

C. Harmonic Distortion Analysis

The total harmonic distortion (THD) of the load voltage is defined as the ratio between the RMS value of the harmonic components and the RMS value of the fundamental component, as follows:

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100, \quad (71)$$

where V_n denotes the RMS value of the n -th harmonic component, and V_1 is the RMS value of the fundamental voltage component.

The harmonic performance of the evaluated topologies was analyzed under rated grid-voltage operation, as well as under 30% voltage sag and 30% voltage swell conditions. The obtained load-voltage THD values are presented in Table 6. It can be observed that the proposed 7L-SAPF provides the lowest THD among the evaluated topologies for all operating conditions.

Compared with the conventional 2L-SAPF, the proposed topology reduces the load-voltage THD from 4.39% to 0.38% under rated operation, from 4.20% to 0.78% under voltage sag, and from 4.13% to 1.10% under voltage swell. These results demonstrate that the proposed structure improves the quality of the compensated load voltage, especially under rated operation, where the THD reduction is more pronounced.

This improved harmonic performance can be attributed to two main factors. First, the proposed topology reduces the DC-link voltage ripple, which directly improves the quality of the voltage synthesized by the series unit. Second, according to (5), the voltage component v_{s40} contributes to the series compensation voltage, increasing the voltage synthesis capability of the converter and improving the resulting waveform quality.

D. Semiconductor Power Losses

The semiconductor losses of the evaluated converters were estimated using the thermal module of PSIM, considering the same IGBT module for all topologies in order to ensure a fair comparison. The selected device was the SEMIKRON SKM200GB125D, a 1200-V, 150-A half-bridge IGBT module. The loss calculation includes both conduction and switching losses of the IGBTs and their antiparallel diodes.

TABLE 6. Load voltage THD (%) under different operating conditions.

Topology	Condition	e_l THD (%)
7L-SAPF	Swell	1.10
	Rated	0.38
	Sag	0.78
6L-SAPF	Swell	3.65
	Rated	2.88
	Sag	2.44
2L-SAPF	Swell	4.13
	Rated	4.39
	Sag	4.20

For each converter, the total semiconductor loss is obtained by summing the conduction and switching losses of all semiconductor devices, as follows:

$$P_T = \sum_{k=1}^N (P_{\text{cond},k} + P_{\text{sw},k}), \quad (72)$$

where N is the total number of semiconductor switches, while $P_{\text{cond},k}$ and $P_{\text{sw},k}$ denote, respectively, the conduction and switching losses associated with the k -th device.

The proposed 7L-SAPF, the conventional 2L-SAPF, and the 6L-SAPF were evaluated under rated grid-voltage operation, as well as under 30% voltage sag and 30% voltage swell conditions. The switching frequency was set to 10 kHz for all cases. The obtained results are summarized in Table 7.

As expected, the proposed 7L-SAPF presents higher losses than the 6L-SAPF due to the additional converter leg. However, this increase is associated with the extra degree of freedom provided by the proposed structure, which extends the operating range of the series active power filter.

The most relevant comparison, however, is with the conventional 2L-SAPF, since it represents the baseline structure. In this regard, the proposed topology demonstrates an advantageous loss behavior. Under rated operation, the total semiconductor losses are reduced from 149.28 W in the 2L-SAPF to 118.98 W in the proposed 7L-SAPF. Under voltage sag, the losses are also reduced, from 159.22 W to 142.72 W. Under voltage swell, the losses of the proposed topology remain in the same range as those of the 2L-SAPF. Therefore, although the proposed structure employs an additional converter leg, it achieves lower losses than the conventional topology in rated and sag conditions, while preserving a comparable loss level under swell operation and extending the voltage compensation capability of the series active power filter.

It is worth noting that all topologies were compared using the same switching frequency. As shown in the harmonic distortion analysis, the proposed 7L-SAPF provides lower load-voltage THD than the benchmark topologies at 10 kHz. Therefore, in a practical design, this improved waveform quality could be exploited to reduce the switching frequency of the proposed converter while still meeting a THD target comparable to that of the 2L-SAPF or 6L-SAPF. Since

the switching losses represent the dominant portion of the total semiconductor losses in Table 7, such an optimization would further improve the loss performance of the proposed topology.

TABLE 7. Semiconductor power losses at 10 kHz switching frequency.

Topology	Condition	P_{cond} (W)	P_{sw} (W)	P_T (W)
7L-SAPF	Swell	17.34	152.21	169.55
	Rated	15.74	103.24	118.98
	Sag	19.44	123.28	142.72
6L-SAPF	Swell	16.11	127.06	143.17
	Rated	14.50	78.01	92.51
	Sag	18.16	102.10	120.26
2L-SAPF	Swell	14.98	126.41	141.39
	Rated	18.44	130.84	149.28
	Sag	22.93	136.29	159.22

XI. CONCLUSION

This work proposed a transformerless open-end series active power filter for the compensation of balanced and unbalanced voltage disturbances. The converter model, PWM strategy, control scheme, operating constraints, controller and passive component design, simulation and experimental results, and a comparative analysis with benchmark topologies were presented.

The proposed topology does not require low-frequency series transformers, which contributes to reducing the size, weight, and cost of the compensation system. In addition, the converter operates independently of the load power factor, does not require a fixed dc source at the DC-link, and avoids phase jumps in the load voltages during compensation.

Compared with the conventional 2L-SAPF, the proposed topology reduces the minimum required DC-link voltage while also requiring fewer DC-link capacitors. These features improve the DC-link voltage utilization and simplify the energy storage structure of the converter. Compared with the 6L-SAPF, the proposed structure uses an additional converter leg, which increases the number of semiconductor devices. However, this additional degree of freedom eliminates the need for split DC-link capacitors and contributes to reducing the DC-link capacitor voltage ripple.

The comparative analysis also showed that, although the proposed topology may present higher semiconductor losses than the 6L-SAPF due to the additional converter leg, its loss performance remains competitive with respect to the conventional 2L-SAPF. Moreover, the proposed 7L-SAPF achieved the lowest load-voltage THD among the evaluated topologies under rated, voltage sag, and voltage swell conditions.

The comparative analysis in terms of DC-link capacitance and stored energy showed that the proposed topology requires the lowest capacitance and stored energy to satisfy the same DC-link voltage-ripple constraint, resulting in a more compact DC-link energy-storage structure, with potential reductions in capacitor size, volume, and cost.

Therefore, the proposed topology provides an effective solution for series voltage compensation, combining transformerless operation, reduced DC-link capacitor requirements, improved DC-link voltage utilization, and enhanced load-voltage quality.

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AUTHOR'S CONTRIBUTIONS

A.T.S.S.SANTOS: Conceptualization, Data Curation, Formal Analysis, Funding Acquisition, Investigation, Methodology, Project Administration, Resources, Software, Supervision, Validation, Visualization, Writing – Original Draft, Writing – Review & Editing. **C.B.JACOBINA:** Conceptualization, Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Visualization. **J.T.CARDOSO:** Investigation, Project Administration, Resources, Software, Supervision, Writing – Review & Editing. **A.S.FELINTO:** Conceptualization, Funding Acquisition, Investigation, Methodology, Software, Supervision, Validation.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

REFERENCES

- [1] C. Deshpande, R. Chilipi, S. Arya, "Frequency Adaptive Enhanced Reduced-Order Generalized Integrator Control for Operation of DVR", *IEEE Transactions on Industry Applications*, vol. 61, no. 6, pp. 8542–8554, 2025, doi:10.1109/TIA.2025.3571863.
- [2] R. d. C. Ferreira, P. H. d. M. Martins, N. Rocha, E. R. C. da Silva, V. F. M. B. Melo, "Comparison Between Hysteresis and Predictive Control with Optimized Vector Selection for Direct Power Control to a Shunt Active Power Filter", *Eletrônica de Potência*, vol. 30, p. e202507, Jan. 2025, doi:10.18618/REP.e202507.
- [3] T. B. Soeiro, C. A. Petry, A. J. Perin, "Estabilizadores De Tensão Alternada Do Tipo Compensadores De Tensão", *Eletrônica de Potência*, vol. 14, no. 2, p. 97–105, May 2009, doi:10.18618/REP.2009.2.097105.
- [4] S. Janardhanan, M. A. Mulla, "Implementation of Voltage Imbalance Mitigation Using SOGI Based PV-DVR System", *IEEE Transactions on Industry Applications*, vol. 60, no. 5, pp. 7858–7868, 2024, doi:10.1109/TIA.2024.3427048.
- [5] V. F. Gruner, C. F. Gonçalves, L. Schmitz, D. C. Martins, R. F. Coelho, "Metodologia para Estimção da Distorção Harmônica Total em Inversores Monofásicos Conectados à Rede Elétrica", *Eletrônica de Potência*, vol. 28, no. 4, p. 314–323, Dec. 2023, doi:10.18618/REP.2023.4.0027.
- [6] B. M. T. L. Simbolon, A. Rajagukguk, "Simulation and Analysis of the Use of Dynamic Voltage Resoster (DVR) on the Power Line Against the Effect of Voltage Sag and Voltage Swell", in *2024 4th International Conference on Electrical Engineering and Informatics (ICon EEI)*, pp. 22–27, 2024, doi:10.1109/IConEEI64414.2024.10748235.

- [7] T. Xia, G. Shi, J. Zhou, J. Zhang, X. Fan, L. Chu, "A Novel Transformer-Less Dynamic Voltage Restorer Based on Modified ANPC for Low-Voltage Distribution Network", *IEEE Transactions on Industrial Electronics*, pp. 1–13, 2026, doi:10.1109/TIE.2026.3658685.
- [8] P. Manitha, M. G. Nair, T. Thakur, "Fundamental voltage peak detection controller for series active filters", *Electric Power Systems Research*, vol. 184, p. 106315, 2020, doi:10.1016/j.epsr.2020.106315.
- [9] M. M. Savrun, T. Koroğlu, A. Tan, M. U. Cuma, K. Bayindir, M. Tümay, "Isolated H-bridge DC–DC converter integrated transformerless DVR for power quality improvement", *IET Power Electronics*, vol. 13, no. 5, pp. 920–926, 2020, doi:10.1049/iet-pel.2019.0687.
- [10] S. Leng, A. R. N. M. R. Haque, N. Perera, A. M. Knight, J. Salmon, "Smart Grid Connection of an Induction Motor Using a Three-Phase Floating H-bridge System as a Series Compensator", *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7053–7064, 2016, doi:10.1109/TPEL.2015.2508422.
- [11] M. F. Cunha, C. B. Jacobina, N. B. de Freitas, "Grid-Connected Induction Motor Using a Floating DC-Link Converter Under Unbalanced Voltage Sag", *IEEE Transactions on Industry Applications*, vol. 57, no. 2, pp. 1609–1618, 2021, doi:10.1109/TIA.2021.3050743.
- [12] K. Rajkumar, P. Parthiban, N. Lokesh, "Control of transformerless T-type DVR using multiple delayed signal cancellation PLL under unbalanced and distorted grid condition", *Engineering Science and Technology, an International Journal*, vol. 24, no. 4, pp. 925–935, 2021, doi:10.1016/j.jestech.2021.01.013.
- [13] A. T. S. Soares Santos, C. B. Jacobina, J. T. Cardoso, A. S. Felinto, "Three-Phase Transformerless Series Active Power Filter for Power Quality Improvement", in *2025 Brazilian Power Electronics Conference (COBEP)*, pp. 1–6, 2025, doi:10.1109/COBEP66423.2025.11231265.
- [14] M. Ghodsi, S. M. Barakati, J. M. Guerrero, J. C. Vasquez, "Dynamic voltage restore based on switched-capacitor multilevel inverter with ability to compensate for voltage drop, harmonics, and unbalancing simultaneously", *Electric Power Systems Research*, vol. 207, p. 107826, 2022, doi:10.1016/j.epsr.2022.107826.
- [15] J. Raphael de Souza Martins, D. Alexandria Fernandes, F. Fragoço Costa, M. Beltrão de Rossiter Corrêa, "Compensação De Tensão Trifásica Em Cargas Sensíveis Baseada Em Um Sistema De Controle Repetitivo E Mínimos Quadrados", *Eletrônica de Potência*, vol. 22, no. 3, p. 237–245, Sep. 2017, doi:10.18618/REP.2017.3.2681.
- [16] J. R. de Assis, D. A. Fernandes, M. B. d. R. Corrêa, A. J. Sguarez Filho, F. F. Costa, E. R. da Silva, "Estratégia de Controle Baseada em Componentes de Sequência Aplicada a um Sistema FV-DVR: Falhas Assimétricas", *Eletrônica de Potência*, vol. 29, pp. e202433–e202433, 2024, doi:10.18618/REP.e202433.
- [17] E. Ribeiro, I. Barbi, "Harmonic Voltage Reduction Using a Series Active Filter Under Different Load Conditions", *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1394–1402, 2006, doi:10.1109/TPEL.2006.880265.
- [18] Y. Abouelmahjoub, S. El Beid, H. Abouobaida, A. Chellakhi, "Advanced Nonlinear Control of Single Phase Half Bridge Series Active Power Filter", in *2020 IEEE 2nd International Conference on Electronics, Control, Optimization and Computer Science (ICECOCS)*, pp. 1–5, 2020, doi:10.1109/ICECOCS50124.2020.9314451.
- [19] S. M. Rao, R. J. Satputale, R. K. Keshri, V. B. Borghate, A. Khergade, "Improving DC-Bus Voltage Regulation in Grid Fed EV Fast Charging Station Using MLI Based DVR", *IEEE Transactions on Power Delivery*, vol. 39, no. 4, pp. 2530–2540, 2024, doi:10.1109/TPWRD.2024.3417483.
- [20] T. Madhubabu, A. Anireddy, N. Sahithi, K. S. Krishna Suman, S. Vikas, K. Chenchireddy, "Reduction of Harmonics to Improve Power Quality in Distribution Lines using a Series Active Power Filter", in *2023 7th International Conference on Trends in Electronics and Informatics (ICOEI)*, pp. 123–128, 2023, doi:10.1109/ICOEI56765.2023.10126006.
- [21] A. A. Khan, U. A. Khan, H. F. Ahmed, S. Ahmad, "New Type High-Frequency Transformer Isolated Cascaded AC-AC Converter for DVR to Compensate Sag or Swell in Voltage", in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–6, 2022, doi:10.1109/ECCE50734.2022.9947418.
- [22] M. N. Musarrat, A. Fekih, M. A. Rahman, M. R. Islam, K. M. Muttaqi, "Event-Triggered SMC-Based FRT Approach for DFIG-Based Wind Turbines Equipped With DVR With High-Frequency Isolation", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2661–2671, 2023, doi:10.1109/JESTPE.2022.3233349.
- [23] H. F. Ahmed, M. S. E. Moursi, B. Zahawi, K. A. Hosani, "A High-Frequency Isolated Multilevel Cascaded-Type Bipolar Direct PWM AC–AC Converter for Utility Voltage Compensation", *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 3188–3201, 2021, doi:10.1109/TIA.2020.3021371.
- [24] C. Meyer, R. W. De Doncker, Y. W. Li, F. Blaabjerg, "Optimized Control Strategy for a Medium-Voltage DVR—Theoretical Investigations and Experimental Results", *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2746–2754, 2008, doi:10.1109/TPEL.2008.2002299.
- [25] D. Zargariashar, E. Babaei, M. Sabahi, M. B. Bannae Shariifan, V. Ranjbarizad, "Isolated Single-Phase Buck–Boost AC–AC Converter with Inherent Commutation for Dynamic Voltage Restorer Applications", in *2025 16th International Conference on Electrical and Electronics Engineering (ELECO)*, pp. 1–5, 2025, doi:10.1109/ELECO69582.2025.11329227.
- [26] A. Venugopal, F. R., "Finite Element Study of Core Materials of a Planar Transformer and Comparison of its Electromagnetic Properties with a High Frequency Transformer", *Journal of Engineering Science and Technology Review*, vol. 16, pp. 123–128, 07 2023, doi:10.25103/jestr.163.16.
- [27] N. Santos, M. Chaves, P. Gamboa, A. Cordeiro, N. Santos, S. F. Pinto, "High Frequency Transformers for Solid-State Transformer Applications", *Applied Sciences*, vol. 13, no. 12, 2023, doi:10.3390/app13127262.
- [28] K. Rajkumar, P. Parthiban, "Grid voltage detection method based on a novel adaptive notch filter for control of transformerless dynamic voltage restorer", in *2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC)*, pp. 1–6, 2020, doi:10.1109/STPEC49749.2020.9297670.
- [29] A. Dharmaraj, K. Arumugam, "Transformerless Dynamic Voltage Restorer based on Switched Capacitor Multi Level Inverter and Interleaved Boost Converter", in *2023 International Conference on Smart Systems for applications in Electrical Sciences (ICSSES)*, pp. 1–6, 2023, doi:10.1109/ICSSES58299.2023.10200417.
- [30] C. Tu, Q. Guo, F. Jiang, H. Wang, Z. Shuai, "A Comprehensive Study to Mitigate Voltage Sags and Phase Jumps Using a Dynamic Voltage Restorer", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1490–1502, 2020, doi:10.1109/JESTPE.2019.2914308.
- [31] A. S. Felinto, C. B. Jacobina, E. L. L. Fabrício, R. P. d. Lacerda, "Three-Phase Four-Wire AC–DC–AC Converter With Shared Legs", *IEEE Transactions on Industry Applications*, vol. 57, no. 4, pp. 3911–3922, 2021, doi:10.1109/TIA.2021.3081403.
- [32] E. Gallo, D. Biadene, I. Toigo, T. Caldognetto, "Ripple Reduction of Active Split DC-Link 4-Wire Inverters by Phase-Shifted Multi-Carrier Modulation", *IEEE Open Journal of Power Electronics*, vol. 5, pp. 864–872, 2024, doi:10.1109/OJPEL.2024.3409065.
- [33] U. Manandhar, X. Zhang, H. B. Gooi, B. Wang, F. Fan, "Active DC-link balancing and voltage regulation using a three-level converter for split-link four-wire system", *IET Power Electronics*, vol. 13, no. 12, pp. 2424–2431, 2020, doi:10.1049/iet-pel.2020.0067.
- [34] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, A. F. Souza, "Comparison of Three Single-Phase PLL Algorithms for UPS Applications", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 2923–2932, 2008, doi:10.1109/TIE.2008.924205.
- [35] M. V. M. Rodrigues, N. d. Silva, "Controlador Multimodais para Inversor Monofásico e Controle de Chave Estática de Transferência Aplicados em Fontes Ininterruptas de Energia", *Eletrônica de Potência*, vol. 21, no. 1, p. 52–62, Mar. 2016, doi:10.18618/REP.2016.1.2582.
- [36] C. Knaesel, L. Michels, A. L. Batschauer, M. Mezaroba, "Conversor CC-CC Isolado de Alto Ganho para Integração em Módulos Fotovoltaicos", *Eletrônica de Potência*, vol. 24, no. 4, p. 482–493, Dec. 2019, doi:10.18618/REP.2019.4.0042.
- [37] F. T. Carneiro, I. Barbi, "Análise, Projeto e Implementação de um Conversor com Transferência de Energia Sem Fio para Carregadores de Baterias de Veículos Elétricos", *Eletrônica de Potência*, vol. 26, no. 3, p. 260–267, Sep. 2021, doi:10.18618/REP.2021.3.0003.

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