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Towards Scalable High-Voltage Battery Packs: A Modular Architecture Enabled by Dual Active Bridge Converters

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ABSTRACT The growing adoption of Battery Energy Storage Systems (BESS) has increased the demand for scalable architectures that convert low-voltage (LV) battery packs into high-voltage (HV) configurations. However, series connection of LV packs is limited by the voltage ratings of their embedded Battery Management System (BMS) and protection circuitry. This paper proposes a modular Smart Battery architecture based on isolated Dual Active Bridge (DAB) DC–DC converters, which provide galvanic isolation, bidirectional power flow and independent voltage regulation for each LV battery module, allowing commercial LV packs to be integrated into an HV DC-link without hardware modifications. A master BMS controller performs State of Charge (SoC) balancing by adjusting the individual DAB output-voltage references through a proportional balancing law, while local proportional–integral (PI) controllers regulate the module output voltages. Functional performance was evaluated through PLECS simulations and controller hardware-in-the-loop (C-HIL) tests with four modules forming a 192-V dc link. The results demonstrate dc-link regulation under load transients and SoC equalization under the evaluated initial imbalances and capacity mismatches, supporting the coordinated-control implementation on the physical DSP against the real-time power-stage model.

KEYWORDS Battery Energy Storage Systems (BESS), Dual Active Bridge (DAB), High-voltage battery module.

I. INTRODUCTION

The increasing deployment of renewable energy sources and the electrification of transportation and industrial systems have intensified the demand for Battery Energy Storage Systems (BESS) capable of providing flexible energy management, mitigating renewable generation intermittency, and improving power system reliability [1], [2]. In this context, BESS must accommodate a wide range of power and voltage levels, from residential installations based on low-voltage (LV) battery packs to high-power applications requiring high-voltage (HV) dc buses. Commercial LV battery packs, typically rated at approximately 48 V, offer advantages in terms of availability and integration into distributed energy systems [3]–[6]. However, their direct interconnection in series to obtain higher dc-link voltages is generally constrained by the voltage ratings and grounding arrangements of their embedded battery management systems (BMS), sensing circuits, communication interfaces, and protection devices. In contrast, HV battery systems, commonly operating from 200 V to 1500 V, require electrical architectures capable of combining multiple battery modules while ensuring adequate voltage regulation, protection, and coordinated energy utilization [7]–[9].

The smart battery concept has emerged as a modular alternative to conventional battery systems by integrating power conversion and local control functions into individual battery modules [10]. Previous studies have investigated module-integrated and distributed battery architectures for second-life batteries and energy storage applications [11], [12], while related approaches have addressed distributed battery power electronics and active battery management [13]–[15]. Nevertheless, the vast majority of existing studies have focused on non-isolated dc-dc converter topologies because of their reduced complexity and lower implementation cost [16]. Although patents applying the smart battery concept with isolated dc–dc converters have been reported [17], [18], they provide limited technical detail regarding the formation of an HV dc-link from LV battery packs and the control strategy required to coordinate power sharing and SoC balancing among the modules.

Among the isolated bidirectional dc–dc converter topologies, the Dual Active Bridge (DAB) converter has become one of the most widely adopted solutions for battery energy storage applications due to its high efficiency, galvanic isolation, bidirectional power flow capability and high power density [19]–[22]. These features make the DAB particularly

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suitable for interfacing battery modules with dc buses operating at different voltage levels while maintaining electrical isolation between individual modules and the common output bus. These characteristics make the DAB an attractive building block for modular battery architectures enabling each battery module to be independently controlled while contributing to the overall high-voltage dc-link.

Based on this background, this paper proposes a modular smart battery architecture where each commercial LV battery pack is interfaced with the HV dc link through an DAB converter. The converter outputs are connected in series, so that the total dc-link voltage is obtained from the sum of the individual module output voltages. Meanwhile, the galvanic isolation between each battery input and its corresponding converter output allows the battery-side electronics to remain referenced to the LV battery terminals, avoiding the need to expose the original BMS and protection circuitry to the cumulative HV dc-link potential. The DAB converters also provide bidirectional power transfer, enabling the architecture to accommodate charging and discharging operation. Unlike an approach that relies only on local voltage regulation, the proposed supervisory strategy uses the SoC information provided by the individual BMSs to modify the voltage reference of each DAB module. This adjustment redistributes the modules power contributions, leading to SoC equalization while maintaining regulation of the overall dc-link voltage. The topology for the proposed solution can be seen in Fig. 1.

The distinction between the proposed approach and the related literature is summarized in Table 1. The novelty of this work lies in combining isolated DAB modules with series-connected outputs to establish an HV dc link, while maintaining the LV reference of the battery-side electronics and implementing a supervisory SoC balancing strategy. This integrated architecture enables the use of commercially available LV battery packs in HV BESS applications without modifying their original BMS. Furthermore, this work extends the preliminary conference publication in [23] by presenting the converter and controller design procedures and evaluating the complete control strategy through Controller Hardware-in-the-Loop (C-HIL) experiments, in addition to PLECS simulations. The validation considers dc-link regulation under load transients and SoC balancing under different initial SoC conditions and battery-capacity mismatches.

The main contributions of this paper are summarized as follows:

- A modular HV battery architecture based on isolated DAB converters, in which the series-connected converter outputs establish the HV dc link while preserving the LV electrical reference of the embedded battery electronics.
- A supervisory control strategy that adjusts the individual DAB output-voltage references according to the battery SoCs, coordinating power sharing and SoC balancing without compromising the regulation of the common dc-link voltage under the evaluated operating conditions.
- Converter and controller design procedures, followed by validation through PLECS simulations and C-HIL experiments under load transients, initial SoC imbalances, and battery-capacity mismatches.

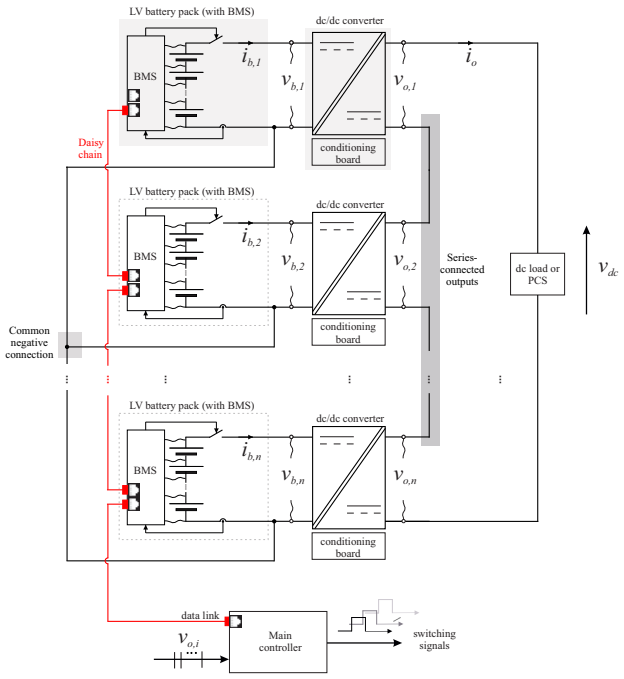


FIGURE 1. System architecture investigated in this work.

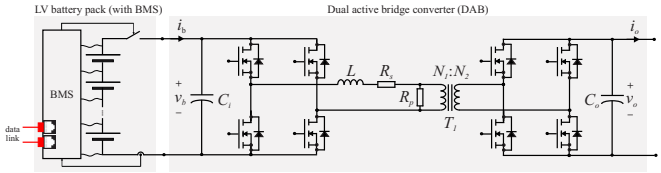


FIGURE 2. Low voltage battery pack with integrated BMS connected to the the Dual Active Bridge converter.

The remainder of this paper is organized as follows. Section II presents the proposed smart battery architecture, the converter design and the control strategy. Section III describes the mathematical modeling and parameters values. Section IV presents the simulation results. Section V reports the C-HIL results. Finally, Section VI summarizes the main conclusions and discusses future research directions.

II. METHODOLOGY

A. System Architecture

The proposed system architecture is shown in Fig. 1. The system consists of three main groups: the low-voltage battery packs with local BMS units; the isolated dc-dc converters and the main controller. The battery terminals are connected

TABLE 1. Qualitative comparison of existing battery architectures and DAB-based systems with the proposed architecture.

Reference	Isolated DAB converter	Series-connected outputs for HV bus	LV to HV battery pack	SoC balancing	Experimental or C-HIL validation
[11], [12]	−	+	+	++	++
[13]	−	++	+	++	−
[14]	−	+	+	++	−
[15]	−	++	++	++	+
[16]	−	+	++	−	++
[17]	+	++	++	−	−
[18]	++	−	+	−	+
[19]	−	+	++	++	++
[20], [21]	++	−	−	−	++
[22]	++	−	−	−	−
[23]	++	++	++	++	−
This work	++	++	++	++	+

++: explicitly and substantially addressed; +: partially addressed or related functionality; −: not addressed or not reported in the reference.

to the input of each converter. The converter outputs are then connected in series to form an HV dc-link in the output.

The galvanic isolation provided by the DAB converters electrically decouples the battery-side terminals from the series-connected converter outputs and enables all battery negative terminals to share a common reference point, as highlighted in Fig. 1. Consequently, the communication interfaces and protection devices remain subjected only to the voltage of an individual low-voltage battery pack, despite the formation of a high-voltage dc-link at the converter outputs. This feature allows existing low-voltage battery packs, including their embedded BMS and protection circuits, to be integrated into a high-voltage energy storage system without requiring modifications to the original low-voltage electronics or additional isolation within the battery-side communication and sensing circuits. The converter outputs, however, float at cumulative string potentials. With the string negative referenced to the common battery-side reference, module i spans approximately $\sum_{k<i} v_{o,k}$ to $\sum_{k\leq i} v_{o,k}$. Transformer barriers and interfaces to floating circuitry must consequently be designed for working and transient voltages that can approach the full dc-link voltage, even though the differential voltage processed by each module remains at module level.

Each battery pack is assumed to provide its SoC information to the main controller through a daisy-chain communication network. By receiving the SoC data from each battery pack, together with the corresponding converter output-voltage measurements, the main controller adjusts the individual DAB output-voltage references, thereby regulating the power processed by each converter and redistributing the power demand among the battery packs. This approach allows SoC equalization while maintaining the required dc-link voltage. Fig. 3 illustrates the balancing and individual voltage-control structure, which is described in detail in Section II.C.

Because all outputs carry the same current, $P_i = v_{o,i} i_{\mathrm{o}}$, these voltage adjustments directly determine each module power contribution. For common charging/discharging operation, equal balancing gains, and unsaturated commands, the corrections sum to zero and preserve the aggregate voltage reference.

This arrangement allows the dc-link voltage to increase with the number of modules: $v_{\mathrm{dc}} = \sum_i v_{o,i}$, reaching $N v_{o,\mathrm{nom}}$ for N identical nominal outputs. At the same current rating, the aggregate nominal power capability also increases proportionally with N. Although the local PI structure is retained, computing the mean SoC and individual corrections requires $O(N)$ operations and data per supervisory update. Centralized execution of the local loops likewise results in an $O(N)$ workload. Moreover, the daisy-chain refresh time increases with the transmitted data: for B bits per module and an effective rate r, a sequential update requires at least NB/r, excluding additional delays. Thus, the controller and communication network must support the update rates required by the enlarged string.

The usable system power also depends on power-sharing requirements. During discharge, converters connected to higher-SoC batteries may process above-average power, meaning that sizing based solely on $|P_{\mathrm{tot}}|/N$ provides no balancing reserve. Additional margin is also required for post-fault operation. After isolating and bypassing a failed module, maintaining the same total power with $N-1$ modules increases their average loading by $N/(N-1)$. For instance, in a four-module system, this corresponds to a 33.33% increase. For m active modules sharing nonzero power in the same direction, define $\beta_m = m \max_i |P_i|/|P_{\mathrm{tot}}| \geq 1$. Identical converter ratings must then satisfy $P_{\mathrm{rated}} \geq \beta_m |P_{\mathrm{tot}}|/m$ over the intended normal and post-fault operating conditions. This requirement accounts for unequal power sharing during balancing; otherwise, total power must be limited to the available module capacity. Furthermore, maintaining the original dc-link voltage requires higher output voltages from the remaining converters, whereas accepting a lower bus voltage increases the current required for the same power. These trade-offs must be considered alongside battery operating limits and converter voltage/current ratings.

Increasing the number of converters also increases the opportunities for module failure, even when individual module reliability remains unchanged. Without a recovery path, a failure that interrupts the series current can stop the entire string. Fault isolation and an output bypass allow the defective module to be removed while preserving the

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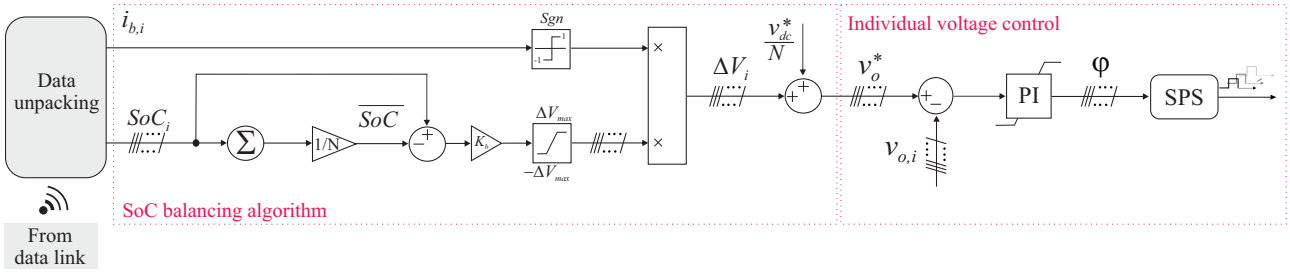


FIGURE 3. System with master balancing and local controller. *Remark:* Parallel bars on a signal line indicate the transmission of multiple signals.

current path, but do not inherently restore the original voltage and power capability. Continued operation therefore depends on the available voltage and power margins, as well as successful fault detection, isolation, and bypass. When sufficient margins exist, the controller can redistribute the references among healthy modules; otherwise, reduced power and, if acceptable to the load, a lower dc-link voltage are required. Hence, module sizing and fault handling must be considered together when scaling the string. The present tests demonstrate coordinated control under normal operating conditions, rather than post-fault recovery.

B. DAB converter design

In this paper, the DAB converters operate using the single-phase-shift (SPS) modulation technique, with both H-bridges driven at a fixed duty cycle of 50%. Under such conditions, the transferred power is controlled exclusively by the phase shift between the primary and secondary side bridge voltages [24]. In this case, the converter output power is given by:

$$P = \frac{n v_b v_o}{2\pi^2 f_s L}\varphi(\pi - |\varphi|), \tag{1}$$

where v_b is the battery voltage, v_o is the DAB output voltage, n is the primary-to-secondary transformer turns ratio N_1/N_2, φ is the phase-shift angle in radians, f_s is the switching frequency and L is the equivalent series inductance referred to the primary side, comprising the transformer leakage inductance and any external series inductance, if present. The equation shows that magnitude and direction of the transferred power are determined by phase difference between the primary and secondary voltages. In addition, maximum power magnitude is achieved when $\varphi = \pi/2$. A monotonic relationship between the transferred power and the phase-shift angle is obtained for phase-shift angles ranging from $-\pi/2$ to $\pi/2$. In general, increasing phase-shift magnitude increases the current available during the switching transitions and can extend the Zero-Voltage Switching (ZVS) operating range [25]. In practice, the operating phase shift is selected by considering power-transfer requirements, RMS current, conduction and switching losses, reactive power, and ZVS constraints [25], [26]. The maximum of the ideal SPS power characteristic at $|\varphi| = \pi/2$ does not, by itself, define a closed-loop stability limit.

By solving (1) for L and φ, respectively, yields:

$$L = \frac{n v_b v_{out}\varphi(\pi - |\varphi|)}{2\pi^2 f_s P}, \tag{2}$$

$$\varphi = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_s L|P|}{n v_b v_o}}\right)\mathrm{sgn}(P). \tag{3}$$

According to the phase-shift convention adopted in this work, positive values of φ result in power flow from the primary to the secondary side, while negative values reverse the direction.

Following the ideal SPS boundaries in [25], let $d = nv_o/v_b$ and $\delta = |\varphi|$. Assuming steady-state half-wave current symmetry, ideal switches, and negligible magnetizing current, parasitic capacitances, and dead-time distortion, the primary and secondary switching-current polarity conditions are $\delta > \pi(1 - 1/d)/2$ and $\delta > \pi(1 - d)/2$, respectively. Thus, both bridges have favorable polarity when

$$|\varphi| > \delta_{\lim}(d) = \frac{\pi}{2}\left[1 - \min\left(d, \frac{1}{d}\right)\right]. \tag{4}$$

These ideal boundaries are symmetric for forward and reverse power flow. On the monotonic branch, $0 \le |\varphi| \le \pi/2$, the corresponding power boundary is

$$P_{\lim} = \frac{n v_b v_o}{2\pi^2 f_s L}\delta_{\lim}(\pi - \delta_{\lim}). \tag{5}$$

Both polarity conditions hold for $|P| > P_{\lim}$; equality gives zero current at a relevant transition. These are necessary conditions within the ideal model, not a guarantee of physical ZVS: actual switching also requires sufficient current to charge and discharge the nonlinear semiconductor output capacitances within an appropriate dead time [25]. In particular, $d = 1$ gives a zero ideal boundary, but does not establish ZVS at zero power.

The capacitors represented in Fig. 2 also perform an important function in filtering the switching-frequency components and determining the converter transient response. The input capacitor is designed following the voltage-ripple criterion and assuming a triangular waveform for the capacitor current. Accordingly [27]:

$$C_i = \frac{i_b}{8 f_s \Delta v_{in}}, \tag{6}$$

where i_b is the current flowing through the battery, Δv_{in} is the peak-to-peak input-voltage ripple, expressed in volts.

Similarly, the output capacitor C_o could, in principle, be designed using the same ripple criterion adopted for the input capacitor C_i. However, unlike C_i, the output capacitor also provides short-term energy buffering and limits the output-voltage deviation of each DAB module during load transients. Therefore, C_o is designed according to the first-order charge-balance criterion given in (7):

$$C_o > \frac{\Delta I \cdot \Delta t}{\Delta V}, \tag{7}$$

where ΔI is the maximum output-current variation, Δt represents the assumed response time of the output-voltage controller, and ΔV is the maximum allowable module output-voltage deviation caused by the load transient. During a full power-flow reversal from $+I_{nom}$ to $-I_{nom}$, $\Delta I = 2I_{nom}$ where I_{nom} is the nominal output-current magnitude. The response time is approximately estimated as $\Delta t \approx 1/f_c$, where f_c is the voltage-control-loop crossover frequency. This criterion generally results in larger output capacitance values than those obtained using the conventional voltage-ripple criterion, since it assumes that the capacitor supplies the entire current variation during Δt. However, because it provides a more conservative estimate, it is adopted for the design of C_o in this work.

In the simulations and C-HIL experiments, the parasitic losses of the DAB transformer are modeled by two equivalent resistances referred to the primary side, as shown in Fig. 2. The resistances are determined based on the total transformer losses at the maximum-efficiency operating point, where the copper and core losses are assumed to be equal. Accordingly, the equivalent resistances are calculated as:

$$R_{\mathrm{s}} = \frac{P_l}{2I_1^2}, \qquad R_{\mathrm{p}} = \frac{2V_1^2}{P_l}, \tag{8}$$

where P_l denotes the total transformer losses, and I_1 and V_1 are the primary-side RMS current and voltage, respectively, at the maximum-efficiency operating point.

C. Control Strategy

Fig. 3 illustrates the control algorithm implemented in the main controller. It is composed of two main control loops: SoC balancing and individual output-voltage control.

The SoC balancing algorithm is implemented following the approaches proposed in [13]–[15], and [28]. After receiving the SoC information from all battery packs through the communication network, the average state of charge $\overline{SoC}$ is computed as:

$$\overline{\mathrm{SoC}} = \frac{1}{N}\sum_{i=1}^{N} \mathrm{SoC}_i, \tag{9}$$

where N is the number of battery–converter modules.

The difference between the individual battery SoC (SoC_i) and the average value is multiplied by the balancing gain K_b, which defines the magnitude of the balancing action and consequently affects the balancing speed.

The transient behavior of the adopted balancing scheme has been evaluated using simplified analytical models developed in [29]. These models show that the balancing dynamics exhibit a first-order response, with a time constant inversely proportional to the magnitude of K_b.

Under steady-state conditions, the output-voltage references required to achieve equal SoC variation rates in batteries with different capacities are given by:

$$v_{o,i} = \frac{v_{dc}^*}{N}\frac{Q_i}{\overline{Q}}, \qquad \overline{Q} = \frac{1}{N}\sum_{i=1}^{N} Q_i, \tag{10}$$

where Q_i is the capacity of battery i. This relationship indicates that capacity mismatches affect the voltage references required for balanced operation. In other words, the converters must provide sufficient voltage and power margins to accommodate the expected capacity mismatch. An additional power margin may also be considered for redundancy, as previously discussed.

Since a proportional controller is adopted, a nonzero steady-state SoC error is expected in the presence of battery capacity mismatches. This error can be estimated as [30]:

$$\Delta\mathrm{SoC}_{i,\mathrm{ss}} = \frac{v_{dc}^*}{NK_b}\left(\frac{Q_i}{\overline{Q}} - 1\right), \tag{11}$$

which indicates that increasing the magnitude of the balancing gain reduces the steady-state SoC error. However, the gain cannot be increased without considering the operating limits of the converters. An excessively aggressive balancing action may cause transient converter saturation. Under these conditions, the sum of the converter output voltages may temporarily deviate from the dc-link voltage reference, resulting in dc-bus voltage variations. This interaction is analyzed in detail in [31]. Therefore, the maximum balancing gain must be selected by considering both the available voltage margin and the maximum expected SoC deviation. Accordingly,

$$K_b = -\frac{\Delta V_{\max}}{|\Delta SoC_{\max}|}, \tag{12}$$

where $|\Delta SoC_{\max}|$ is the maximum absolute deviation of an individual battery SoC from the average SoC for which the maximum voltage correction $\Delta V_{\max}$ is applied. The negative sign follows from the adopted control convention. To prevent excessive voltage deviations, the compensation signal is limited to $\pm\Delta V_{\max}$.

The battery output current $i_{b,i}$ determines the direction of the balancing action. During discharge, batteries with higher estimated SoC receive higher output-voltage references and therefore supply more power. During charging, the action is reversed so that batteries with lower estimated SoC receive more charging power. This action seeks to reduce SoC differences within the converter operating limits.

SoC estimation errors can affect the balancing action. If ε_i is the estimation error of module i, the perturbation in its deviation from the average SoC is $\bar{\varepsilon} - \varepsilon_i$, where $\bar{\varepsilon}$ is

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the average error. Before saturation, the resulting voltage-reference perturbation has magnitude $|K_b||\bar{\varepsilon} - \varepsilon_i|$.

For four modules with errors bounded by ± 1 percentage point, this magnitude is at most $1.5|K_b|$ volts when K_b is expressed in volts per percentage point. Common errors cancel from the balancing correction, whereas differential errors can cause incorrect power sharing.

The voltage compensation term ΔV_i is added to the nominal converter voltage reference. As the converter outputs are connected in series, each module is assigned a nominal voltage reference equal to v_{dc}^*/N. Therefore, the individual voltage reference becomes $v_{o,i}^* = v_{dc}^*/N + \Delta V_i$. Since the sum of the SoC deviations from the average value is zero, the voltage-reference corrections also sum to zero under unsaturated operating conditions. Thus, the balancing action does not modify the total dc-link voltage reference as long as none of the compensation signals is saturated.

Then, going into the individual voltage control loop, the difference between the individual voltage reference $v_{o,i}^*$ and the measured output voltage $v_{o,i}$ is processed by the PI controller to determine the phase-shift angle φ.

With the DAB parameters (φ, L, C_i and C_o) defined, the PI controller can be designed following the procedure proposed in [32]. The resulting small-signal control-to-output transfer function, linearized around the operating point $\varphi = \Phi$, is given by:

$$G_p(s) = \frac{\widetilde{v}_o(s)}{\widetilde{\varphi}(s)} = \frac{b(\Phi)}{s + a}. \tag{13}$$

where

$$a = \frac{1}{R_{load} C_o}, \tag{14}$$

$$b(\Phi) = \frac{n v_b (\pi - 2\Phi)}{2\pi^2 f_s L C_o}. \tag{15}$$

Using the pole placement method, the PI controller gains K_p and K_i are calculated as follows:

$$K_p = \frac{2\pi f_c}{b(\Phi)}, \tag{16}$$

$$K_i = K_p a, \tag{17}$$

where f_c represents the crossover frequency. Since the control is implemented digitally and the controller is updated once per switching period, the computation and modulation processes introduce a delay. To limit the influence of this delay, the crossover frequency is set to $f_c = f_s/20$.

Regarding the control strategy, the following aspects should be highlighted:

- The local voltage-control loops operate on a much faster timescale than the outer SoC-balancing loop, supporting reference tracking with limited dynamic interaction under normal operating conditions. This assumption requires stable local loops and sufficient voltage and power margins, since converter saturation may affect dc-link regulation and balancing convergence.
- The architecture relies on SoC estimates supplied by local BMS units. Their influence on the voltage references is assessed analytically above. The reported simulation and C-HIL tests use battery models and do not evaluate physical BMS estimation algorithms or impose SoC estimation errors.
- Balancing the SoC can contribute to a more uniform utilization of the battery modules, potentially promoting a more balanced evolution of their state of health (SoH), enhancing functional safety, and increasing energy extraction and overall battery pack utilization. The proposed strategy does not explicitly account for aging, thermal dynamics, or SoH differences, which could be incorporated into future extensions to further improve battery utilization and operational reliability.

III. CASE STUDY

The battery model was developed based on the experimental characterization of the UPLFP48-20E battery manufactured by Unicoba. The characterization was performed using an ITECH IT8511A+ electronic load under a constant discharge current of 3 A. The resulting terminal voltage discharge curve is presented in Fig.4. Battery parameters are summarized in Tab.2.

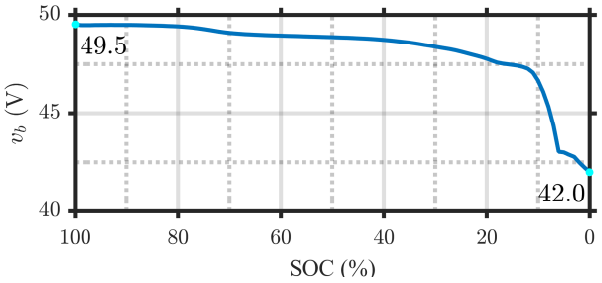


FIGURE 4. Measured battery discharging curve.

TABLE 2. Battery Parameters

Parameter	Value
Intrinsic resistance (R_e)	0,052 Ω
Nominal voltage (v_b)	48 V
Minimum voltage (v_{bmin})	42 V
Maximum voltage (v_{bmax})	49.5 V
Capacity (C)	20 Ah
C rate	1C
Power (P)	1 kW

The converter rated power was selected as 1 kW, which is approximately equal to the power delivered by the 48 V, 20 Ah battery pack at a $1C$ discharge rate. The converter parameters are shown in Tab. 3.

TABLE 3. DAB Parameters and system control gains

Parameter	Value
Nominal DAB output voltage (v_o)	48 V
Switching Frequency (f_s)	25 kHz
Crossover Frequency (f_c)	1.25 kHz
Primary-to-Secondary turns ratio (n)	1
Transformer Leakage Inductance (L)	6.4 μH
Transformer Series Resistance (R_s)	8.9mΩ
Transformer Parallel Resistance (R_p)	658 Ω
Input Capacitance (C_i)	217 μF
Output Capacitance (C_o)	10 mF
Nominal phase shift (Φ)	30°
Proportional Gain (K_p)	2.47 V^{-1}
Integral Gain (K_i)	107.1 $(V{\cdot}s)^{-1}$
Balancing gain magnitude ($\lvert K_b \rvert$)	0.234 V/%

The switching frequency was set to 25 kHz, a typical value for practical DAB converters that is also feasible in the Typhoon HIL 606, the platform used to validate the proposed system. The control-loop crossover frequency was set to one-twentieth of the switching frequency. The transformer primary-to-secondary turns ratio was set to $n = N_1/N_2 = 1$ for simplicity.

The transformer equivalent inductance L was estimated by using (2), assuming the rated power, rated voltage, and a phase-shift angle of $\varphi = \Phi = 30°$. The input capacitor C_i was sized according to Eq. (6), assuming the rated current and an input voltage ripple of 1%. The output capacitor was designed considering a maximum current variation of $\Delta I = 2I_{\text{nom}} = 2 \times 20$ A, where 20 A corresponds to the nominal C-rate. The transient response time was roughly estimated as $\Delta t \approx 1/f_c = 0.8$ ms, and the maximum allowable output voltage deviation was set to 10% of the nominal voltage, i.e., $\Delta V = 4.8$ V. Applying these values to the output capacitor sizing equation yields a minimum required capacitance of 6.67 mF. Since the analytical design neglects capacitor tolerances and parasitic effects, this value should be regarded as an approximation. Therefore, a 10 mF output capacitor was selected to provide an adequate design margin.

Fig. 5 represents the plot from output power in function of the phase shift angle, shown in (1). It is represented three different cases. Firstly, Case 1 represents the nominal phase shift angle curve, that can be found by applying the values from Tab. 2 and from Tab. 3 for the f_s, L, P, n, v_b, v_o into (3). The nominal phase shift angle found is 30°. This value is aligned with the Fig. 2 from [25] each shows that at 30° the system can operate in a condition sufficient for transient operation and bidirectional power regulation. Case 2 and Case 3 were simulated to ensure that the phase-shift controller does not operate close to its boundary. In Case 2, the input voltage was set to the maximum battery voltage, $v_{in} = v_{bmax} = 49.5\,V$, while the output voltage was defined as the maximum output voltage, $v_{out} = v_{omax} = v_{bnom} + \Delta V_{max}$. In Case 3, the input voltage was set to the minimum battery voltage, $v_{in} = v_{bmin} = 42$ V, whereas the output voltage was defined as the minimum output voltage, $v_{out} = v_{o,\min} = v_{bnom} - \Delta V_{max}$, where ΔV_{max} is defined as a maximum of 5% of the $V_b = 48$ V. So, the full phase shift angle values vary between 27° to 38° for positive power and symmetrically to negative power −38° to −27°, as shown in Fig. 5.

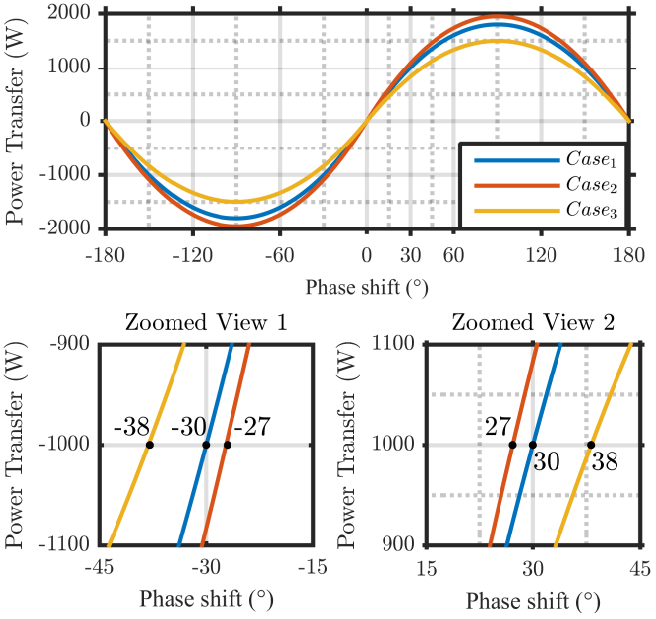


FIGURE 5. DAB power output based on phase shift angle with focus on designed nominal power of -1000W and +1000W respectively

Fig. 6 evaluates these conditions using the parameters in Tab. 3, $v_b \in [42, 49.5]$ V, and the ±5% steady-state output-voltage interval $v_o \in [45.6, 50.4]$ V. All independent combinations, including crossed voltage extremes, are considered. The entire calculated ±1 kW envelope satisfies both polarity conditions, with $|\varphi| \approx 27.2°$–$38.2°$. The largest mismatch, $v_b = 42$ V and $v_o = 50.4$ V ($d = 1.2$), gives $\delta_{\text{lim}} = 15°$ and $P_{\text{lim}} \approx 505$ W per module; the rated-power angle is 33.4°. At $v_o = 48$ V, the boundaries are approximately 369 W and 111 W for the minimum and maximum battery voltages, respectively.

Consequently, favorable polarity holds at rated power in either direction, but fails at some light-load points; full-range ZVS cannot be assumed. For $d > 1$, the primary bridge sets the limiting angle, whereas for $d < 1$ the secondary bridge does so. Since balancing changes both $d_i = nv_{o,i}/v_{b,i}$ and $P_i = v_{o,i}I_{\text{dc}}$, the criterion must be assessed per module. The shaded envelope represents calculated steady-state points, not transient trajectories. Output-voltage excursions outside the stated interval are excluded, and neither this analysis nor the C-HIL results establishes device-level ZVS, switching losses, or efficiency.

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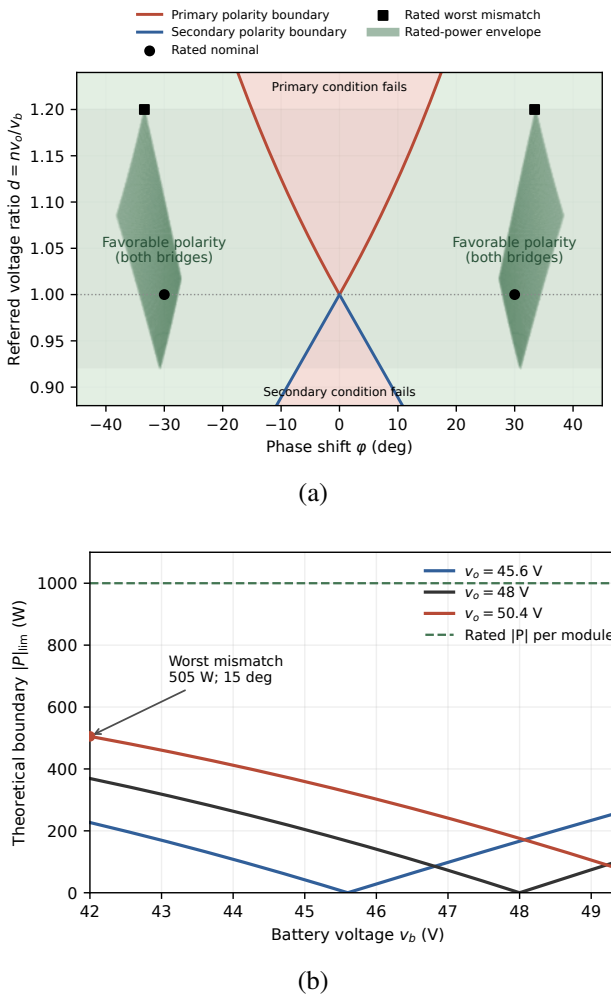


FIGURE 6. Steady-state ideal model: favorable current polarity does not guarantee device-level ZVS. Theoretical SPS current-polarity conditions for ZVS. (a) Primary and secondary boundaries and calculated operating envelope at ± 1 kW per module. (b) Power magnitude at the boundary for three output voltages. The analysis assumes $n = 1$, $f_s = 25$ kHz, $L = 6.4\ \mu$H, $v_b \in [42, 49.5]$ V, and $v_o \in [45.6, 50.4]$ V.

Finally, the control gains K_p, K_i are calculated. The battery and DAB parameters from Tab. 2 and Tab. 3 are first substituted into Equations (14) and (15) and the resulting values are then used in Equations (16) and (17). Therefore, $K_p = 2.47\,V^{-1}$ and $K_i = 107.1\,(V \cdot s)^{-1}$.

Applying the nominal parameters the transfer function from (13) can be written as

$$G_p(s) = \frac{3183.1}{s + 43.4}. \tag{18}$$

However, this equation is valid only for the nominal output power and the corresponding phase-shift angle. To evaluate the behavior of the designed controller over the entire operating range, a family of transfer functions was considered having different output power (P). For each condition, the equivalent load resistance was estimated according to $R_{load} = v_o^2/P$. The corresponding phase-shift angle was then calculated based on (3), resulting in different values of the coefficients a and b of the transfer function in (13). Therefore, each operating point yields a different plant model.

Fig. 7 presents the closed-loop step responses obtained for output powers ranging from -1000 W to 1000 W. Although the plant dynamics vary with the operating point, all responses remain stable and exhibit similar transient behavior, demonstrating that the controller designed using the nominal model provides satisfactory response over the entire operating range.

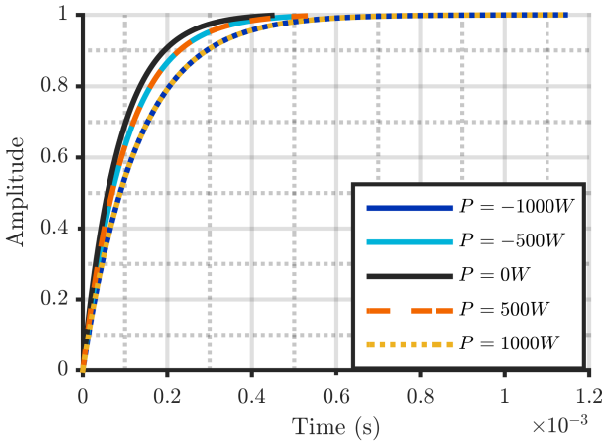


FIGURE 7. System closed feedback response to a Step signal over operating power output

The balancing algorithm is evaluated under two scenarios. The first scenario considers different initial SoCs and identical battery capacities, whereas the second scenario considers different initial SoCs and different battery capacities, as shown in Tab. 4.

TABLE 4. Battery capacities and individual SoCs for the analyzed scenarios.

	Simulation		C-HIL	
Parameter	**Scenario 1**	**Scenario 2**	**Scenario 1**	**Scenario 2**
SoC_1	100%	100%	60%	60%
SoC_2	93%	93%	53%	53%
SoC_3	86%	86%	46%	46%
SoC_4	80%	80%	40%	40%
C_1	200 mAh	200 mAh	2.0 Ah	2.0 Ah
C_2	200 mAh	190 mAh	2.0 Ah	1.9 Ah
C_3	200 mAh	180 mAh	2.0 Ah	1.8 Ah
C_4	200 mAh	170 mAh	2.0 Ah	1.7 Ah

The maximum voltage-reference correction $\Delta V_{\max}$ was selected as 5% of the nominal module voltage, corresponding to 2.4 V. The initial average SoC is $(100+93+86+80)/4 = 89.75\%$, and the maximum initial deviation from the average value is $|\Delta \mathrm{SoC}_{\max}| = |100 - 89.75| = 10.25\%$. Thus, the balancing gain magnitude is $|K_b| = \Delta V_{\max}/|\Delta \mathrm{SoC}_{\max}| =$

$2.4/10.25 \approx 0.234$ V per percentage point. Under the sign convention adopted in (12), the corresponding gain is negative.

The adopted system was initially evaluated through simulations in PLECS environment. In this case, voltage reference changes and load steps are used to evaluate reference tracking and disturbance rejection of the proposed control. Secondly, the balancing control scheme was evaluated, considering 2 different scenarios of battery capacities and initial states of charge. The simulated values are shown in Tab. 4. Due to the long time required to simulate the balancing process, the battery capacities were reduced by a factor of 100, while the remaining electrical and control parameters were kept unchanged. Consequently, the balancing dynamics are accelerated by the same factor, and the reported balancing time does not represent the physical balancing time of the original 20 Ah battery packs.

The PLECS simulation results were later one validated in a HIL environment by using the Typhoon HIL 606 connected to the DSP 180 interface board, as shown in the Fig. 8.

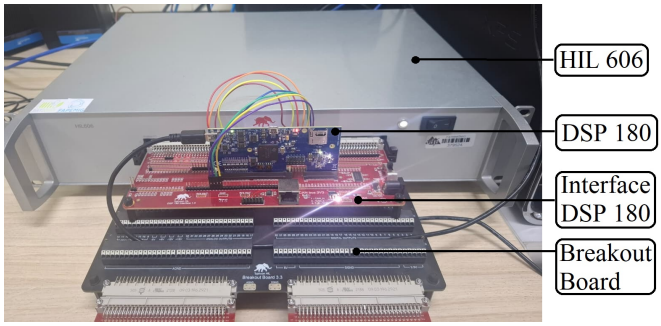


FIGURE 8. Typhoon HIL 606 connected to the DSP board

With respect to load modeling, a controlled current source is used as the load in the PLECS simulations. However, this approach led to numerical conditioning issues in the HIL implementation. Therefore, in the HIL model, the load was represented by a constant resistance of 9.6 Ω with an anti-parallel controlled current source. At the nominal dc-link voltage of 192 V, the resistive load draws 20 A. The current source is controlled by a pulsed reference ranging from 0 to 40 A, allowing the net load current to be varied and its direction to be reversed, thereby emulating both charging and discharging conditions while improving numerical conditioning.

IV. SIMULATION RESULTS

A. Local Control

Fig. 9 presents the simulation results obtained to validate the proposed control strategy. The individual output-voltage reference was set to $v^*_{o,i} = 48$ V for each converter module. With four converter outputs connected in series, the resulting dc-link voltage reference is $v^*_{dc} = 192$ V. As shown in Fig. 9(a) and Fig. 9(b), both the individual output voltages and the overall dc-link voltage accurately track their reference values, exhibiting negligible steady state error.

Moreover, a load transient was applied by changing the output current from its maximum discharge value to the minimum value at $t = 0.5$ s, and restoring the initial operating condition at $t = 1.0$ s, as illustrated in Fig. 9(c). During both transients, the dc-link voltage exhibits an overshoot and an undershoot of approximately 10%, as shown in Fig. 9(b). The corresponding phase-shift angles, shown in Fig. 9(d), are automatically adjusted to regulate the transferred power according to the load demand while maintaining stable operation. These results demonstrate that the proposed control strategy provides accurate voltage regulation, reliable operation under abrupt load variations and satisfactory dynamic response.

B. Balancing Control

The following results evaluate the performance of the proposed balancing strategy under the two scenarios defined in Tab. 4.

Fig. 10 shows the evolution of the individual battery SoCs during the balancing process. In both scenarios, the batteries start with different initial SoCs. However, the proposed balancing algorithm gradually reduces these differences, leading all battery packs to converge to nearly the same SoC by the end of the discharge process. This behavior confirms the effectiveness of the proposed balancing strategy in equalizing the SoC values among the battery packs.

A comparison between Fig. 10(a) and Fig. 10(b) highlights the influence of battery capacity mismatch on the balancing dynamics. In Scenario 1, where all batteries have identical capacities, the SoCs converge more closely. In contrast, Scenario 2 considers battery packs with different capacities. Although the controller does not explicitly use the capacity values, these differences affect the individual rates of SoC variation and, consequently, the balancing behavior. As a result, a larger steady-state SoC error is observed in Scenario 2, although the individual SoC values still converge within the simulated time interval. This behavior is consistent with the theoretical analysis presented in Section II-C.

Fig. 11 presents the dc-link voltage during the balancing process for both scenarios. Despite the continuous adjustment of individual battery power to promote SoC equalization, the dc-link voltage remains regulated around its 192 V reference. These results demonstrate that the proposed controller achieves battery balancing while maintaining dc-link voltage regulation. The observed transients are associated with the power reversal events considered in the simulations and are effectively rejected by the local control strategy.

Fig. 12 shows that the DAB module connected to the battery pack with the highest initial SoC starts with the highest output-voltage reference and, consequently, delivers more power during discharge. As the SoC differences decrease, the individual voltage corrections are reduced, and

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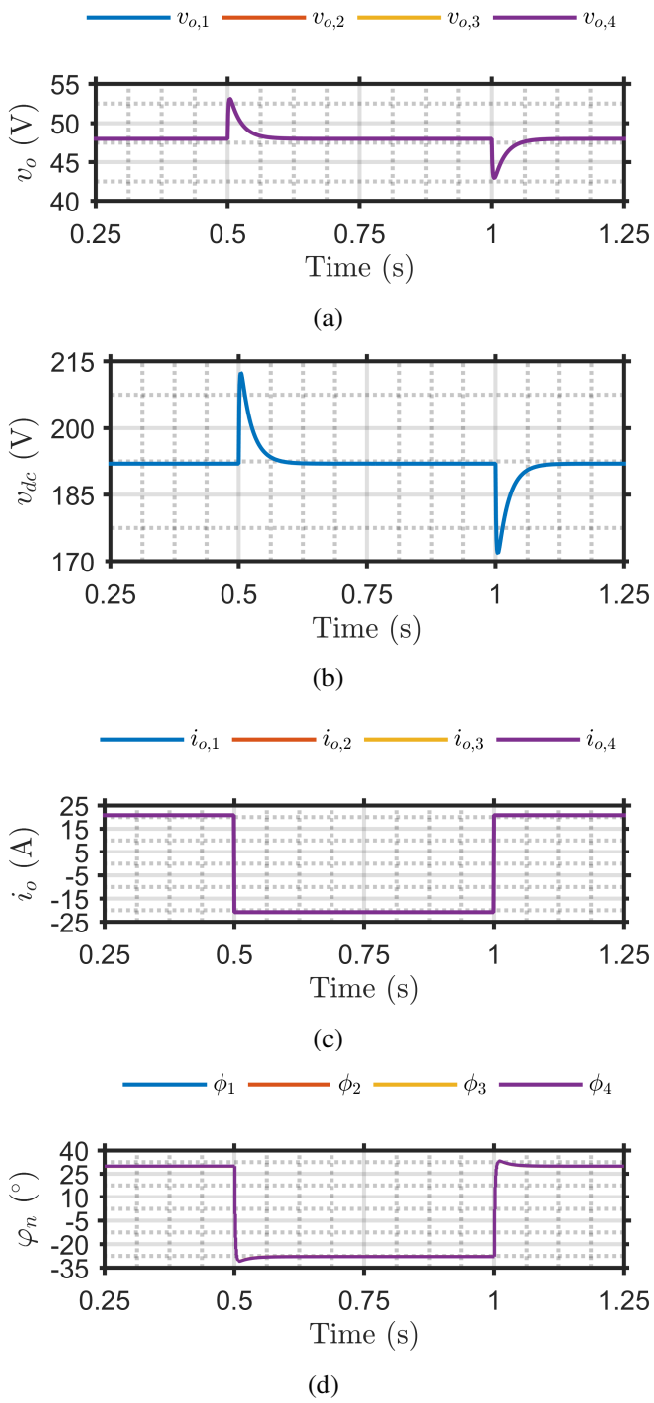


FIGURE 9. Simulation results during the load transient: (a) individual DAB output voltages, (b) dc-link voltage, (c) DAB output currents, and (d) phase-shift angles.

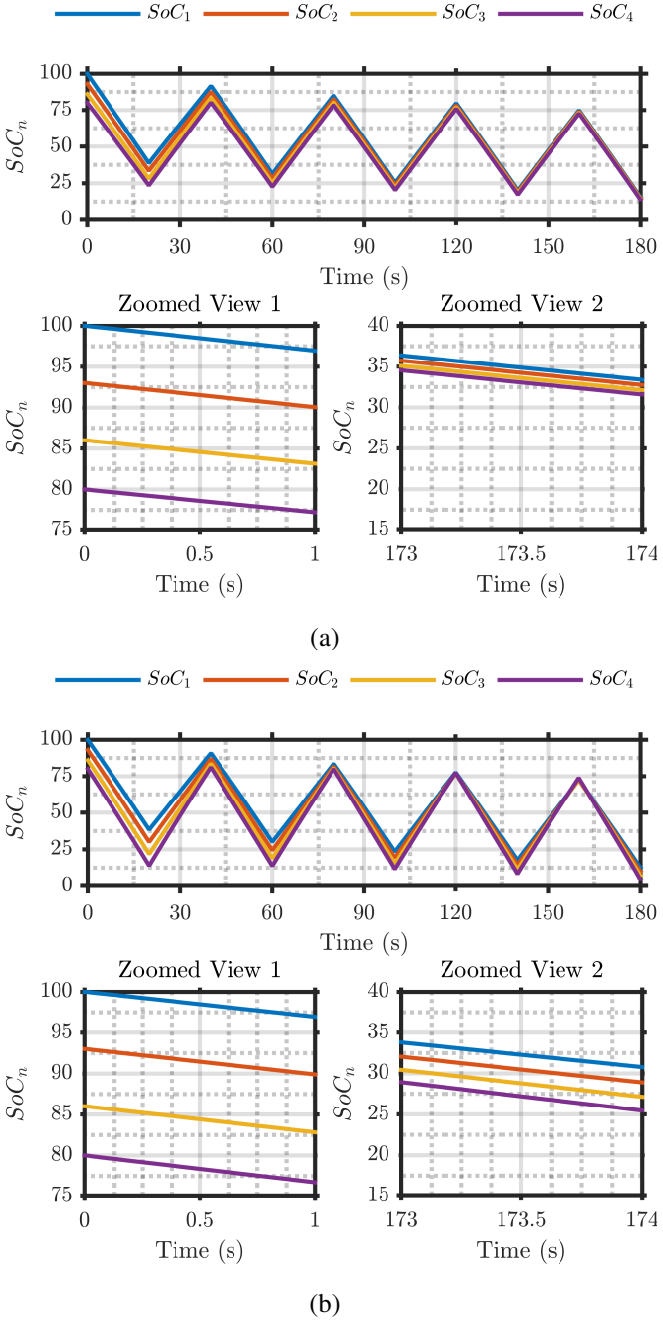


FIGURE 10. Simulation results for the balancing control considering different initial SoCs and (a) identical capacities, (b) different capacities

the DAB output voltages gradually converge toward their common nominal reference.

V. C-HIL VALIDATION

This section presents the C-HIL results for the local voltage control, the SoC balancing control under the two scenarios defined in Tab. 4, and the DAB operating waveforms. In the C-HIL setup, the DAB power converters, battery packs, and electrical load are represented by real-time models running in the Typhoon HIL 606 with a simulation step of 0.6 μs, whereas the control algorithm is executed in the external digital controller. It was used the DSP 180 as a hardware interface to the DSP TMS320F28379D and the PLECS Coder as the software tool to flash the code. The control algorithm runs at a sampling frequency of 25 kHz.

For monitoring the DSP internal variables, a decimation factor relative to the control frequency was applied. In the

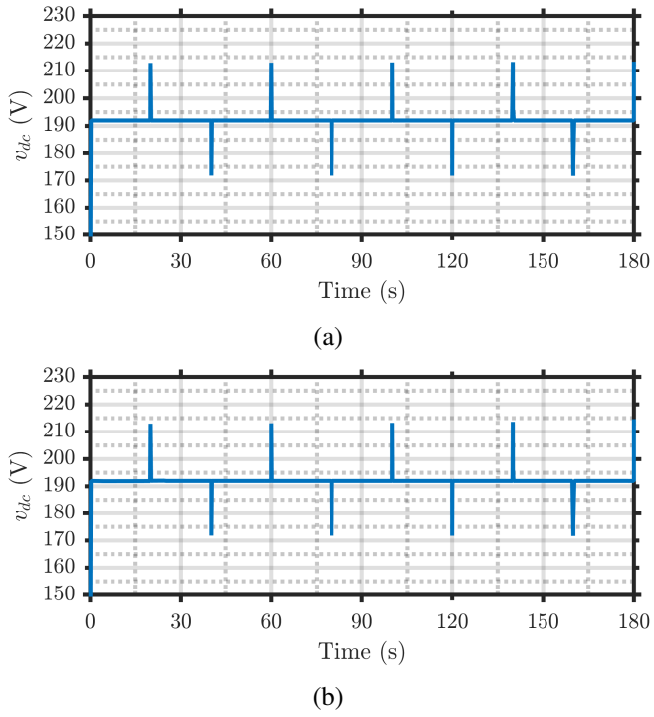


FIGURE 11. v_{dc} **behavior for the balancing control considering different initial SoCs and (a) identical capacities, (b) different capacities.**

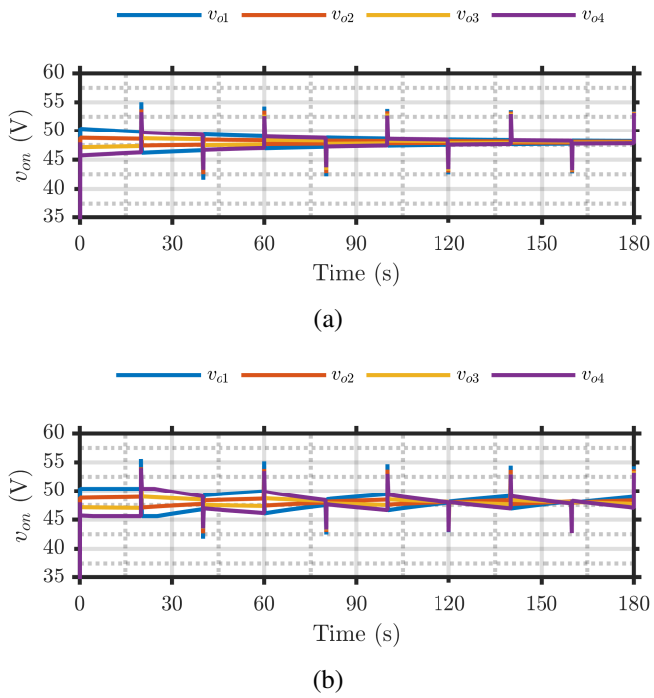


FIGURE 12. v_{on} **behavior for the balancing control considering different initial SoCs and (a) identical capacities, (b) different capacities.**

Typhoon HIL SCADA, an update rate of 1.6 MHz was used to capture fast transient responses, whereas the scope acquisition rate was reduced to 2 kHz for evaluating SoC balancing over extended test durations.

C-HIL evaluates the implemented control algorithm on the physical DSP, with closed-loop signal exchange between the controller and the real-time power-stage model. The tests exercise the voltage-control and balancing functions together, assessing reference tracking, rejection of the applied load disturbances, and power redistribution under different initial SoCs and battery capacities. Thus, they provide evidence of functional integration and real-time controller execution for the evaluated four-module system.

The tests validate controller functionality for the modeled system; device-level commutation, efficiency, thermal and insulation performance, and physical BMS interfaces are outside this scope. Capacity scaling accelerates the balancing tests, so their durations do not represent full-capacity balancing times.

A. Local Control

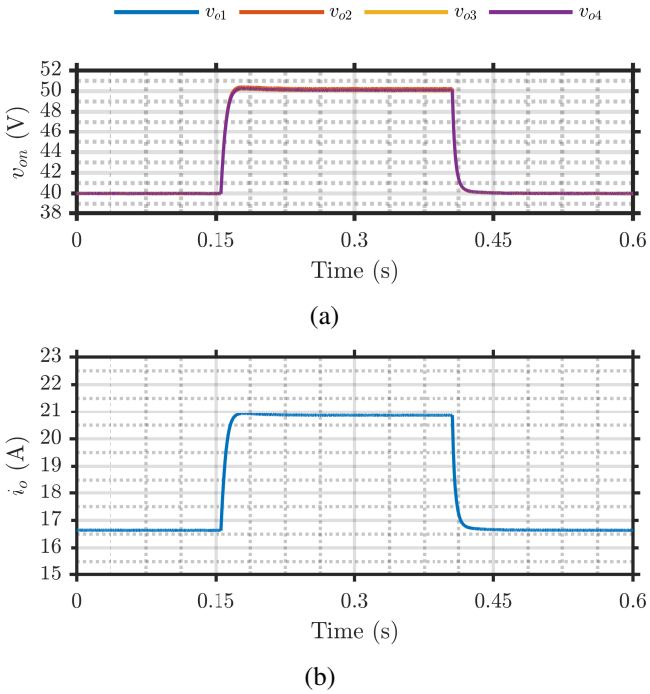


FIGURE 13. C-HIL response to an individual DAB output-voltage reference step: (a) output voltage and (b) output current. ***Remark*****: Data collected through HIL SCADA interface.**

The dynamic performance of the local voltage controller was initially evaluated under a step change in the individual DAB output-voltage reference, considering a 9.6 Ω resistive load connected to the dc-link and a controlled current source set to 0 A. Fig. 13(a) presents the response when the reference is changed from 40 V to 50 V. The controller demonstrated stable operation, with accurate reference tracking and no sustained oscillatory behavior. Fig. 13(b) shows the corresponding current behavior, indicating that the converter adjusted the transferred power as expected to satisfy the new operating condition.

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Fig. 14 shows a zoomed-in view of the phase-shift evolution during a voltage reference increase, based on data captured directly from the DSP memory. The phase-shift angle increases in response to the voltage regulation demand while remaining below 90° throughout the transient, confirming that the modulation remains within the expected operating limits and preserves power transfer capability.

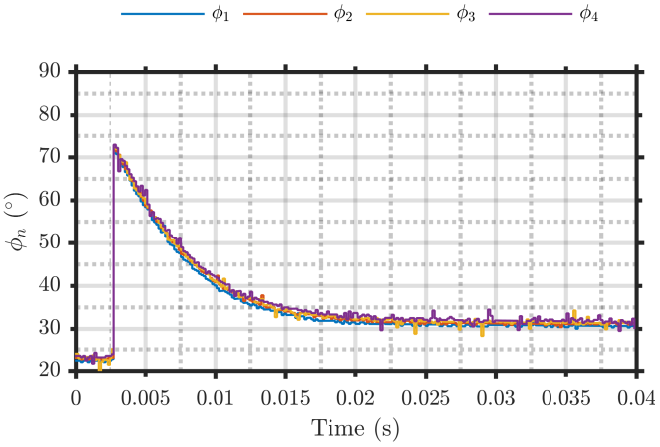


FIGURE 14. Phase-shift angle response. *Remark*: Data collected through PLECS Coder interface using a decimation factor of 4.

Fig. 15 presents the system response with a constant resistive load of 9.6 Ω, initially with the controlled current source set to 0 A. The current source reference is stepped to 40 A and subsequently returned to 0 A. Fig. 15(a) shows the individual DAB output voltages. Power reversals occur at $t = 0.16$ s and $t = 1.02$ s, producing transient voltage deviations. At $t = 0.16$ s, the output voltage rises to approximately 56.3 V, whereas during the subsequent transition, it drops to approximately 40 V. These deviations are transient, and the module voltages subsequently recover toward their nominal value of 48 V, demonstrating effective compensation by the local PI controllers.

Fig. 15(b) shows the total dc-link voltage (v_{dc}). The short recovery time and rapid voltage stabilization after each disturbance confirm that the distributed control architecture maintains overall dc-link regulation, even under severe dynamic loading.

Fig. 15(c) shows that all series-connected DAB outputs carry the same dc-link current, as imposed by the series connection. Consequently, the power processed by each module is determined by its individual output voltage. The current transitions between 20 A and −20 A follow the imposed charging/discharging profile. These results demonstrate the coordinated operation of the series-connected DAB converters and their ability to accommodate bidirectional power variations while maintaining stable operation.

Fig. 16 presents the real-time simulated DAB waveforms corresponding to the module connected to Battery 1. As shown in Fig. 16(a), the phase-shift angle between the

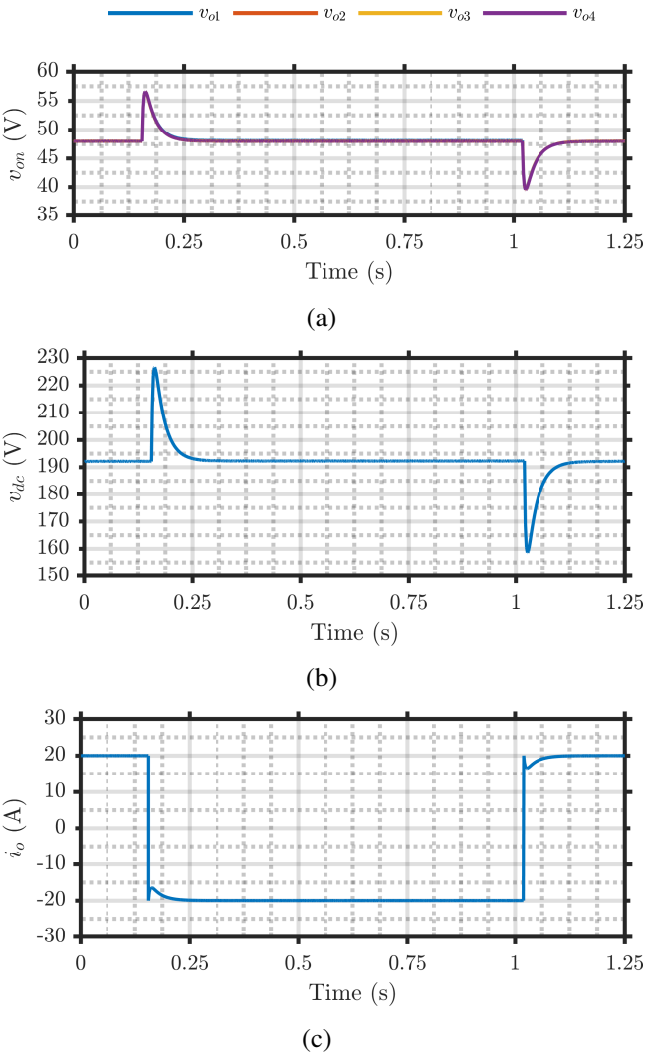


FIGURE 15. Behavior of (a) individual DAB output voltages, (b) dc-link voltage, (c) module currents. *Remark*: Data collected through HIL SCADA interface.

primary and secondary bridge voltages (v_{t1} and v_{t12}) dictates the magnitude and direction of the power flow. This phase displacement is the fundamental control parameter for regulating energy transfer within the system. Complementarily, Fig. 16(b) illustrates the high-frequency current i_{t1} circulating through the coupling inductor. The linear slopes observed in the current waveform are consistent with the application of rectangular voltage pulses across the leakage inductance, characterizing the typical inductive behavior of the DAB topology under SPS modulation.

B. Balancing Control

Fig. 17 presents the individual SoC values during the discharge interval. The initial SoC differences progressively decrease as the balancing process proceeds. This demonstrates that the balancing methodology is not restricted to identical modules and can tolerate practical manufacturing or aging variations. It confirms that batteries with relatively higher

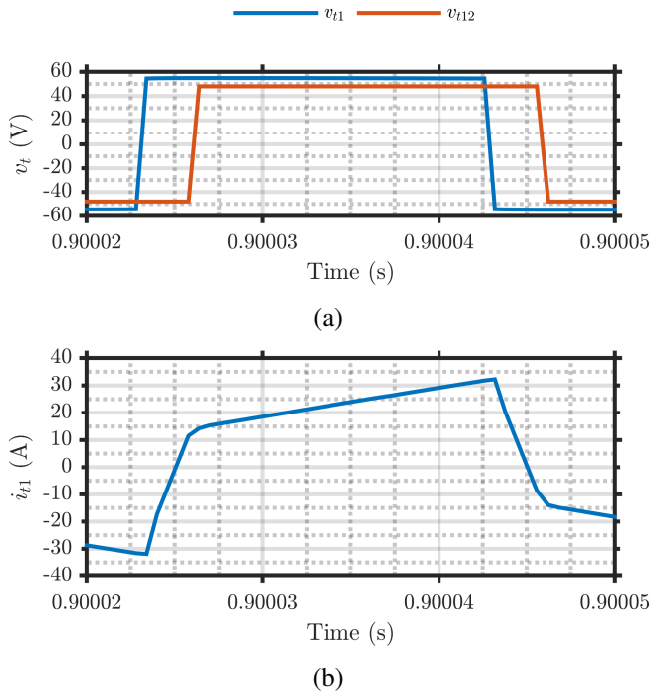


FIGURE 16. DAB converter waveforms: (a) primary and secondary voltage and (b) primary current. *Remark*: Data collected through HIL SCADA interface.

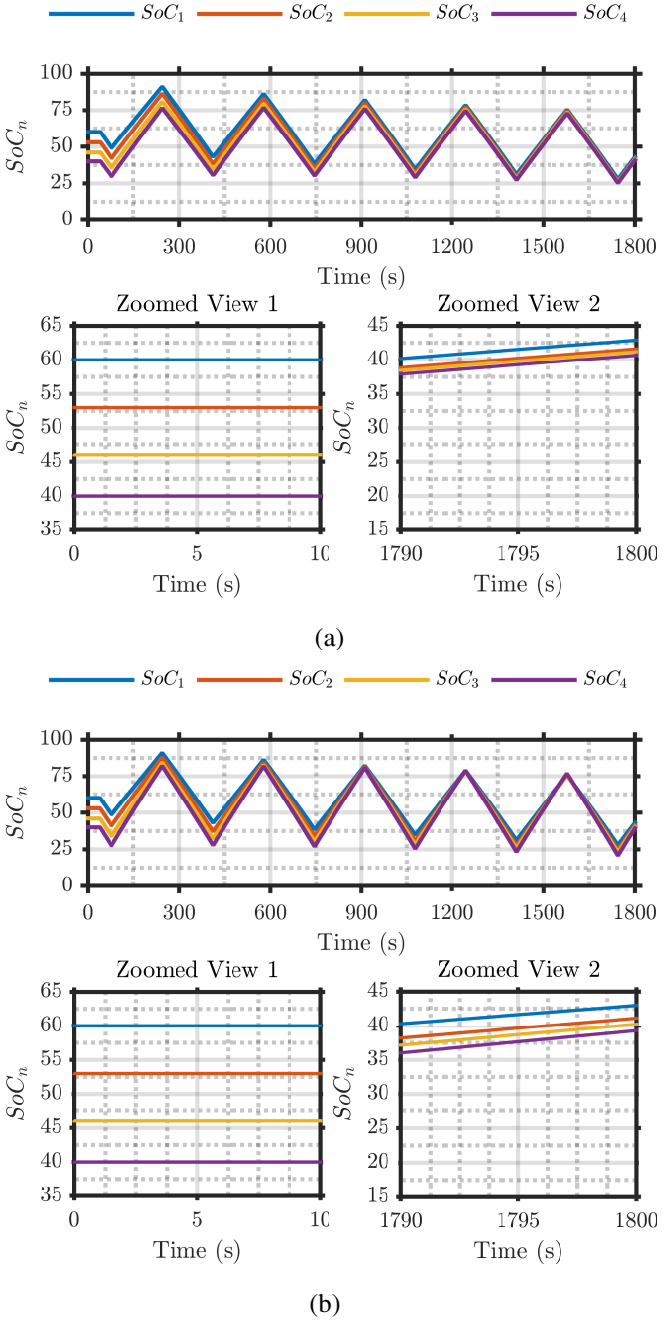


FIGURE 17. C-HIL SoC balancing results considering different initial SoCs and (a) identical battery capacities and (b) different battery capacities. *Remark*: Data collected through HIL SCADA interface.

SoC contribute proportionally more power, accelerating their discharge rate, while lower-SoC batteries are preserved until convergence is achieved.

Fig. 18 presents the corresponding dc-link voltage over the same interval, showing an overshoot and undershoot of approximately 17% during the transients. Despite these deviations, the balancing process has a limited impact on dc-bus regulation, demonstrating the ability of the proposed control strategy to achieve simultaneous SoC equalization and maintain high-voltage bus stability.

Fig. 19 shows the output voltage behavior. Battery 1, which initially has the highest SoC, is assigned the highest output voltage, beginning near 50 V. This elevated voltage reference causes Battery 1 to deliver more power to the dc-link, thereby accelerating its discharge rate. Conversely, Battery 4, with the lowest initial SoC, starts at approximately 45 V, reducing its power contribution and preserving its available charge. Batteries 2 and 3 operate at intermediate voltage levels proportional to their respective SoC values, creating a coordinated gradient of power contribution across the battery string. Over time, the output voltages progressively converge toward a common steady-state value near 48 V, reflecting the gradual equalization of all battery SoCs. This voltage convergence demonstrates that the balancing algorithm redistributes the module power contributions without requiring direct energy transfer between battery packs. Instead, balancing is achieved through controlled modulation of each converter power contribution to the shared dc-link.

VI. CONCLUSION

This paper proposed a modular Smart Battery architecture using isolated DAB converters with series-connected outputs and supervisory SoC balancing. PLECS simulations and four-module C-HIL tests with a 192-V dc link demonstrated voltage-reference tracking, load-disturbance rejection, and SoC equalization under the evaluated initial imbalances and capacity mismatches. The C-HIL results substantiate the integration of local and supervisory control on the physical

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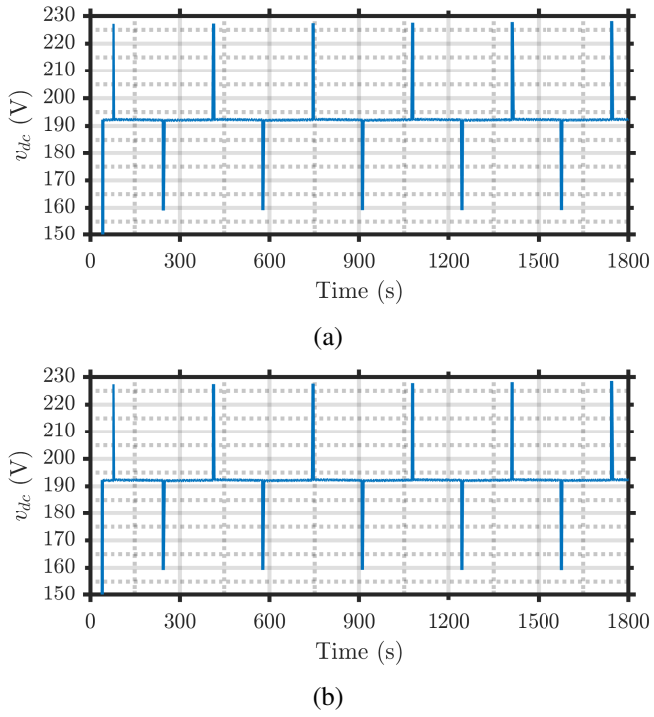


FIGURE 18. C-HIL dc-link voltage during SoC balancing considering different initial SoCs and (a) identical battery capacities and (b) different battery capacities. *Remark*: Data collected through HIL SCADA interface.

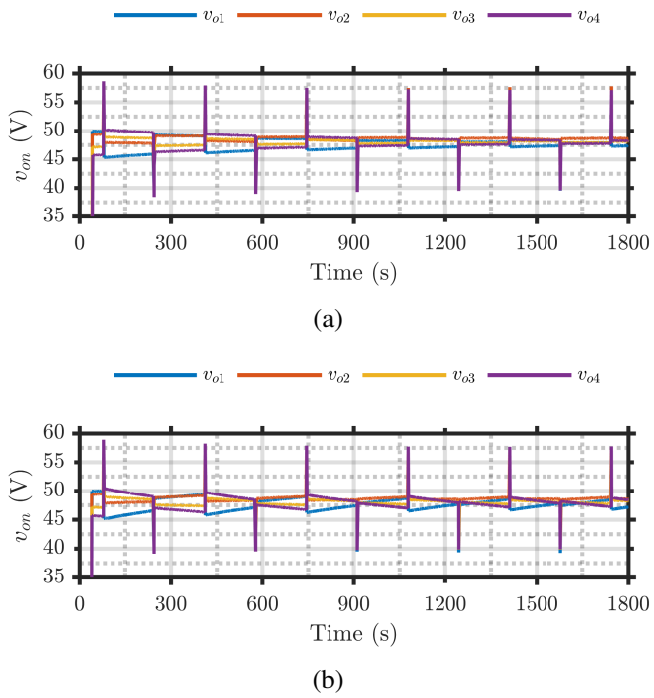


FIGURE 19. C-HIL individual DAB output voltages during SoC balancing considering different initial SoCs and (a) identical battery capacities and (b) different battery capacities. *Remark*: Data collected through HIL SCADA interface.

DSP and their closed-loop operation with the real-time power-stage model.

The architectural analysis establishes ideal voltage and power scaling with module count while identifying the associated control/communication workload, cumulative insulation requirements, and fault-handling and reserve-capacity requirements. The SPS assessment identifies favorable switching-current polarity at rated power in both directions over the considered voltage interval and quantifies the light-load boundaries. These are necessary theoretical conditions for ZVS.

These conclusions concern control implementation and architectural analysis; physical power-stage performance is outside the validation scope.

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AUTHOR'S CONTRIBUTIONS

G.A.B.SANTOS: Formal Analysis, Investigation, Methodology, Software, Writing – Original Draft. **A.F.CUPERTINO**: Conceptualization, Funding Acquisition, Investigation, Supervision, Writing – Review & Editing. **J.V.M.FARIAS:** Conceptualization, Formal Analysis, Investigation, Supervision, Writing – Review & Editing. **G.M.SOARES:** Conceptualization, Investigation, Project Administration, Writing – Review & Editing.

PLAGIARISM POLICY

This article was submitted to the similarity system provided by Crossref and powered by iThenticate – Similarity Check.

DATA AVAILABILITY

The data used in this research is available in the body of the document.

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