# BOOST DC-DC CONVERTER WITH SWITCHED-CAPACITOR AND FOUR-STATE SWITCHING CELL

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***Abstract* – The integration of switched-capacitor voltage multiplier cells in basic converter topologies has been studied to provide voltage gain and voltage stress reduction. However, SC cells do not provide current sharing and additionally they induce high current spikes in the devices, which are limitations of these structures to operate in high power levels. The main contribution of this paper is to overcome this drawback proposing the use of a multistate switching-cell for current sharing in SC-based boost converters, which reduces the current stress in the power devices and increases the power levels of this family of converters. The proposed concept can be generalized for m number of SC cells and n number of switching cells to increase the voltage gain and current levels. Furthermore, it can be applied to other basic structures. The theoretical analysis of the proposed structure was evaluated experimentally in a 3 kW boost-type dc-dc converter, achieving 200 V to 1200 V voltage gain, and reaching 98.4% of maximum efficiency.**

***Keywords* – High Voltage Gain, Hybrid Dc-Dc Converter, Multistate Switching Cell, Switched-Capacitor, Voltage Multiplier.**

## I. INTRODUCTION

A large variety of topologies and concepts have been explored in the scientific literature to develop new structures with high conversion rates and low voltage and current stress. Thus, it is possible to benefit from features of different structures to select the desired characteristics for a design [1], [2].

Several applications require high conversion rates and high voltage levels to work. Some renewable energy systems, such as photovoltaic modules, fuel cell and small wind generators typically provide low voltage levels, which must be converted to higher levels for practical applications. There are also types of loads that require high voltage supplies to operate properly, such as pulsed lasers, railway traction systems and electric vehicles [1], [3], [4].

Structures developed for high voltage gain have been conceived by integrating topologies that provide a high conversion ratio and are able to reduce the voltage stress on switches. Several techniques can be used, such as transformers, switched-capacitor (SC) voltage multiplier cells [5]–[7], switched-inductor cells [8]–[10], cascaded converters [11]–[13] and the association these different techniques to develop new topologies [14], [15].

SC-based converters have been proposed in the literature for high gain applications due to their simplicity and stable circuits, which do not require inductive elements. Some SC topologies can increase the conversion ratio without compromising the voltage stress on the switches. These converters, however, have some limitations. The lack of inductive elements can affect the capability of regulating the voltage in SC converters, making it more complex. Furthermore, the charge and discharge of the capacitors can induce current spikes if not designed correctly, since the current in SC converters is usually only limited by parasitic devices in the path. However, inductive elements can be also used in series with the capacitors to limit these current spikes. The voltage regulation limitations of SC converters can be worked around by integrating the SC cells with basic converter topologies, thus achieving high voltage gain and reducing the voltage stress on devices. The current stress and discontinuous current are also issues in some SC topologies, therefore the use of current sharing techniques can help improving the performance of these converters [16]–[20].

An alternative to reduce the current stress is interleaved converters, which associate converters in parallel to reduce the current stress in the devices and phase-shift the switching signals to reduce harmonic content. In boost topologies, the interleaved converters reduce the input current high-frequency harmonic content, allowing the use of smaller harmonic filters. The interleaving technique can be applied with single inductors or with an Intercell-Transformer (ICT) [21]–[25].

This paper proposes the concept of a new boost topology that integrates SC cells and a multistate switching cell, which uses an ICT for current sharing in the devices. The SC cell provide a higher voltage gain with lower voltage stress on the devices and the ICT provides current sharing and input current harmonic reduction. The main contributions of this study are the use of an ICT for the current sharing, proposing a generalized topology that can be configured in different ways and providing a comparison of different topologies with generalized equations for n interleaved cells. In the latest years some topologies have been proposed in the literature integrating interleaving techniques with SC circuits. However, most SC converters are designed for low power levels and their structures often cannot be generalized into more stages [26], [27]. Other structures also use more switches that may require isolated gate drivers [28]–[30].

This paper is presented in four sections. Section II shows the converter operation, steady state analysis and main design equations. Section III shows the experimental validation of the converter, and Section IV shows the conclusions of the study.

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## II. PROPOSED TOPOLOGY

The integration of SC cells in the basic boost converter was proposed by [21], which used an interleaved boost converter with voltage multipliers. The converter proposed in [22] provides high voltage gain and current sharing. On the other hand, the voltage stress on the diodes is twice the input voltage multiplied by the conventional boost conversion ratio.

The concept proposed in this paper is based on the converter proposed in [23], which integrates a ladder SC cell with the classic boost converter to increase voltage gain and reduce the voltage stress on the switches. The main drawback of the topology proposed in [31] and SC-based topologies is the high current spikes provided by the capacitor charge, which limits the power range of this family of converters. The main contribution of this study is the insertion of an ICT to reduce the voltage stress in converters based on the integration of the boost converter with SC cells. The generalization of the proposed structure is shown in Figure 1.

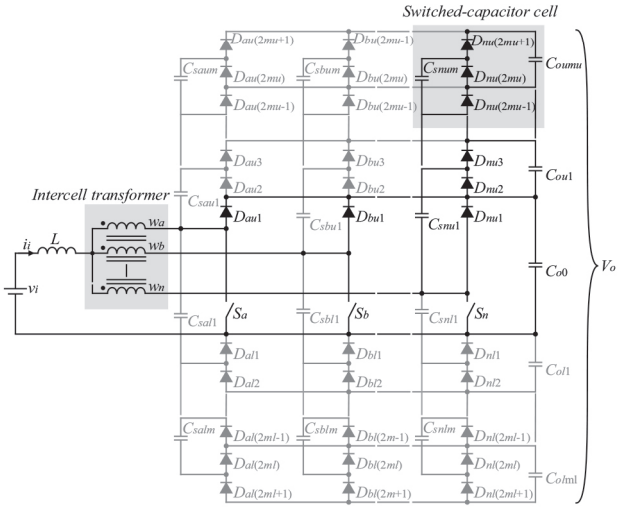



Fig. 1. Generalization of the proposed topology.

The proposed structure can be configured in different ways according to the project requirements. More SC cells can be added to increase the voltage gain, the cells can be added to a single leg or to all legs, and more legs can be inserted to reduce the current and to reduce the number of cores and size of the input filter. The diodes can be replaced by active switches whether a bidirectional structure is needed or to improve the efficiency in applications with a lower input voltage. In this study, a structure with three legs and one upper and one lower SC cell in each leg is studied, shown in Figure 2.

Although the focus of this paper is to present the topology in steady-state operation, it is possible to control the converter by using classic control techniques. The main control limitation of the converter is that major differences in the gate drivers due to non-idealities may affect the current balance in the ICT. There are works in the literature that approach this issue and present solutions, such as using the Lunze transform to model the multistate switching cell [32], or by using an auxiliary winding in the ICT to measure the current imbalance [33]. The output capacitors do not require any control technique, since the SC-cell natural characteristic already provides balanced capacitor voltages.

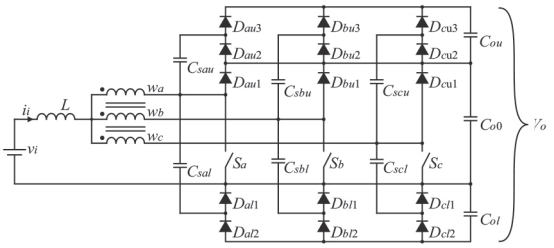



Fig. 2. Proposed structure with three legs.

The symmetrical configuration of the SC cell shown in Figure 2 is not a requirement. Three variations of the proposed converter are shown in Figure 3 to exemplify the different ways of implementing the converter. Since the current in the SC cell contribution for the switch losses is less than the input current contribution, it is possible to use the SC cell in only one leg, as shown in Figure 3.a. The ladder SC cell can also be implemented with a single output capacitor and the middle output capacitor $C_{o0}$ acting as a cell capacitor, as shown in Figure 3.b. This configuration can be more efficient and economical for some applications, but does not have balanced series capacitors in its output. It is also not necessary to employ a symmetrical configuration for the cells, the converter can be implemented with only upper SC cells, as shown in Figure 3.c. This configuration has as a major advantage the same ground reference for the switches and the output, but it requires one intermediate conversion stage between the boost converter and the uppermost cell, which reduces the converter efficiency. In converters with a lower voltage rating, all the diodes can be replaced by active switches to improve the efficiency. However, this would require the use of isolated gate drivers.

The converter analysis is performed considering that all legs have the same duty cycle, thus the duty cycle of all legs is referred to as d, instead of $d_a$ to $d_n$. This topology operates in three different regions, region A, where $0 > d > 1/3$, and the switch gate signals never overlap; region $B$, where $1/3 > d > 2/3$ and two signals overlap at some stages; and region C, where $d > 2/3$ and there are at least two gate signals overlapping in each operational stage. For more conciseness, only region A will be explained with more details to understand the operation principle, since all of the operation regions share the same static gain and have similar characteristics.

### *A. Region A (0 < d <1/3)*

The modulation of the proposed converter is performed by phase-shifting the carrier signals in 120°. In the region A, since the duty cycle is below 1/3, there are no overlapping signals, as can be seen in the modulation scheme, shown in Figure 4.

The proposed converter has six operational stages in the region A, which are described in Figure 5. In the first stage [See Figure 5.a], the switch $S_a$ is turned ON and the diodes $D_{au2}$ and $D_{al2}$ are forward biased. The upper cell capacitor $C_{scu}$ receives energy from the intermediary output capacitor $C_{o0}$ while $C_{sal}$ delivers energy to the output capacitor $C_{ol}$. In the other legs, the switches are turned OFF and the diodes $D_{bu1}$, $D_{bl1}$, $D_{bu3}$, $D_{cu1}$, $D_{bl1}$ and $D_{cu3}$ (the odd numbered diodes in the legs where the switch is turned OFF) are forward

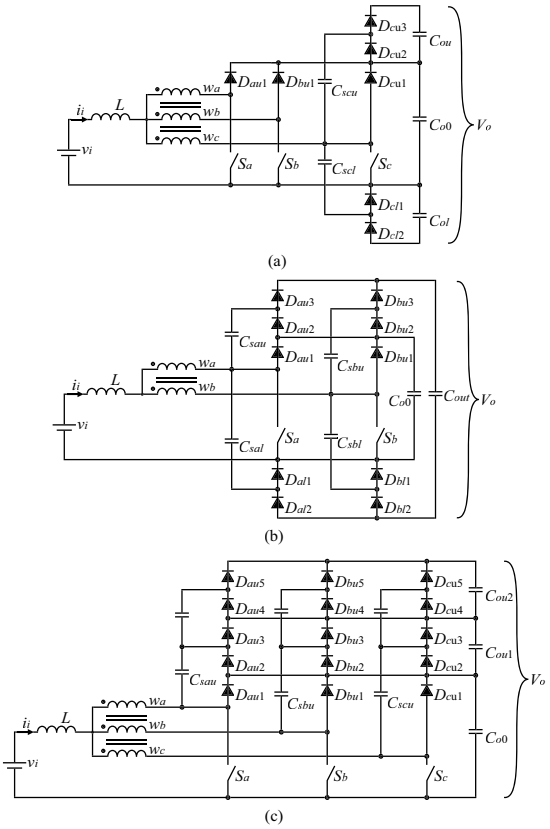



Fig. 3. Converter configurations: (a) SC cells in a single leg, (b) Single output capacitor and (c) only upper SC cells.

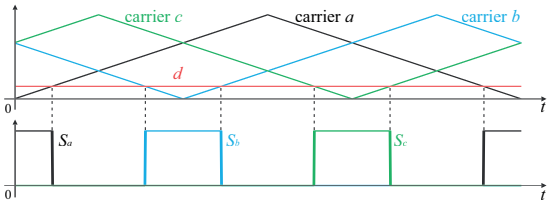



Fig. 4. Modulation scheme in region A.

biased. The input current is divided between the windings of the ICT. The current at $w_a$ flows through $S_a$ and the currents in the other windings flow through the diodes $D_{bu1}$ and $D_{cu1}$. In the legs $b$ and $c$, the upper cell capacitors $C_{sbu}$ and $C_{scu}$ transfer energy to the upper output capacitor $C_{ou}$ and the lower capacitors receive energy from the middle output capacitor $C_{o0}$. For a clearer visualization, Figure 6 shows how the cell capacitors in each leg are connected to the output when its respective switch is turned ON or OFF.

In the second stage [See Figure 5.b], all switches are turned OFF and all the odd numbered diodes ($D_{iu1}$, $D_{iu3}$ and $D_{il1}$) are forward biased. All windings of the coupled inductor are connected to the output capacitor $C_{o0}$ through the diodes $D_{iu1}$, therefore there is a direct connection between the input inductor and output intermediary capacitor, since the legs in the ICT are short-circuited through the forwardly biased diodes $D_{au1}$, $D_{bu1}$ and $D_{cu1}$. The output capacitor $C_{o0}$ and the coupled inductor transfer energy to the lower cell capacitors $C_{sal}$, $C_{sbl}$ and $C_{scl}$, which are connected in parallel with the output capacitor $C_{o0}$ and store energy in this stage. All the upper cell capacitors $C_{sau}$, $C_{sbu}$ and $C_{scu}$ transfer energy to

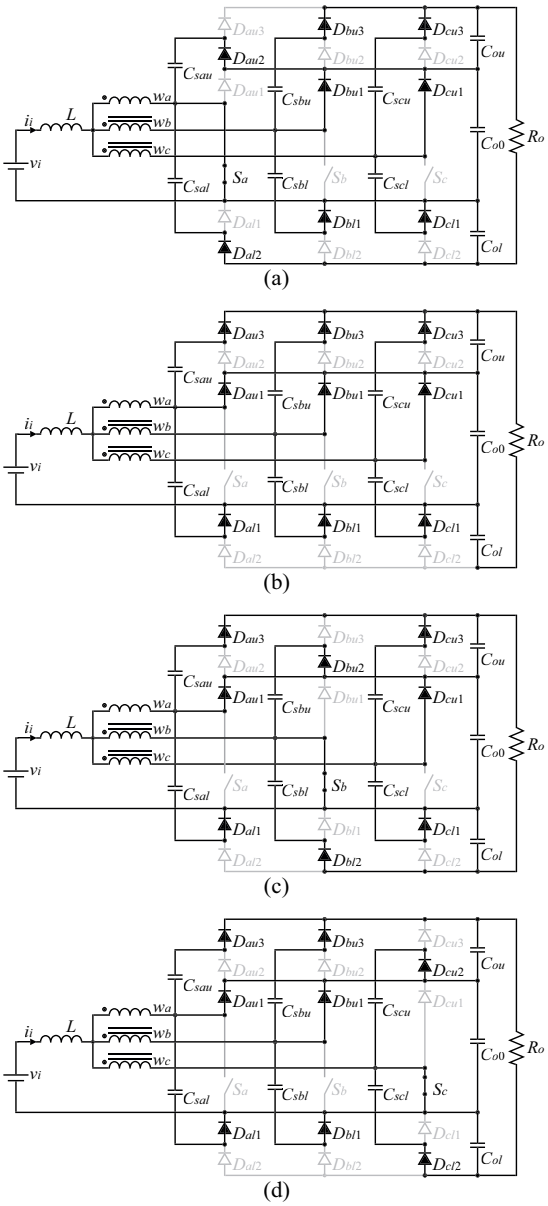



Fig. 5. Operational stages in region A: (a) stage 1, (b) stage 2, 4 and 6, (c) stage 3 and (d), stage 5.

the upper output capacitor $C_{ou}$ through the diodes $D_{au3}$, $D_{bu3}$, $D_{cu3}$, $D_{au1}$, $D_{bu1}$ and $D_{cu1}$. Since the current of the windings in the ICT is higher then discharge currents of the upper cell capacitors, the diodes $D_{au1}$, $D_{bu1}$ and $D_{cu1}$ are forward biased and allow the parallel connection between the upper cell capacitors and the upper output capacitor.

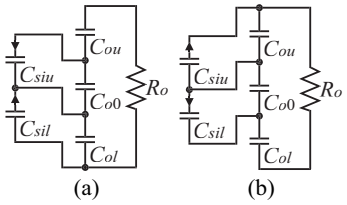



Fig. 6. Equivalent circuits to the capacitor connections in the proposed converter: (a) Switch turned ON and (b) Switched turned OFF

The operational stages 3 and 5 [See Figures 5.c and 5.d]

have similar operation principles to that of stage 1, but with the switches $S_b$ and $S_c$ turned ON in each respective stage. The operational stages 4 and 6 [See Figure 5.b] have the same operation principle as that of stage 2, since no switch is turned ON in these stages.

The main waveforms of the converter in the region $A$ are shown in Figure 7. The main advantages highlighted in these waveforms are the current sharing in the coupled inductor windings, the current ripple frequency in the input inductor, the voltage levels on the inductor and the output voltage divided in the capacitors.

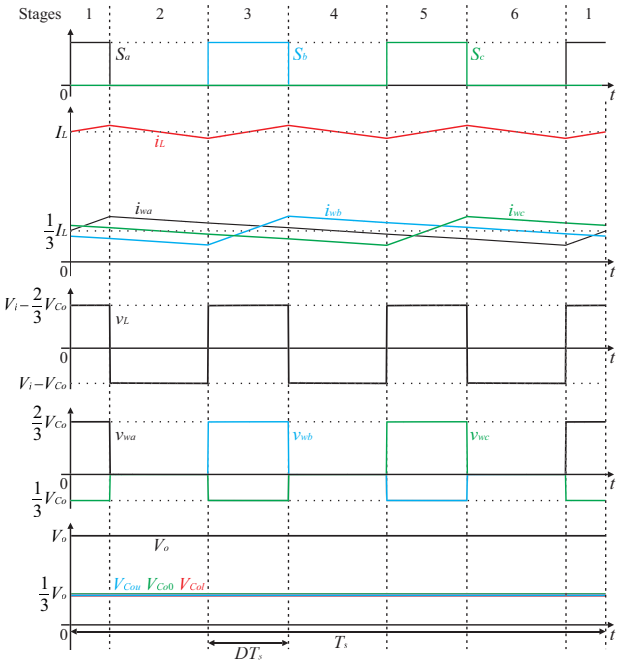



Fig. 7. Main waveforms in the Region A.

Aiming to simplify the analysis of the converter, the SC cell can be represented as an ideal transformer that represents the voltage gain of the cell. This simplification can be considered due to the SC cell natural capacity of self-balancing the capacitor voltages. Thus, an equivalent circuit can be used to obtain the converter gain and analyze the inductor ripple. The equivalent circuit is shown in Figure 8, where mu is the number of upper SC cells in at least one leg and ml is the number of lower SC cells. Using SC cells in more legs do not affect the total multiplication factor, it only affects the current distribution in the legs.

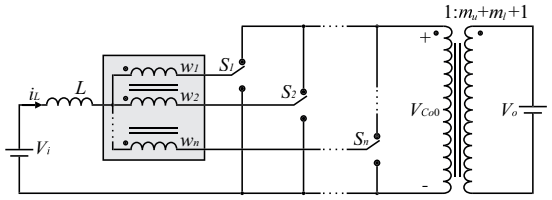



Fig. 8. Equivalent circuit of the proposed topology.

It should be noted that the odd and even operational stages have similar operation principles from the input perspective. Therefore, the steady-state analysis can be performed for one third of the switching period. The stages 1, 3 and 5 and the stages 2, 4 and 6 can be represented by equivalent circuits, as shown in Figures 9.a and 9.b, respectively. In the equivalent circuits it should be noted that, even though all windings have the same number of turns, the voltage is not the same in all windings. This happens because of the way the ICT is implemented. In the ICT for four state switching cells each winding is built in a different leg, thus the magnetic flux in one leg is divided between the other legs in the core. Therefore, the coupling factor of the ICT is given by

$$k = \frac{M_{ij}}{\sqrt{L_i L_j}} = -\frac{1}{n-1} \tag{1}$$

where $M_{ij}$ is the mutual inductance of the windings $i$ and $j$, $L_{ii}$ is the self inductance of a winding and $n$ is the total number of windings.

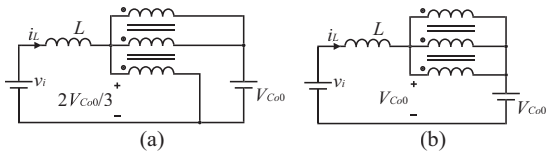



Fig. 9. Equivalent circuit of the operational stages in the region A: (a) stages 1, 3 and 5, and (b) stages 2, 4 and 6.

The static gain of the topology is obtained by verifying the Volts-second relation on the input inductor. Given that

$$V_{Co0} = \frac{V_o}{m_u + m_l + 1} \tag{2}$$

the voltage gain of the proposed topology is described by.

$$\frac{V_o}{V_i} = \frac{m_u + m_l + 1}{1 - D} \tag{3}$$

where $m_u$ and $m_l$ are the number of upper and lower cascaded SC cells in the leg with most SC cells. Figure 10 shows the voltage gain generalized for $m_u + m_l$ SC cells.

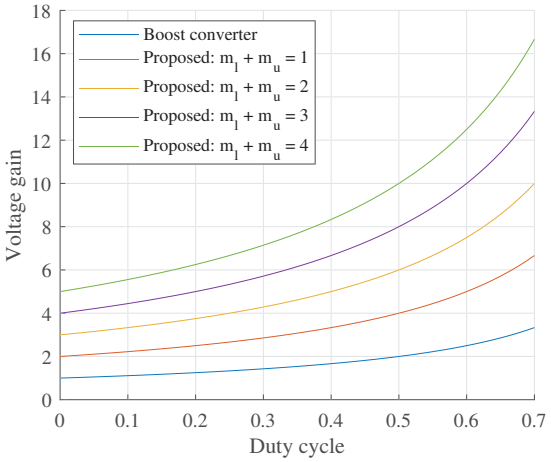



Fig. 10. Voltage gain of the proposed topology.

By deriving the voltage gain with the Volts-second relation for converters with a different number of phases, it should not affect its ideal voltage gain. This happens because the coupling factor of the transformer depends the number of

phases and should change the voltage relation on the winds of the ICT in a way that compensates this difference, as long as (1) is obeyed. By analyzing the voltage on the input inductor in one stage, it is possible to derive the inductor current ripple, described by

$$\Delta i_L{}^{regA} = \frac{V_o(1-3D)D}{3Lf_s(m_u+m_l+1)}. \quad (4)$$

To analyze the voltage ripple in all the regions in function of the duty cycle, the current ripple is normalized, as given by

$$\overline{\Delta i_L}^{regA} = (1-3D)D. \quad (5)$$

*B. Regions B and C (d > 1/3)*

In regions *B* and *C* there is overlap between the pulses. In region *B*, in one operational stage there is either one or two switches turned ON in each stage, whereas in region *C* there are always two or all of the switches turned ON. This results in different waveshapes, illustrated in Figure 11. However, by performing the voltage-seconds analysis in the inductor and deriving the static gain it can be verified that the static gain in these regions is the same as in region *A*.

The current ripple in these regions can also be derived through the inductor voltage in each stage, resulting in

$$\begin{cases} \Delta i_L{}^{regB} = \frac{V_o(1-3D)D}{3Lf_s(m_u+m_l+1)} \\ \Delta i_L{}^{regC} = \frac{V_o(-9D^2+9D-2)}{9f_s(m_u+m_l+1)L} \end{cases}. \quad (6)$$

The normalized inductor current ripple in regions *b* and *c* are given by

$$\begin{cases} \overline{\Delta i_L}^{regB} = (1-3D)D \\ \overline{\Delta i_L}^{regC} = \frac{-9D^2+9D-2}{3} \end{cases}. \quad (7)$$

The normalized current ripple in all regions can be plotted as a function of the duty cycle, as shown in Figure 12. It should be noted that the maximum current ripple occurs where *D* = 1/6, 1/2 and 5/6. In the transition between the regions the current ripple is zero. By calculating the inductance replacing *d* by the condition where the ripple is at its maximum value, the same inductance value is obtained, given by

$$L = \frac{V_o}{36(m_u+m_l+1)\Delta i_L f_s}. \quad (8)$$

*C. Capacitors*

The capacitors are chosen by calculating the equivalent resistance of the SC module composed of the cells in each leg, considering that 1/3 of the total output power is processed in each leg. Since the theoretical analysis is too extensive, it will not be included in this paper, just explained briefly.

There are several methods proposed in the literature to obtain the equivalent resistance of an SC circuit [34]–[36]. Ladder SC cells can also be designed for zero-current switching operation by inserting an inductor in series with the cell capacitors. This resonant operation cell provides better voltage regulation, soft-switching, but may increase the volume and cost in SC-based converters by the insertion of this inductor [37]. The method used is based on method proposed by [35], which calculates the equivalent resistance based on two asymptotes based in idealizations of slow and fast switching characteristics of the circuit. By calculating the equivalent resistance as a function of the capacitance it is possible to choose a capacitor to suit the application.

The capacitors in this study were chosen by plotting the resistance vs capacitance curve and choosing a capacitance value in the highlighted region, which balances capacitor size and equivalent resistance. By choosing an operation point in this area the SC cell should operate within the partial-charge mode. The equivalent resistance curve is shown in Figure 13.

Although the insertion of the ICT does not provide a current division in the capacitor itself, the total power is reduced between the cells, which makes it possible to design SC cells rated for lower power levels in each converter leg. Besides that, with a lower power rating for each leg, faster switches can be used, which reduces the capacitor size.

*D. Intercell Transformer*

The ICT can be designed in several configurations according to the number of legs that is desired to share the input current. There are different configurations that allow the implementation of the ICT with more or less cores. In some configurations more ICTs can be cascaded for an easier implementation with commercial cores [38]. On the other hand, using a single ICT for all phases can reduce the number of magnetic cores used in a practical implementation [32].

The ICT is built with a symmetrical core (all legs have the same reluctance), and each leg of the core has a winding with the same number of turns, so that the average flux in the core is zero. Thus, the coupling factor of the ICT is given by (1).

Each winding is connected to a leg. Each leg is switched with a carrier wave phase-shifted in 360°/n each. In this study, a three-phase ICT was implemented with a single gapped core used to equalize the reluctances of the legs, as proposed by [27]. The current ripple in the ICT legs can be calculated by analyzing the voltages on the windings, given by

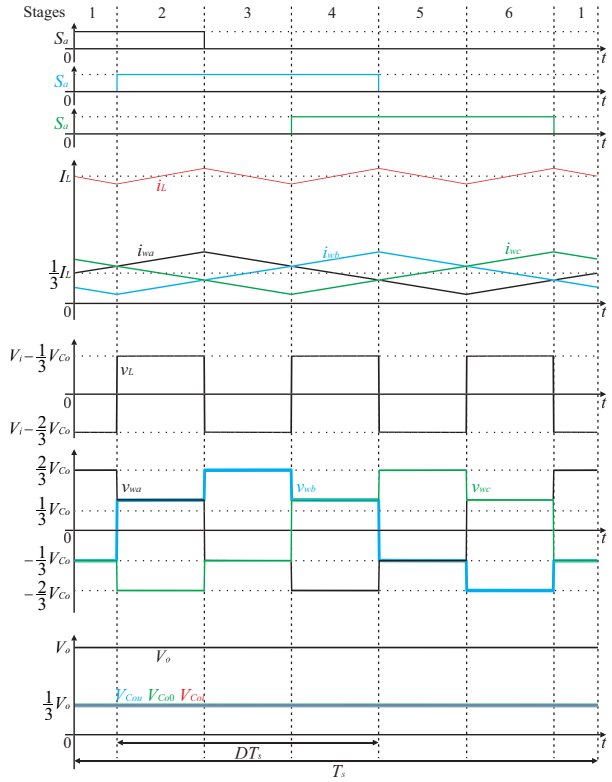
$$V_{wi} = L_{ii}\frac{di_{wi}(t)}{dt} + \sum_{j=1\wedge j\neq i}^{n} M_{ij}\frac{di_{wj}(t)}{dt}. \quad (9)$$

In some converters that use transformers it is common to use a model with a magnetizing inductance and leakage inductances, but since the coupling factor of the ICT is not 1, the mutual inductance matrix is a more practical model to calculate the current ripple in the windings.

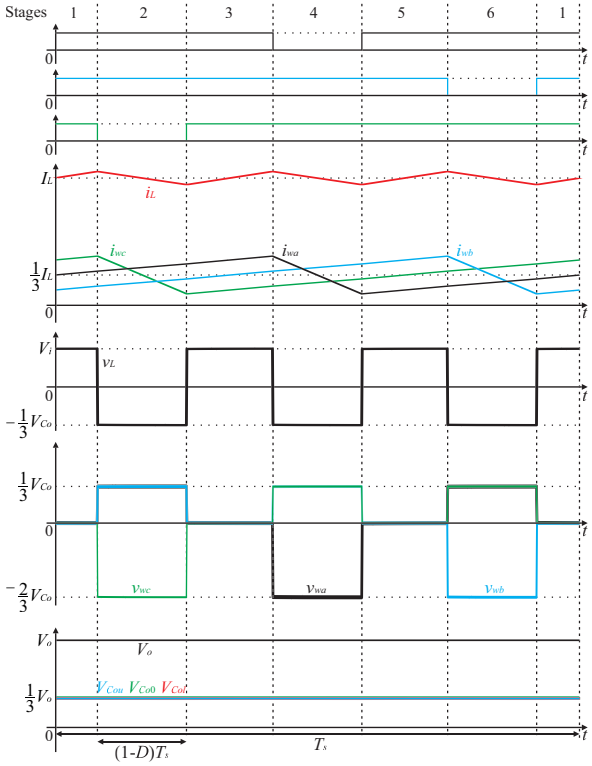
The current ripple can be analyzed for one operational stage and the equation can be rewritten for a three-phase transformer in a matrix form, given by

$$\begin{bmatrix} L_{aa} & M_{ab} & M_{ac} \\ M_{ba} & L_{bb} & M_{bc} \\ M_{ca} & M_{cb} & L_{cc} \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{wa} \\ \Delta i_{wb} \\ \Delta i_{wc} \end{bmatrix} = \begin{bmatrix} V_{wa}\Delta t \\ V_{wb}\Delta t \\ V_{wc}\Delta t \end{bmatrix} \quad (10)$$

where $\Delta i_{wi}$ is the current ripple in the winding $w_i$ and $\Delta t$ is the period of the operational stage that is being analyzed. Considering that the ICT is symmetrical, (10) can be rewritten




Region *B*




Region *C*

Fig. 11. Main waveforms in regions *B* and *C*.

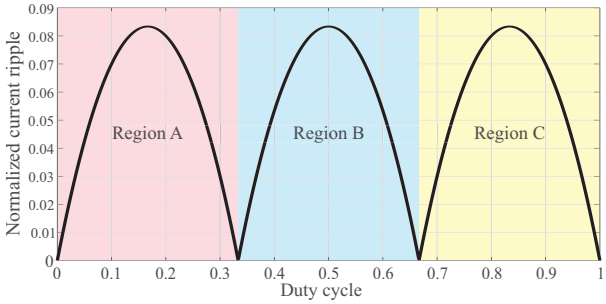



Fig. 12. Normalized input current ripple.

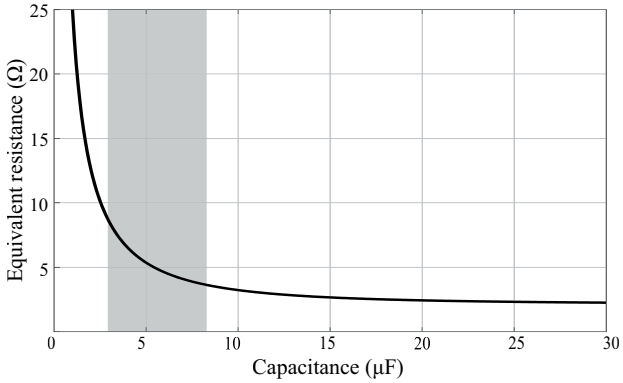



Fig. 13. Equivalent resistance vs capacitance.

as

$$\begin{bmatrix} L_{ii} & -\frac{L_{ii}}{2} & -\frac{L_{ii}}{2} \\ -\frac{L_{ii}}{2} & L_{ii} & -\frac{L_{ii}}{2} \\ -\frac{L_{ii}}{2} & -\frac{L_{ii}}{2} & L_{ii} \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{wa} \\ \Delta i_{wb} \\ \Delta i_{wc} \end{bmatrix} = \begin{bmatrix} V_{wa}\Delta t \\ V_{wb}\Delta t \\ V_{wc}\Delta t \end{bmatrix}. \quad (11)$$

The resulting system cannot be solved in the way it is currently written because the equations are linearly dependent. It is known that the sum of the instant currents in the ICT is equal to the input inductor current, thus a complementary equation can be substituted in the system to make it solvable, resulting in

$$\begin{bmatrix} L_{ii} & -\frac{L_{ii}}{2} & -\frac{L_{ii}}{2} \\ -\frac{L_{ii}}{2} & L_{ii} & -\frac{L_{ii}}{2} \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{wa} \\ \Delta i_{wb} \\ \Delta i_{wc} \end{bmatrix} = \begin{bmatrix} V_{wa}\Delta t \\ V_{wb}\Delta t \\ \Delta i_L \end{bmatrix}. \quad (12)$$

The system is then solved and the ICT winding ripple values are isolated

$$\begin{cases} \Delta i_{w1} = \frac{\Delta i_L}{3} - \frac{2V_{w2}\Delta t}{3L_{ii}} - \frac{2V_{w3}\Delta t}{3L_{ii}} \\ \Delta i_{w2} = \frac{\Delta i_L}{3} - \frac{2V_{w1}\Delta t}{3L_{ii}} - \frac{2V_{w3}\Delta t}{3L_{ii}} \\ \Delta i_{w3} = \frac{\Delta i_L}{3} - \frac{2V_{w1}\Delta t}{3L_{ii}} - \frac{2V_{w2}\Delta t}{3L_{ii}} \end{cases}. \quad (13)$$

Since the ripple in all windings is the same, the total ripple in the switching period can be calculated for each region by summing the ripple values for either all the stages that the switch of a phase is ON or all the stages that the respective switch is OFF. Therefore, the current ripple in each region for

a winding of the ICT is given by

$$\begin{cases} \Delta i_{wi}^{RegionA} = \frac{\Delta i_L}{3} + \frac{4dV_o}{9(m_u+m_l+1)L_{ii}f_s} \\ \Delta i_{wi}^{RegionB} = \frac{\Delta i_L}{3} + \frac{4V_o}{27(m_u+m_l+1)L_{ii}f_s} \\ \Delta i_{wi}^{RegionC} = \frac{\Delta i_L}{3} + \frac{4(1-d)V_o}{9(m_u+m_l+1)L_{ii}f_s} \end{cases}. \quad (14)$$

*E. Voltage and Current Stress*

The voltage on the semiconductor devices is the same as in the capacitors, since the switches and diodes are associated in parallel with one or more capacitor when it is turned OFF. Thus, the voltage stress on the devices is given by

$$V_{s,d} = V_{Co,s} = \frac{V_o}{m_u + m_l + 1}. \quad (15)$$

The current stress on the devices is calculated by simplifying the SC cell, considering that it operates with a very high switching frequency. This simplification is made because the SC cell presents a very non-linear behavior, which makes an analytical solution for the current stress impractical if the non-idealities of the SC cell are considered. Another simplification for the analysis is to assume that the currents in the ICT are balanced, therefore

$$I_{wa} = I_{wb} = I_{wc} = \frac{I_L}{n}. \quad (16)$$

If there is any current imbalance, the equations for calculating the current in the devices of the respective leg must consider Iwa instead of the simplification $I_L/n$.

The average current on the diodes is a fraction of the total output current, given by

$$I_D = \frac{I_o}{n} \quad (17)$$

where $n$ is the number of legs and $I_o$ is the average output current.

Knowing the average current during an operational stage, it is possible to calculate the instant current values in each stage, described by

$$\begin{cases} i_{Deven}^{st1} = \frac{I_o}{nD} \\ i_{Dodd}^{st2} = \frac{I_o}{n(1-D)} \end{cases}. \quad (18)$$

The switch current is given by

$$\begin{aligned} i_{Si}^{st1} &= \frac{i_L}{n} + \sum_{j=2,4,\ldots}^{2m_u} i_{Diuj} + \sum_{j=2,4,\ldots}^{2m_l} i_{Dilj} \\ &= \frac{i_L}{n} + (m_u + m_l)\frac{I_o}{nD} \end{aligned}. \quad (19)$$

The RMS values of the switch and diode currents obtained from (14) and (15), given by

$$\begin{cases} I_{Si}^{RMS} = \frac{\sqrt{D}}{n}\left(i_L + (m_u+m_l)\frac{I_o}{D}\right) \\ I_{Dieven}^{RMS} = \frac{I_o\sqrt{D}}{nD} \\ I_{Diodd}^{RMS} = \frac{I_L\sqrt{1-D}}{n(m_u+m_l+1)} \end{cases} \quad (20)$$

where $m_u$ and $m_l$ are, respectively, the number of SC cells employed in the leg $i$.

## III. EXPERIMENTAL RESULTS

A prototype was built to evaluate the proposed concept using the specifications shown in Table I A photograph of the prototype used for the experiments is shown in Figure 14, its power density is close to 1.2 kW/L.

**TABLE I**
**Converter Specifications**

| Specification | Value |
|---|---|
| Rated power | 3 kW |
| Input voltage | 200 V |
| Output voltage | 1200 V |
| Switching frequency | 100 kHz |
| Input inductor | 74 $\mu$ H |
| ICT self inductances | 122 $\mu$ H |
| Cell capacitors $C_s$ | 5.6 $\mu$ F |
| Output capacitors $C_o$ | 3 $\times$ 5.6 $\mu$F |
| MOSFETs | SCT3080AL |
| $R_{dson}$ | 80 $m\Omega$ |
| Diodes | C3D04065 |
| $V_F$ | 1.4 V |

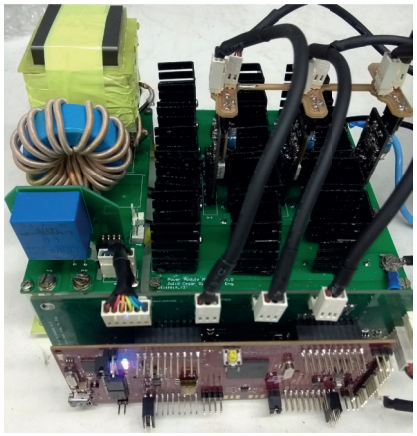


Fig. 14. Photograph of the prototype.

The converter was able to work at the rated power level and provide a voltage gain near 6 (200.8 V to 1.187 kV) working with a duty cycle value at 0.5. The input and output voltages of the converter operating at rated power are depicted in Figure 15. It should be noted that the input current presents low ripple at the frequency of 300 kHz. The main advantages of the proposed concept are the capability of dividing the voltage in the components through the SC cells and sharing the input current through the coupled inductor. The coupled inductor also reduces the current ripple in the input inductor by multiplying the frequency and reducing the voltage levels in the inductor for each topological state. The current sharing between the windings of the coupled inductor are shown in Figure 16.

It is noticed that the inductor current ripple is significantly lower than the coupled inductors. In this figure, it is also possible to see the main limitation of the proposed converter that is the current imbalance in the coupled inductor, in which the windings $w_a$, $w_b$, and $w_b$ RMS currents are, respectively, 5.56 A, 4.68 A and 5.48 A. This imbalance did not cause any major issue in the converter in this study, but a

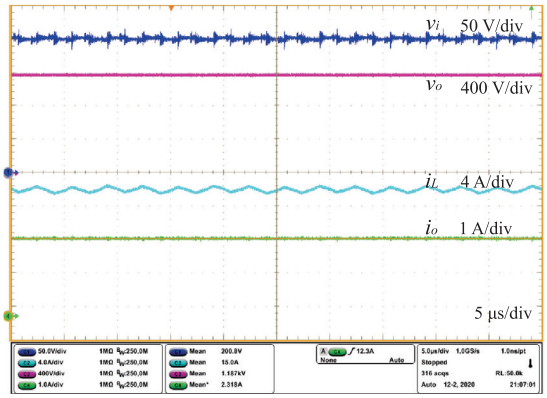



Fig. 15. Rated power operation (The voltage and current values indicated are the average values).

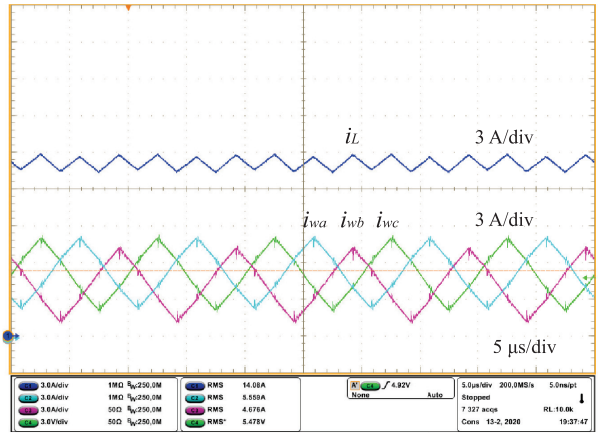



Fig. 16. Current in the windings and input inductor.

larger imbalance could result in an unequal power distribution between the devices, which could result in overheating.

The results in this paper were taken with a constant duty cycle to verify the steady state open loop performance. The imbalance of the currents in interleaved converters are usually due to slight differences in the duty cycle of the converter legs, which can be caused by some nonidealities of the gate drivers. In this work the converter was tested without an active control; however, there are studies in the literature that propose active techniques to solve the imbalance issue in interleaved converters, such as using the Lunze transformation to derive the currents as differential and common-mode currents [32], and then controlling the differential mode currents to a zero reference. Another approach proposed by [39] is reading the differences in the voltage ripple to avoid using additional current sensors.

The current ripple in the inductor is about 1.5 A. The inductor was designed to operate with a 10% ripple at the rated voltage gain, which is the operation point where it presents the highest ripple in the region B, as shown in the theoretical analysis. The current ripple in the ICT windings is under 5.7 A and the calculated value was 5.44 A, which is a reasonable result considering the high frequency resonances that occur at the moment of the switching and affect the measurements.

The main limitation of interleaved is that a slight difference between the duty cycle of the switches (caused by the control or driver circuits) can affect the current balance and, in cases where there is too much difference between the current in the windings, active control techniques must be used to achieve proper current balance. Other drawback in the implementation of a topology with the input current divided by three is the implementation of the coupled inductor, since the commercially available cores are asymmetric. The way the ICT is built can affect the relation between the self and the mutual inductances, thus affecting the input current dynamics. In this study that drawback was compensated by using a gapped core to equalize the reluctance in the legs, as performed in [40].

The integration of the SC cell in the converter provides voltage sharing between the capacitors and a higher static gain. The voltage in the capacitors in an SC cell are self-balanced due to the operation principal of the SC cell. In the SC cells the capacitors are connected in parallel in some stages. Thus, if they are adequately designed, the voltage on the capacitors are the same. This voltage sharing results in a reduced voltage value across the switches and diodes, as depicted in Figure 17. The average experimental output voltage is 1.199 kV and the voltage amplitude in $S_c$ and $D_{cu1}$ are, respectively, 397 V and 404.5 V. The difference might be due to the voltage probes that present slightly different offsets and gains.

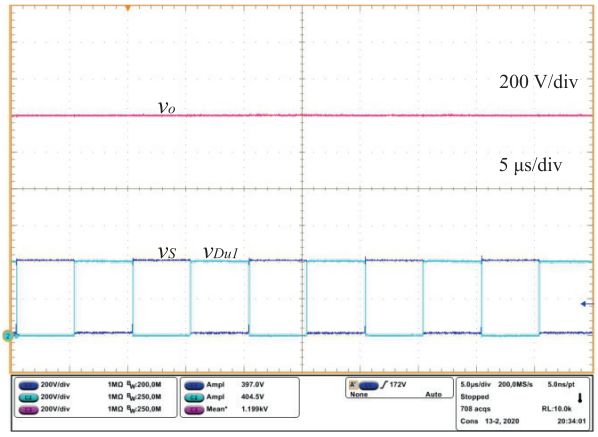



Fig. 17. Voltage on the switch $S_c$, diode $D_{cu1}$.

Although the SC cells reduce the voltage stress on devices and provide a higher voltage gain, they can insert current spikes in the circuit. Since the capacitors are connected in parallel in each stage, the charge and discharge current in the capacitors are only limited by the parasitic resistances and inductances of the circuit. The current in the cell capacitors are shown in Figure 18, where it can be seen that the SC cell operates in partial charge mode, near total charge mode. A Rogowski probe was used to measure the current in the cell capacitors, and since Rogowski probes are affected by low frequency interference, the current values are not very precise. However, the measurements can be used to understand the current shapes in high frequency. These shapes can be smoothed by increasing the capacitance values or using LC circuits instead of using just capacitors.

To evaluate the applicability of the proposed topology, Table II compares it to other high gain topologies with current sharing capability and voltage multiplier techniques, where TBV is the total blocking voltage of the topology, given by

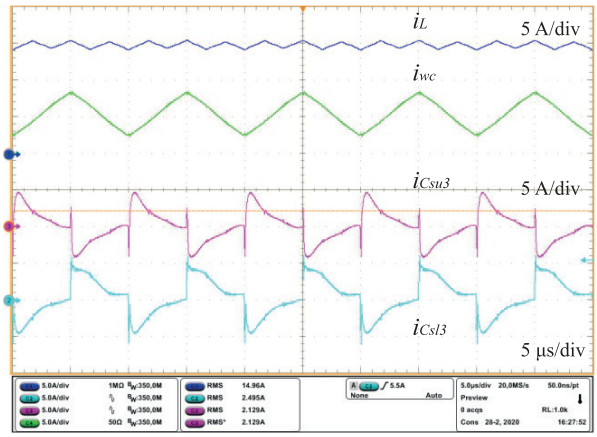



Fig. 18. Current in the cell capacitors $C_{scu}$, $C_{scl}$, coupled inductor winding $w_c$ and input inductor $L$.

$$TBV = \frac{1}{V_o}\sum(V_{Si} + V_{Di}). \tag{21}$$

Some equations are different from the original papers, since most papers do not provide a generalized equation. Other equations were derived for this table, since some studies are incomplete and do not present some of these equations. Thus, all the equations in Table II are adapted to n interleaved cells and m switched capacitor cells. Other equations were not derived in the original papers and were derived in this study for this comparison. In topologies with transformers, the turn ratio is referred to as $a$. In Table II IL means interleaved, and possible means that the specification depends on the way the converter is configured. The proposed topology is considered possibly transformerless in Table II because the ICT could be replaced by single inductors without affecting the static gain or component stress. Balanced series outputs means that, if the converter supplies different sources in series, the voltage will be self balanced.

All topologies shown in Table II can operate with a higher voltage gain than the conventional boost and they use voltage and current sharing techniques. The converters presented in [21] and [41] have the same voltage gain and a lower device count than the proposed topology. However, the voltage stress on the diodes is twice the voltage stress on the converter herein proposed. The converter proposed in [42] also uses less devices and has a higher voltage gain. However, it cannot be generalized to more stages and has a higher voltage stress. The converter proposed in [43] has a higher voltage gain and a lower device count for n>2, but the capacitors do not have the same voltage value and the number of SC cells depend on the number of interleaved cells, increasing the number of inductors in a configuration with a higher voltage gain. The converters proposed by [44]–[47] are non-isolated structures that provide a high voltage gain. However, these converters use a coupled inductor or a transformer, which results in a higher voltage gain. The converters presented in [46] and [47] are designed for a higher power than the previous ones, that were chosen for this comparison for being similar to the proposed concept or having some kind of current sharing and voltage reducing technique. Although the structures shown in [46] and [47] have a higher voltage gain than the proposed concept, they are not generalized for more stages, resulting in a limitation for the voltage and current sharing capabilities, and they do not present balanced series output capacitors.

The converter efficiency curve was measured by evaluating the converter for different output loads using a Yokogawa WT 230 power meter. The maximum efficiency achieved was 98.4% at 30% of the rated power. Additionally, the efficiency obtained at rated power was 97.8%. Both measures can be seen in the efficiency curve, shown in Figure 19.

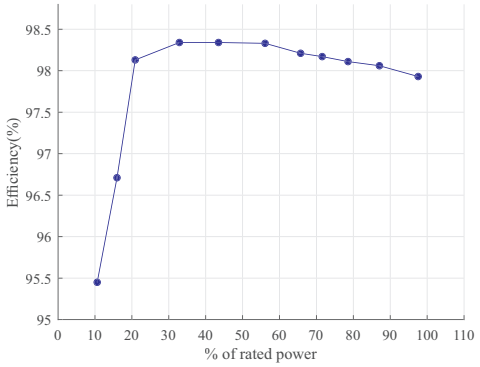



Fig. 19. Efficiency curve.

The losses breakdown of the converter is shown in Figure 20. It should be noted that, although the converter has many diodes, the current is so low that they do not contribute significantly to the power losses. Most losses are due to the magnetic devices.

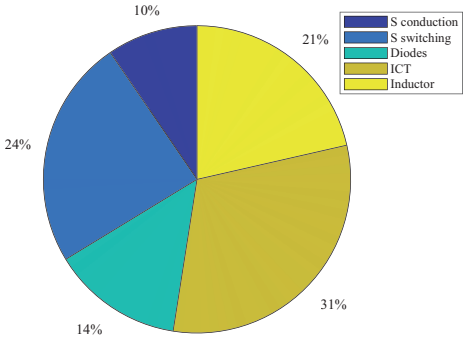



Fig. 20. Loss breakdown.

## IV. CONCLUSIONS

This paper proposed a dc-dc topology concept based on the integration of SC cells and magnetic coupling. The SC cells increased the boost gain and reduced the voltage stress on the devices by a fraction of the output voltage. By reducing the voltage stress on the devices, the converter can be designed with components with a lower voltage rating, which are less expensive, have faster switching times and lower series resistance, thus improving the converter efficiency.

The use of coupled inductors reduced the current stress in the switches, which helped increasing the efficiency of the prototype, achieving an efficiency over 98% in a 3 kW prototype. Furthermore, the coupled inductor also allowed the use of an input filter designed for three times the switching

**TABLE II**
**Topology Comparison**

| Specification | IL Boost | [21], [41] | [42] | [43] | [44] | [45] | [46] | [47] | Proposed |
|---|---|---|---|---|---|---|---|---|---|
| Voltage gain | $\frac{1}{1-D}$ | $\frac{m+1}{1-D}$ | $\frac{2m}{1-D}$ | $\frac{2(m+1)}{1-D}$ | $\frac{m+1+aD}{1-D}$ | $\frac{4+2a}{1-D}$ | $\frac{a_1(D-D^2)+a_2D+1}{D(1-D)}$ | $\frac{3+2a}{1-D}$ | $\frac{m_l+m_u+1}{1-D}$ |
| Minimum possible number of switches | $n$ | $n$ | 2 | $m$ | $n$ | 2 | 1 | 3 | $n$ |
| Minimum possible number of diodes | $n$ | $n(m+1)$ | $2(m+1)$ | $2(m+1)$ | $n(2m+1)$ | 4 | 5 | 6 | $2m_u+2m_l+n$ |
| Minimum possible number of capacitors | 1 | $nm+1$ | $2m+1$ | $2m+1$ | $2mn$ | 4 | 4 | 4 | $2(m_u+m_l)+1$ |
| Maximum voltage stress on semiconductor devices | $V_o$ | $\frac{2V_o}{m+1}$ | $\frac{V_o}{m}$ | $\frac{V_o}{m+1}$ | $\frac{V_o}{m+1+aD}$ | $\frac{(2+2a)V_o}{4+2a}$ | $\frac{DV_o}{(1-D)\left(a_1\left(D-D^2\right)+a_2D+1\right)}$ | $\frac{3}{3+2a}$ | $\frac{V_o}{m_l+m_u+1}$ |
| Current stress in the switches | $\frac{I_i}{n}$ | $\frac{I_i}{n}+\frac{mI_o}{nD}$ | $I_i$ | $\frac{I_i}{m+1}$ | $\frac{I_i}{n}+\frac{I_o(1-D)}{nD}$ | $\frac{I_i}{2}+\frac{2I_o}{D}$ | $I_i+I_o\frac{a_1D+1}{D}$ | $\frac{2}{3}i_i$ | $\frac{i_i}{n}+(m_u+m_l)\frac{I_o}{nD}$ |
| $TBV$ | $2n$ | $2n$ | $\frac{1+2m}{m}$ | $\frac{3m+2}{m+1}$ | $\frac{(m+1)n}{m+1+aD}$ | $\frac{10+4a}{4+2a}$ | $\frac{D(5a_2+1)}{(1-D)\left(a_1\left(D-D^2\right)+a_2D+1\right)}$ | $\frac{15+4a}{3+2a}$ | $2\frac{m_l+m_u+n}{m_l+m_u+1}$ to $2n$ |
| Self-balanced capacitors | NA | Yes | Yes | Yes | Yes | No | No | Yes | Yes |
| Generalized for more IL cells | Yes | Yes | No | Yes | Yes | No | No | No | Yes |
| Transformerless | Yes | Yes | Yes | Yes | No | No | No | No | Possible |
| Balanced series outputs | NA | Yes | Yes | No | No | No | No | No | Yes |
| Line-load common ground | Yes | Yes | No | Yes | No | No | Yes | Yes | Possible |
| Maximum efficiency | | 97.9% | 94.16% | 94.6% | 94.1% | 95% | 94.5% | 88% | 98.4% |
| Full load efficiency | | 95.3% | 90% | 93.8% | 89% | 93.2% | 90.5% | 88% | 97.8% |

frequency.

The main limitations of the proposed topology are the current spikes of the cell capacitors, which can be reduced by increasing the capacitance value, working with higher switching frequency or inserting more legs to reduce the power processed by each leg. Another limitation is the slight imbalance in the coupled inductor, which can affect the converter losses and make some components overheat if the imbalance is too significant. The current imbalances issues can be overcome by using active control techniques used in conventional boost converters with multistate switching cells.

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