DESIGN AND IMPLEMENTATION OF A T-TYPE BASED TOPOLOGY FOR GRID-CONNECTED CURRENT-SOURCE INVERTERS IN PV APPLICATIONS

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***Abstract* – This paper presents a novel non-isolated 5-level inverter for interfacing renewable sources to the power grid. It consists of a modified T-type converter with an HERIC-based AC decoupling strategy. The 5-level output voltage is filtered by a passively damped LCL filter, resulting in a high power density structure. Experimental results on a scaled-down 250 W prototype are presented to validate the operating principle of the proposed topology and show a high efficiency over the entire output power range. Besides, the injected current complies with the IEEE 1547-2018 specifications regarding harmonic content until the 10th harmonic, using a classical PI controller with an additional feedforward term.**

***Keywords* – Current Controlled Inverter, Grid-Connected, LCL Filter, Multilevel Inverter, PV Applications.**

I. INTRODUCTION

One of the most popular renewable energy resources for commercial and residential purposes is solar power harvested through photovoltaic arrays (PV), which utilization has increased throughout the last decade in the whole world [1]. In this context, there is great interest in developing more efficient power converters with low current THD to inject the harvested energy into the power grid. Usually, two-stage transformerless converters are preferred for low power applications, since they can step up the input voltage and modulate the current to be injected into the AC grid, with a reduced component count and higher power density. The focus of this article is the DC-AC stage of such converters, where the only assumption about the DC-DC stage is that the PV voltage is raised above the peak voltage of the power grid.

In the literature it can be found three approaches for power injection into the grid: topologies based on an inverter operating as a voltage source (VSI), a quasi-impedance or impedance source converter [2] and current source inverters (CSI). In this article, the latter option is chosen, as it enables more accurate control of the harmonic content of the injected current despite the grid voltage harmonic distortion due to external factors. In addition, it is more resilient to short-circuit in the grid [3]. A detailed review of several topologies for grid-connected applications is presented in [4].

Manuscript received 07/12/2022; first revision 08/24/2022 and accepted for publication 11/30/2022, by recommendation of Editor Telles Brunelli Lazzarin. http://dx.doi.org/10.18618/REP.2022.4.0032

The T-type converter, among other multilevel topologies like the ANPC, H5, H6, and HERIC converters, is a proper candidate to interface with the AC power grid of a multi-stage renewable source converter, since it requires a smaller output filter compared to the two- or three-level inverters and reduces the voltage stress on the switches. In particular, several approaches for 5-level T-type inverters have been presented in the recent literature.

In [5], a three-phase 5-level inverter with flying capacitors is presented. The main drawback is the increased component count since the working principle depends on a complex array of switches that allows the restructuration of the topology in different redundant ways to produce the multilevel output and balance the voltages of the flying capacitors. In [6], a T-type inverter with two additional diodes and transistors is proposed to achieve a 5-level output voltage. Similarly, the authors in [7] suggest a 5-level T-type inverter with a multistate switching cell designed to divided the current among the switches. However, both experimental results show a decreasing efficiency with increasing output power, rendering it unable to scale up to medium-high power applications. An alternative way to provide five voltage levels with a T-Type-based topology is presented in [8]. It has a reduced number of switching devices and two of them can operate at the line frequency. Nonetheless, the power losses among the switches become very different, in addition to having a common mode voltage with higher dv/dt, which can lead to severe leakage currents.

A novel modulation strategy for the H6 bridge is proposed in [9] in order to obtain a novel five-level single-phase inverter. However, the common-mode voltage of the H6 can no longer be kept constant, and the leakage current becomes an issue. The article [10] presents a novel modulation strategy for a 5-level T-type standard inverter, in which the transistor leg without connection to the DC bus capacitor is switched at the line frequency, thus reducing the switching losses. Nevertheless, the proposed output filter is a single inductor, which decreases the overall power density compared to other more advanced circuits that achieve the same switching harmonics attenuation with less volume. In this matter, high-order passive filters are usually preferred in power converters to cancel out high-frequency harmonics, since they reduce the size and cost of the converter [11]. However, the filter resonance peaks require the addition of active [12] or passive damping [13], [14].

The article [15] proposes a cascaded multilevel inverter topology, resulting from the combination of a HERIC

converter and an additional transistor leg that connects the inverter DC bus to either the full PV input source, or its lower half. However, it produces an asymmetrical utilization of the PV array, thus reducing drastically the power density of the system as a whole. In [16] a novel F-type inverter is proposed as a more efficient alternative to a T-type inverter. However, it relies on a higher component count and outputs a three-level voltage, requiring a larger output filter to achieve a low enough voltage harmonic distortion. In [17], a 5-level inverter topology is presented. The main advantage of this configuration is that the PV array negative terminal is directly connected to the neutral terminal of the grid voltage, enabling both an almost zero leakage current and stepping up the input voltage. Nevertheless, the circuit is composed of many passive elements including series capacitors, which usually cause problems in the control law design.

In this article, a modified T-type 5-level inverter topology is proposed, along with an In-Phase Modulation (IPD) based modulation technique. The topology is derived from the combination of a hybrid T-type converter with the AC decoupling cell of the HERIC-AC converter. Its 5-level output voltage allows reducing the output filter sizing and volume, hence rendering it a proper candidate for the DC-AC stage of a multi-stage renewable source power converter. Compared to its counterparts (T-type and HERIC converters), the proposed 5-level topology has important advantages, as better-quality output current waveform and less electrical stress in the power semiconductors. In contrast, when compared to other 5-level topologies, the proposed one have a similar behavior, but with a better power loss distribution over the components.

A similar proposal was presented in [18], but it provides neither experimental results for the validation of the topology nor a control design for the converter, even though the proposal considers a single L filter to interface the grid. In contrast, this article presents experimental results over a scaled-down 250W prototype to validate the advantages of the proposed topology, and a more complex filter at the output, capable of decreasing the filter sizing and thus increasing the power density. It also describes the design of a control law that results in low output current harmonic distortion. The article includes a detailed analysis of the voltage and current stresses that the switches and the capacitors must withstand, which the previously cited also failed to include.

Furthermore, in this article, it is also proposed the usage of a passively damped LCL output filter with an optimal design for the damping components to minimize the gain peak around the resonance frequency while retaining the high attenuation rate. The chosen controller is a PI compensator plus an additional feedforward term, although it has already been proven in [19] that this type of controller introduces a phase and amplitude error in the output current. Since this paper focuses on the presentation of the novel topology, improvements in the control strategy are left for future works.

II. PROPOSED TOPOLOGY

Figure 1 shows the schematic circuit of the proposed topology. It consists of a full-bridge inverter with four additional switches arranged to operate as two bidirectional switches with independent gates. One connects the DC bus

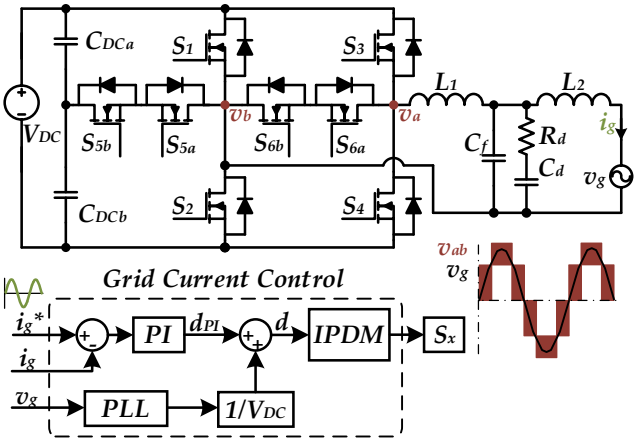


Fig. 1. Proposed 5-level inverter circuit and control strategy for grid-connected applications.

capacitors with one of the inverter's legs in both the midpoints and the other between the inverter legs'. This topology resembles a hybrid T-type converter with an AC decoupling cell like a HERIC-AC converter. This proposed topology allows for a multilevel output voltage to be synthesized, thus lowering the injected current THD and reducing the required output filter size. In this article, a passively damped LCL filter [13] is proposed for the interface with the power grid, since it profits from the advantages of the regular LCL filter, such as higher attenuation and smaller volume, but without the drawbacks that arise from the high-frequency resonance peak.

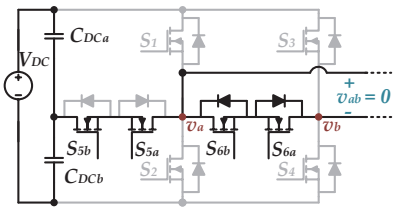
The proposed modulation strategy is based on the in-phase disposition (IPD) level shift strategy. The application of this modulation results in a 5-level output voltage v_{ab}, which arises from five different switching structures, as shown in Figure 2. The voltage harmonics are then filtered out by a low-pass LCL filter, resulting in a pure sine wave output voltage. The operation over a full grid-frequency cycle is composed of six different regions (Ω_i) in which two of the structures are used:

First Region ($0 < \omega_0 t \leq \theta_1$): in this region, the switches S_1, S_2 and S_3 are turned off and the complementary switches S_{5x} are turned on. The switches S_4 and S_{6x} are alternately switched to change between structures (a) and (b). The first one enforces a zero output voltage while the other sets the voltage between the terminals A and B to $V_{dc}/2$.

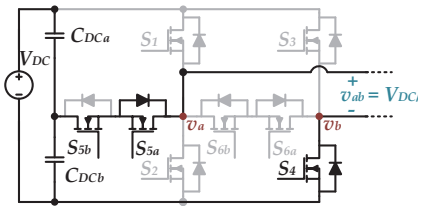
Second Region ($\theta_1 < \omega_0 t \leq \pi - \theta_1$): in this region, the switches S_2, S_3 and S_{6x} are turned off, while the switch S_4 is turned on. The switches S_1 and S_{5x} are alternately switched to change between structures (b) and (c) and thus, the output voltage switches between $V_{dc}/2$ and V_{DC}.

Third Region ($\pi - \theta_1 < \omega_0 t \leq \pi$): this region operates in the same way as the first region.

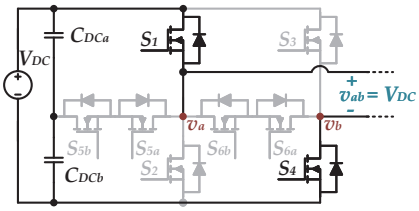
Fourth Region ($\pi < \omega_0 t \leq \pi + \theta_1$): this region starts when the negative semi-cycle begins. Alike in region 1, the switches S_1, S_2, and S_4 are turned off, and the complementary switches S_{5x} are turned on. The switches S_3 and S_{6x} are alternately switched to change between structures (a) and (d) to get the output voltage switching



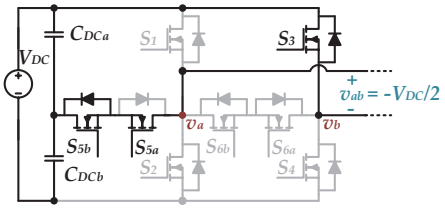
(a) Structure a) $v_{ab} = 0$



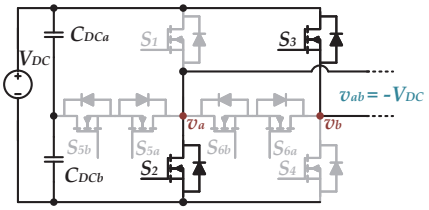
(b) Structure b: $v_{ab} = \frac{V_{DC}}{2}$



(c) Structure c: $v_{ab} = V_{DC}$



(d) Structure d: $v_{ab} = -\frac{V_{DC}}{2}$



(e) Structure e: $v_{ab} = -V_{DC}$

Fig. 2. Converter switching structures used to output a 5-level voltage.

between zero and $-V_{dc}/2$.

Fifth Region ($\pi + \theta_1 < \omega_0 t \leq 2\pi - \theta_1$): in this region, the switches S_1, S_4 and S_{6x} are turned off, while the switch S_3 is turned on. The switches S_2 and S_{5x} are alternately switched to change between structures (d) and (e) and thus, the output voltage switches between $-V_{dc}/2$ and $-V_{DC}$.

Sixth Region ($2\pi - \theta_1 < \omega_0 t \leq 2\pi$): this last region is the same as the fourth region, concluding one full grid voltage period.

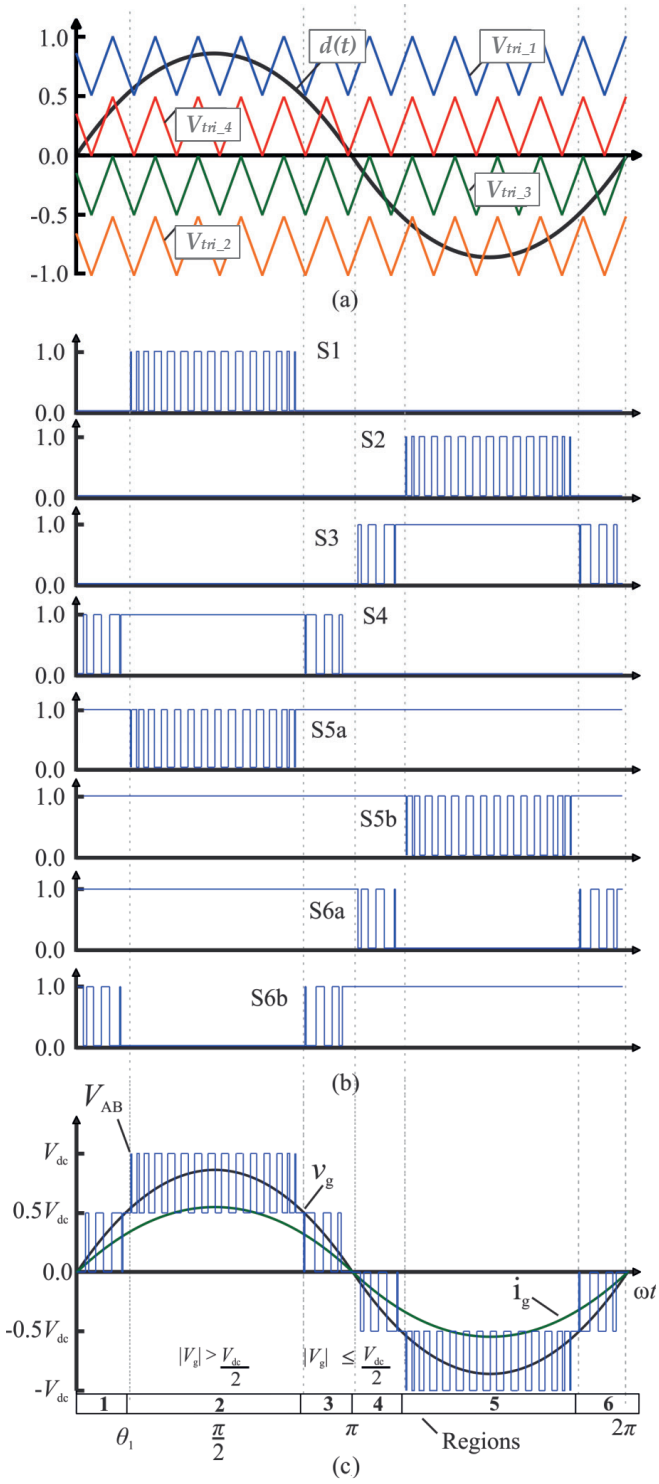


Fig. 3. Theoretical waveforms: (a) triangular carriers and modulating signal; (b) MOSFETs driving signals; (c) voltage v_{ab}, grid voltage and grid current.

This sequence is summarized in Table I. It also includes the common mode voltage $v_{cm} = (v_a + v_b)/2$, which is responsible for the generation of leakage current in transformerless PV systems. As one can note, in any region Ω_i, the maximum dv/dt in the common mode voltage is $V_{DC}/4$, while the frequency remains equal to the switching frequency.

Figure 3.a depicts the IPD modulation presenting its carriers ($V_{tri\_1,2,3,4}$) that will be compared with the

TABLE I
Operating Regions for a 5-level Sinusoidal Output Voltage

Grid voltage v_g	Ω_i	Converter structures	Output voltage v_{ab}	Common mode voltage v_{cm}
$0 < v_g \leq \frac{V_{DC}}{2} \wedge \dot{v}_g > 0$	1	a-b	0 & $\frac{V_{DC}}{2}$	0 & $-\frac{V_{DC}}{4}$
$\frac{V_{DC}}{2} < v_g \leq V_{DC}$	2	b-c	$\frac{V_{DC}}{2}$ & V_{DC}	$-\frac{V_{DC}}{4}$ & 0
$0 < v_g \leq \frac{V_{DC}}{2} \wedge \dot{v}_g < 0$	3	a-b	0 & $\frac{V_{DC}}{2}$	0 & $-\frac{V_{DC}}{4}$
$-\frac{V_{DC}}{2} < v_g \leq 0 \wedge \dot{v}_g < 0$	4	a-d	0&$-\frac{V_{DC}}{2}$	0 & $\frac{V_{DC}}{4}$
$-V_{DC} < v_g \leq -\frac{V_{DC}}{2}$	5	d-e	$-\frac{V_{DC}}{2}$ & V_{DC}	$\frac{V_{DC}}{4}$ & 0
$-\frac{V_{DC}}{2} < v_g \leq 0 \wedge \dot{v}_g > 0$	6	a-d	0 & $-\frac{V_{DC}}{2}$	0 & $\frac{V_{DC}}{4}$

modulating signal (M), thus producing the driving signals for the switching of the MOSFETs (S_1, S_2, S_3, S_4, S_{5a}, S_{5b}, S_{6a}, S_{6b}), as per Figure 3.b. The transition between carriers defines the ending of a region of operation and the start of another one. Then, the 5-level output voltage of the proposed topology results in a sinusoidal current injected into the power grid modeled by the source $v_g = \hat{V}_g sin(2\pi f_g t)$, as shown in Figure 3.c.

III. SWITCH AND PASSIVE COMPONENTS SIZING

This section presents the equations required to select the power switches and the passive filter components. Firstly, the voltage and current stresses of the switches are calculated, assuming that the low-frequency voltage drops on the output filter may be neglected and the output current is purely sinusoidal with a power factor close to unity. This allows modelling the grid as a resistor and simplifies the expressions. After that, the passively damped LCL filter and the DC bus capacitor design equations are presented.

A. Switch Voltage Stress

The voltage stress of each switch varies according to the region the converter is operating in, but to sum up, all transistors have to withstand the total bus voltage V_{DC} in some states. The only exceptions are the switches S_{5a} and S_{5b} whose maximum voltage is half of the bus voltage, due to having one of their terminal directly connected to the bus capacitors midpoint.

B. Switch Current Stress

To compute the current stress of each transistor it is necessary to find an expression for the total output current i_g and the angle θ_1 at which the operation regions change. Assuming that the inverter is injecting pure active power P_{out}, the grid may be modeled as a resistor:

$$R_g = \frac{v_{g\_RMS}^2}{P_{out}} = \frac{\hat{V}_g^2}{2P_{out}}. \tag{1}$$

Then, neglecting the low-frequency voltage drop and phase angle difference in the output filter, the grid current is derived doing:

$$i_g = \frac{\langle v_{ab} \rangle \big|_{Ts}}{R_g}. \tag{2}$$

The average output voltage within a switching period $\langle v_{ab} \rangle \big|_{Ts}$, is a function of the time-varying duty cycle $d(t)$:

$$\langle v_{ab} \rangle \big|_{Ts}(t) = V_{DC} d(t) = V_{DC} M sin(2\pi f_g t), \tag{3}$$

where:

$$M = \frac{\hat{V}_g}{V_{DC}}. \tag{4}$$

The average and RMS current values (I_{Sx_avg} and I_{Sx_RMS}, respectively) for every switch are then calculated as

$$I_{Sx\_avg} = \frac{1}{2\pi} \int_{\theta_i}^{\theta_f} I_{Sx\_Ts\_avg}(i_g) dt, \tag{5}$$

$$I_{Sx\_RMS} = \sqrt{\frac{1}{2\pi} \int_{\theta_i}^{\theta_f} I_{Sx\_Ts\_RMS}(i_g)^2 dt}. \tag{6}$$

where: $I_{Sx\_Ts\_avg}(i_g)$ and $I_{Sx\_Ts\_RMS}(i_g)$ are the average and RMS current in the switch during a switching period T_s, respectively, which are functions of the output current waveform i_g. In (5) and (6), the angles θ_i and θ_f represent the operating region boundaries. In particular, the transition from region 1 to region 2 occurs when $\langle v_{ab} \rangle \big|_{Ts} = V_{DC}/2$ at the angle θ_1:

$$\theta_1 = sin^{-1}\left(\frac{1}{2M}\right). \tag{7}$$

Then, the transition from region 2 to 3 occurs at $\theta_2 = \pi - \theta_1$ and it is extended by symmetry for regions 4, 5, and 6. The resulting expressions for the average and RMS current of each switch are detailed in Appendix A.

C. DC Bus Capacitor

The capacitor sizing must be done such as the voltage ripple over each DC bus capacitor is less than some value Δv_{Cx}. To simplify the analysis, it is assumed that the losses are negligible ($P_{in} = P_{out}$) and that the DC bus capacitors absorb any instantaneous difference between the input and the output power since the former is continuous and the latter is given

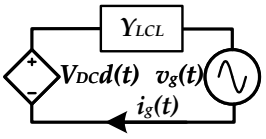


Fig. 4. Simplified model of the output stage of the converter

by $p_{out}(t) = P_{out}(1+\cos(2\omega t))$. Let us consider both the input current and the bus capacitor voltage to be composed of a constant and a time-varying term:

$$i_{in}(t) = I_{in} + \hat{i}_{in}(t) = \frac{P_{out}}{V_{DC}} + \frac{P_{out}}{V_{DC}}\cos(2\omega t), \tag{8}$$

$$v_{Ceq}(t) = V_{Ceq} + \hat{v}_{Ceq}(t). \tag{9}$$

Thus, both time-varying component are related as

$$\hat{v}_{Ceq}(t) = \frac{1}{C}\int \hat{i}_{in}(\tau)d\tau = \frac{P_{out}}{C_{eq}V_{DC}}\int \cos(2\omega\tau)d\tau. \tag{10}$$

Solving the integral leads to the design equation for the DC bus capacitors, which have equal values for a balanced operation:

$$C_1 = C_2 = \frac{P_{out}}{2\omega\Delta v_{Ceq}V_{DC}} = \frac{P_{out}}{\omega\Delta v_{Ceq\%}V_{DC}^2}. \tag{11}$$

Furthermore, the RMS current value that the capacitors must withstand can be derived from (8), obtaining:

$$i_{Ceq\_RMS} = \frac{P_{out}}{V_{DC}\sqrt{2}}. \tag{12}$$

D. Output Filter Design

The output filter employed in the proposed inverter is a passively damped LCL filter. This third-order filter presents a better attenuation (60 dB/dec) than the L or LC filters above the filter resonance frequency, and its implementation is more straightforward than some others like the harmonic traps [11]. Furthermore, it provides less peak gain around the resonance frequency than the classical LCL filter, which requires the addition of virtual damping in the control law to prevent instabilities. Following the design procedure presented in [20], the inductances are calculated as a function of the desired current ripple on the converter side inductor. Besides, they are set to the same value, since that achieves the minimum total inductance, as formerly demonstrated in [14]. In this case, it is proposed to set the maximum current ripple as 50% of the RMS output current:

$$L_1 = L_2 = \frac{V_{DC}}{8f_s}\frac{2v_{g\_RMS}}{P_{out}}. \tag{13}$$

Regarding the capacitors, their values must be such as the resonance frequency is above one-sixth of the switching frequency ($f_r \geq \frac{1}{6}f_s$) which results from a trade-off between high-frequency harmonics attenuation and bandwidth. In this article, both the damping and the filter capacitors (C_d and C_f, respectively) are designed to be equal. Then, their values may be calculated as:

$$C_f = C_d = \frac{1}{2(2\pi f_r)^2(L_1//L_2)}. \tag{14}$$

At last, the damping resistor is calculated as:

$$R_d = Q_{opt}R_0, \tag{15}$$

where:

$$Q_{opt} = \begin{cases} \sqrt{\frac{(5n+4)(n+2)(n+1)}{2n^2(4-n)}} & \longrightarrow n \in (0, 1.3] \\ 2.5 & \longrightarrow n \in (1.3, \infty) \end{cases}. \tag{16}$$

$$n = C_d/C_f = 1, \tag{17}$$

$$R_0 = \sqrt{\frac{L_1//L_2}{C_d + C_f}}. \tag{18}$$

IV. GRID CURRENT CONTROL DESIGN

In this article, a PI+feedforward compensator is proposed for the control of the grid current. The design requires the knowledge of the converter dynamic model when connected to the grid, considering that the measured value is the filter output current i_g. For that purpose, Figure 4 shows an equivalent model of the proposed inverter, in which the output voltage is expressed as:

$$v_{ab}(t) = v_{DC}d(t), \tag{19}$$

considering only its low frequency components. Moreover, the output filter is reduced to a single admittance:

$$Y_{LCL} = \frac{1}{s(L_1+L_2)}\frac{\tau_d s + 1}{\tau_d C_f L_{eq}s^3 + C_{eq}L_{eq}s^2 + \tau_d s + 1}, \tag{20}$$

where:

$$\tau_d = R_d C_d, \tag{21}$$

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2}, \tag{22}$$

$$C_{eq} = C_d + C_f. \tag{23}$$

Both these simplifications lead to the output current calculation as follows:

$$I_g(s) = \left[D(s)v_{DC} - V_g(s)\right]Y_{LCL}. \tag{24}$$

The duty cycle $d(t)$ is strategically set as the sum of two terms:

$$d(t) = \frac{v_g(t)}{V_{DC}} + d_{PI}(t), \tag{25}$$

which results in the output voltage v_{ab} to have two components as well:

$$v_{ab}(t) = v_g(t) + V_{DC}d_{PI}(t). \tag{26}$$

The first term is equal in magnitude but connected in opposition to the grid voltage, thus cancelling each other mutually out. The other one is proportional to output of the PI controller d_{PI} as is responsible for enforcing the current according to the reference signal.

Therefore, by replacing the Laplace transform of (25) in

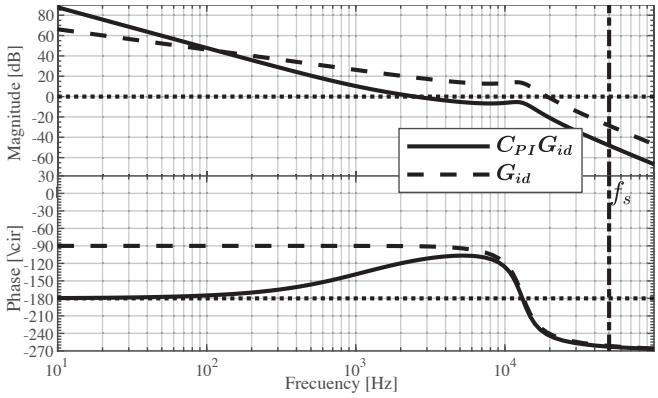


Fig. 5. Bode plot of the open loop (continuous line) and the open loop with the designed controller (dashed line) transfer functions for the proposed converter.

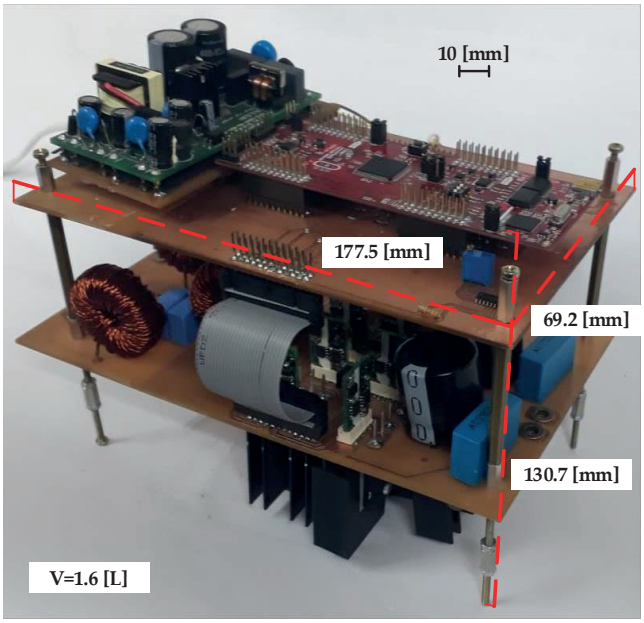


Fig. 6. Photograph of the implemented converter prototype

(24), the transfer function of the grid current is obtained:

$$G_{Igd}(s) = \frac{I_g(s)}{d_{PI}(s)} = V_{DC}Y_{LCL}. \quad (27)$$

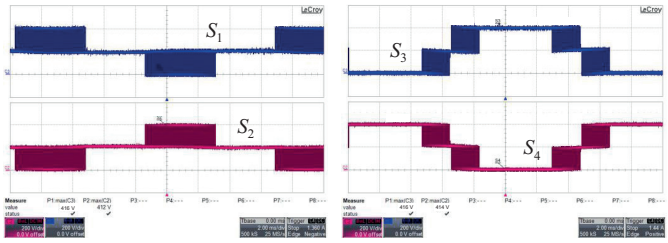
The crossover frequency is set to be equal to a twentieth of the switching frequency to provide reasonably good attenuation of the switching harmonics and, especially, the peak gain at the resonance frequency of the LCL filter ($\omega_{c\_Igd} = \omega_s/20 = 2\pi.50000/20 = 15707.96 rad.s^{-1}$). The phase margin is set equal to 65° to get a damping ratio of $\zeta = 1/\sqrt{2}$ which provides stability and a good transient response. Figure 5 shows the resulting open-loop Bode plots of I_g/d_{PI} transfer function with the designed PI controller, which values are $K_P = 0.1055$ and $K_I = 753.2$.

V. EXPERIMENTAL RESULTS

This section presents the experimental results using the prototype shown in Figure 6 and whose parameters are presented in Table II. It is to be noticed that this topology

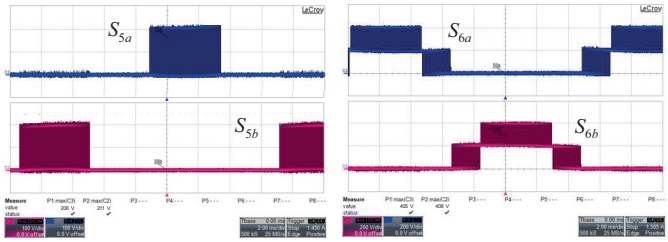
TABLE II
Parameters of the Implemented Converter Prototype

Parameter	Description	Value
P_{out}	Output Power	250 [W]
PF	Power Factor	≈ 1
V_{DC}	DC Input Voltage	400 [V]
$\hat{v}_g$	Grid Peak Voltage	311[V]
f_g	Grid Frequency	60 [Hz]
f_s	Switching Frequency	50 [kHz]
f_r	LCL Resonant Frequency	10 [kHz]
C_{DCa}	DC Bus Capacitor 1	200 [µF]
C_{DCb}	DC Bus Capacitor 2	200 [µF]
L_1	Filter Inductor 1	1.56 [mH]
L_2	Filter Inductor 2	1.56 [mH]
C_f	Filter Capacitor	150 [nF]
C_d	Damping Capacitor	150 [nF]
R_d	Damping Resistor	68 [Ω]
$MOSFETs$	MOSFET Transistor	SCT 3120AL



(a) (b)

Fig. 7. Voltage over the switches S_1, S_2, S_3 and S_4 during a full grid frequency cycle (200 V/div; 2 ms/div).



(a) (b)

Fig. 8. Voltage over the switches S_5a, S_5b, S_6a and S_6b during a full grid frequency cycle (200 V/div; 2 ms/div).

is not appropriate for such low power outages due to its relatively high component count. However, the experimental setup implemented for this article is a scaled-down prototype for demonstration purposes of the advantages previously discussed.

Figure 9 shows the five-level output voltage v_{ab} waveform during three grid frequency cycles, whereas Figure 10 presents the waveform of the common mode voltage v_{cm}, validating the proposed modulation strategy. Figures 7 and 8 show the voltage across each switch, proving the maximum voltage transition is about half the input voltage, rendering lower voltage stresses compared to other commonly used topologies. Figures 11, 13, and 15, show experimental results of the proposed converter injecting power into the power grid operating with 100%, 75%, and 50% of the designed power rating ($P_{out} = 250(W)$), respectively. These measurements

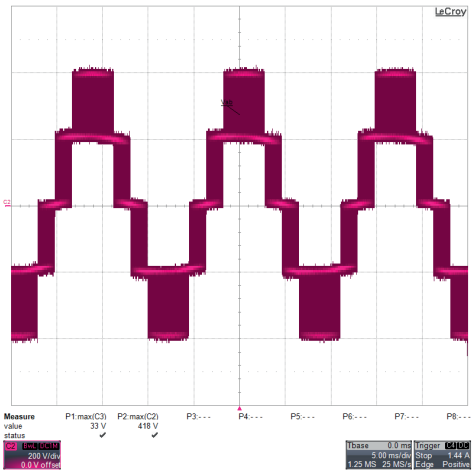


Fig. 9. Output voltage v_{ab} of the converter before the LCL filter (200 V/div; 5 ms/div).

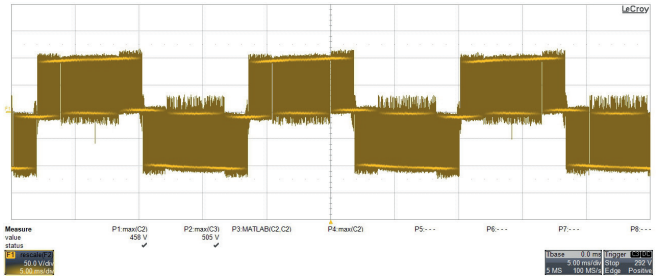


Fig. 10. Common mode voltage v_{cm} of the converter (50 V/div; 5 ms/div).

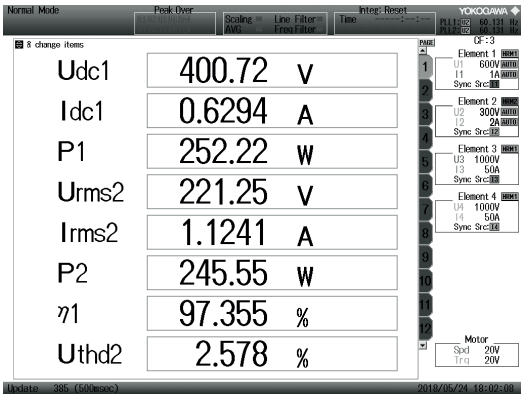


Fig. 11. Power analyzer measurement of the input voltage and current when operating at 100% of the rated power ($P_{out} \approx 250(W)$).

include the efficiency of the converter as well as the steady-state values for the input and output currents and voltages.

Figures 12, 14, and 16, show the harmonic content of the output current in each case, compared to the limits imposed by the IEEE 1547-2018 standard [21]. The waveform for the injected current and output voltage are included as well. Each one presents an adequate performance of the designed controller, although the inherent phase mismatch of the PI controller is present, as discussed in a previous section. It is clear that the efficiency increases as the output power does, which is a desirable trait for a power converter, and that is portrayed in Figure 17, where the measured efficiency at more operating points is plotted against the measures output power

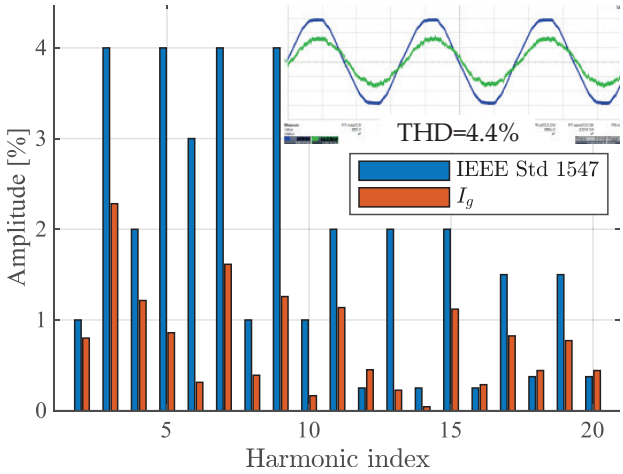


Fig. 12. Harmonic content of the injected current when operating at 100% of the rated power ($P_{out} \approx 250(W)$), compared to the limits established by the IEEE 1547-2018 standard. Top right corner: Injected current i_g (green) and grid voltage v_g (blue).

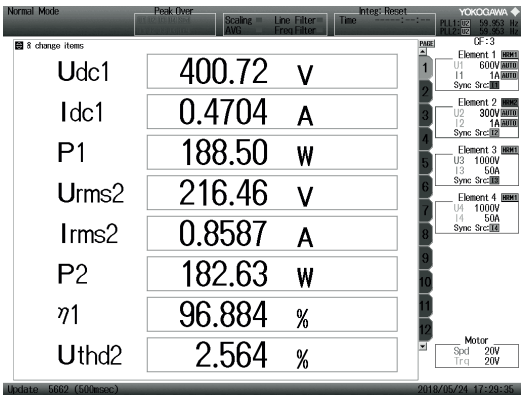


Fig. 13. Power analyzer measurement of the input voltage and current when operating at 75% of the rated power ($P_{out} \approx 187.5(W)$).

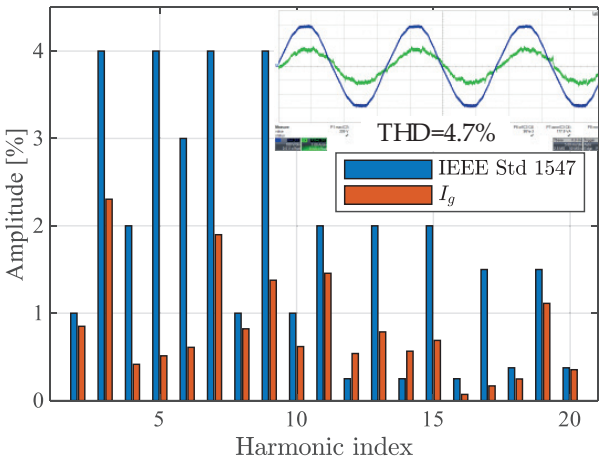


Fig. 14. Harmonic content of the injected current when operating at 75% of the rated power ($P_{out} \approx 187.5(W)$), compared to the limits established by the IEEE 1547-2018 standard. Top right corner: Injected current i_g (green) and grid voltage v_g (blue)

for each case. Furthermore, it is important to compute the weighted efficiency ($\eta_{CEC} = 95.38$) as proposed in [22]:

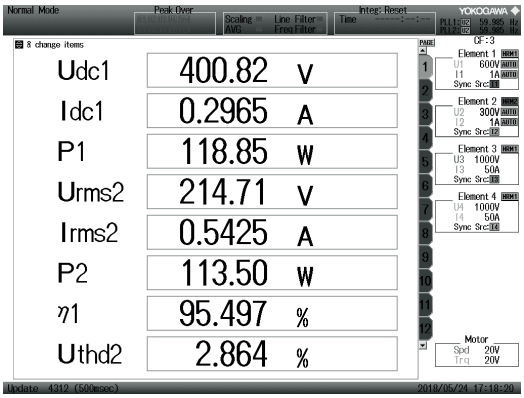


Fig. 15. Power analyzer measurement of the input voltage and current when operating at 50% of the rated power ($P_{out} \approx 125(W)$).

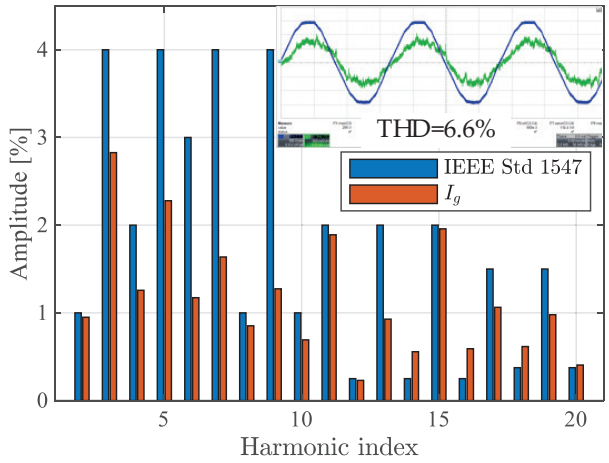


Fig. 16. Harmonic content of the injected current when operating at 50% of the rated power ($P_{out} \approx 125(W)$), compared to the limits established by the IEEE 1547-2018 standard.. Top right corner: Injected current i_g (green) and grid voltage v_g (blue)

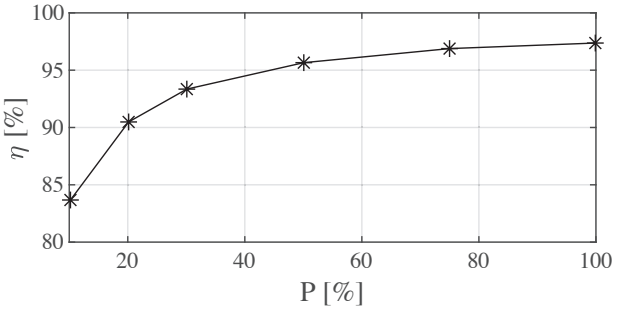


Fig. 17. Efficiency (%) of the converter with respect to the nominal output power percentage.

VI. CONCLUSIONS

This article presents a new topology for renewable sources interfacing with a single-phase power grid. It results from adding AC decoupling with an additional bidirectional switch to a T-type inverter. An optimal passively damped LCL output filter is implemented, since it has the same attenuation rate as the traditional LCL but with a lower gain around the resonance frequency which simplifies the control design.

The presented experimental results prove the advantages of the proposed topology, which presents high-efficiency operation for most of the output power range, lower voltage stresses on the switches, and lower output voltage and current THD due to its 5-level output. In particular, the current harmonic content complies with the IEEE 1547-2018 limits at least until the 10th harmonic.

Further work is to be done with this topology, adopting a Fictive-Axis 5-level SVM, which should result in an optimal switching sequence. Also, a more complex control strategy could be implemented to further improve the THD in the whole power range, as well as to improve the disturbance rejection and robustness to parametric uncertainty, which was not analyzed in this article.

APPENDIX

A. Average and RMS Current Equations for Each Switch

$$I_{S1,2\_avg} = \frac{7I_o}{44}\left(2M\cos(\theta_1)\sin(\theta_1) + \pi M - 2M\theta_1 - 2\cos(\theta_1)\right), \tag{28}$$

$$I_{S1,2\_RMS} = \frac{7I_o}{43}\sqrt{\begin{array}{l}-6\cos(\theta_1)\sin(\theta_1) - 8M\cos(\theta_1)^3 + \ldots \\ \ldots + 24M\cos(\theta_1) + 6\theta_1 - 9.42\end{array}}, \tag{29}$$

$$I_{S3,4\_avg} = \frac{I_o}{\pi}\left(-M\left(\cos(\theta_1)\sin(\theta_1) - \theta_1\right) + \cos(\theta_1)\right) \tag{30}$$

$$I_{S3,4\_RMS} = \frac{22I_o}{39}\sqrt{\begin{array}{l}M\left(\frac{2}{3}\cos(\theta_1)^3 - 2\cos(\theta_1) + \frac{4}{3}\right) + \ldots \\ \ldots + 0.5\cos(\theta_1)\sin(\theta_1) - 0.5\theta_1 + 0.785\end{array}}, \tag{31}$$

$$I_{S5a,5b\_avg} = 0, \tag{32}$$

$$I_{S5a,5b\_RMS} = 0.5641 I_o\sqrt{0.5\cos(\theta_1)\sin(\theta_1) - 0.5\theta_1 + \frac{4}{3}M}, \tag{33}$$

$$I_{S6a,6b\_avg} = 0, \tag{34}$$

$$I_{S6a,6b\_RMS} = 0.325 I_o\sqrt{\begin{array}{l}-3\cos(\theta_1)\sin(\theta_1) - 4M\cos(\theta_1)^3 + \ldots \\ \ldots + 12M\cos(\theta_1) + 3\theta_1 - 8M\end{array}}. \tag{35}$$

ACKNOWLEDGEMENTS

The authors would like to thanks the National Council for Scientific and Technological Development (CNPq) for the financial support (Process number: 316053/2021-0).

REFERENCES

[1] M. H. Saeed, W. Fangzong, B. A. Kalwar, S. Iqbal, "A Review on Microgrids' Challenges and Perspectives", *IEEE Access*, vol. 9, pp. 166502–166517, Dec. 2021, doi:10.1109/ACCESS.2021.3135083.

[2] H. Komurcugil, S. Bayhan, F. Bagheri, O. Kukrer, H. Abu-Rub, "Model-Based Current Control for Single-Phase Grid-Tied Quasi-Z-Source Inverters With

Virtual Time Constant", *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 8277–8286, Feb. 2018, doi:10.1109/TIE.2018.2801778.

[3] M. Rajeev, V. Agarwal, "Single Phase Current Source Inverter With Multiloop Control for Transformerless Grid–PV Interface", *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2416–2424, May-Jun. 2018, doi:10.1109/TIA.2017.2788414.

[4] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes, F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 805–835, Mar. 2020, doi:10.1109/JESTPE.2019.2908672.

[5] S. Xu, J. Zhang, X. Hu, Y. Jiang, "A Novel Hybrid Five-Level Voltage-Source Converter Based on T-Type Topology for High-Efficiency Applications", *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4730–4743, Sept.-Oct. 2017, doi:10.1109/TIA.2017.2713762.

[6] S. K. Kuncham, K. Annamalai, N. Subrahmanyam, "A Two-Stage T-Type Hybrid Five-Level Transformerless Inverter for PV Applications", *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9510–9521, Sept. 2020, doi:10.1109/TPEL.2020.2973340.

[7] R. G. d. Almeida Cacau, R. P. Torrico-Bascopé, J. A. F. Neto, G. V. Torrico-Bascopé, "Five-Level T-Type Inverter Based on Multistate Switching Cell", *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3857–3866, Nov.-Dec. 2014, doi:10.1109/TIA.2014.2311508.

[8] S.-J. Park, F.-S. Kang, M. H. Lee, C.-U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme", *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 831–843, May 2003, doi:10.1109/TPEL.2003.810837.

[9] G. Buticchi, E. Lorenzani, G. Franceschini, "A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems", *IEEE Transactions on Industrial Electronics*, vol. 60, no. 3, pp. 906–918, March 2013, doi:10.1109/TIE.2012.2189538.

[10] G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazún, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez, J. M. S. Zuñiga, "A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 140–150, March 2018, doi:10.1109/JESTPE.2017.2726989.

[11] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, C. L. Bak, "A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 54–69, March 2016, doi:10.1109/JESTPE.2015.2507203.

[12] M. A. Awal, L. D. Flora, I. Husain, "Observer Based Generalized Active Damping for Voltage Source Converters With LCL Filters", *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 125–136, Jan. 2022, doi:10.1109/TPEL.2021.3093504.

[13] W. Wu, Y. He, T. Tang, F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter", *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4339–4350, Oct. 2013, doi:10.1109/TIE.2012.2217725.

[14] P. Channegowda, V. John, "Filter Optimization for Grid Interactive Voltage Source Inverters", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 4106–4114, Dec. 2010, doi:10.1109/TIE.2010.2042421.

[15] S. Jain, V. Sonti, "A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multilevel Inverter for PV Systems", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2865–2875, April 2017, doi:10.1109/TIE.2016.2633537.

[16] C. I. Odeh, A. Lewicki, M. Morawiec, D. Kondratenko, "Three-Level F-Type Inverter", *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11265–11275, Oct. 2021, doi:10.1109/TPEL.2021.3071359.

[17] B. Karami, X. Yang, M. Samizadeh, W. Chen, M. Kamranian, A. Hassan, M. A. Houran, "A New 5-level Grid-Connected Transformerless Inverter with Eliminating Leakage Current", *in IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, pp. 454–459, 2020, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367920.

[18] G. Vázquez, J. M. Sosa, M. A. Juarez, P. R. Martinez-Rodriguez, G. Escobar, "A Modulation Strategy for a Single-Phase Transformerless Multilevel Inverter with Dual Bidirectional Switch", *in AEIT International Annual Conference*, pp. 1–6, 2018, doi:10.23919/AEIT.2018.8577206.

[19] A. Kuperman, "Proportional-Resonant Current Controllers Design Based on Desired Transient Performance", *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5341–5345, Oct. 2015, doi:10.1109/TPEL.2015.2408053.

[20] R. N. Beres, X. Wang, F. Blaabjerg, M. Liserre, C. L. Bak, "Optimal Design of High-Order Passive-Damped Filters for Grid-Connected Applications", *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2083–2098, March 2016, doi:10.1109/TPEL.2015.2441299.

[21] "IEEE Draft Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces", *IEEE P15471/D95*, pp. 1–269, April 2019.

[22] W. Bower, C. Whitaker, W. Erdman, M. Behnke, M. Fitzgerald, "Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems", [Online], 12 2004.

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