THE UFMG MICROGRID LABORATORY: A TESTBED FOR ADVANCED MICROGRIDS

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***Abstract* – This paper describes a test facility for the design and validation of advanced microgrids (MGs) to integrate high penetration of renewable energy and electric vehicles. The UFMG MG laboratory is a joint effort of UFMG, industry, and government. The UFMG MG laboratory is a physical simulation tool for the design, development, testing, and didactic purposes of advanced MG projects under islanded and grid-connected operating modes. Using commercial inverters, and flexible digital control cards, the testbed is modular and flexible in terms of control of inverters, communication technology, and MG architectures. The capabilities of such a testbed in the development of MG management systems are illustrated by means of experimental results considering an advanced MG performing grid-connected ancillary services, such as self-consumption and power factor regulation. The example also highlights the flexibility of the setup incorporating user-adjustable communication latency and user-defined communication failure.**

***Keywords* – Advanced Microgrid, Ancillary Services, Centralized Control, Distributed Energy Resource, Testbed.**

I. INTRODUCTION

The current concern with rising electricity costs and carbon emissions has led to a high penetration of renewable energy and electric vehicles, which challenges grid hosting capacity [1]. To mitigate typical power quality issues, ancillary services (ASs) can be performed autonomously by distributed energy resources (DERs), and/or coordinatedly by DERs and loads grouped in microgrid (MG) models. The MG model can be split into basic and advanced MGs, in which the former serves as standby generation with the capability to island from the main grid, while the latter must operate as a single-controllable entity in order to increase the grid hosting capacity [2].

Following the same concerns, the Federal University of Minas Gerais (UFMG) has approved a technical-scientific research project titled Minirrede Oasis-UFMG [3]. This institutional project aims: (*i*) the development of MG technology; (*ii*) to increase the self-generation of electricity energy into the UFMG's Pampulha Campus, Belo Horizonte, Brazil, shown in Figure 1; (*iii*) to show UFMG commitment to sustainable policies; and (*iv*) to achieve a reduction of up to 40% in the UFMG electricity bill. To succeed in these goals, it will be installed until 2024 about 500 kWp of photovoltaic (PV) power split into three plants of 128.4 kWp, 232.8 kWp, 138.8 kWp; 1 MW/3.2 MWh of energy storage based on battery banks; and 160 kW of gas microturbine (3 units). All of them will be coordinated as an advanced MG to supply 50 academic buildings, which add up to 12.2 MW of total installed power. Moreover, other actions carried on are: migration of some buildings to the free energy market; replacing the traditional light bulbs with LED lighting; limiting the non-critical air-conditioning to 8 working hours; and IoT energy management system to coordinate demand-side and load shedding under grid absence.

To support this grand enterprise, one of the Oasis-UFMG deliverables is the UFMG MG Laboratory (UFMG^{2}Lab) shown in Figure 1. It is a physical simulation tool for design, development, testing, and future didactic purposes of islanded and grid-connected advanced MG projects. It comprises commercial inverters with flexible digital control cards; hardware-in-the-loop (HIL) devices; and different wired and wireless communication technologies such as CAN, LoRaWan, and Zigbee. The UFMG^{2}Lab MG is initially deployed with a centralized controller based on hierarchical control coordinating distributed grid-feeding inverters. The grid-forming converters act in the absence of the main grid to ensure islanded operation. Due to the flexible deployment environment, decentralized or distributed MG architectures can be also implemented with different control targets.

A. Literature review

Universities and research facilities have developed their own MG testbeds [4]–[7]. For instance, the authors of [4] present an overview of several MG testing facilities around the world, such as CERTS AEP Microgrid, Mad River Microgrid, GE Microgrid, Shimizu's Microgrid, and many others. Reference [5] details the major research efforts and the development of MG control in laboratories and in pilot installations located in Europe, the United States, Japan, and Canada. The authors of [6] show the iMG lab at Aalborg University, Denmark, for MG comprehensive studies. Hierarchical control organization and results for voltage/frequency restoration and voltage unbalance compensation are also shown. In [7], it is developed a MG testbed architecture used for educational and research purposes. Other universities [8] have transformed parts of their power systems into MGs. This sustainable infrastructure

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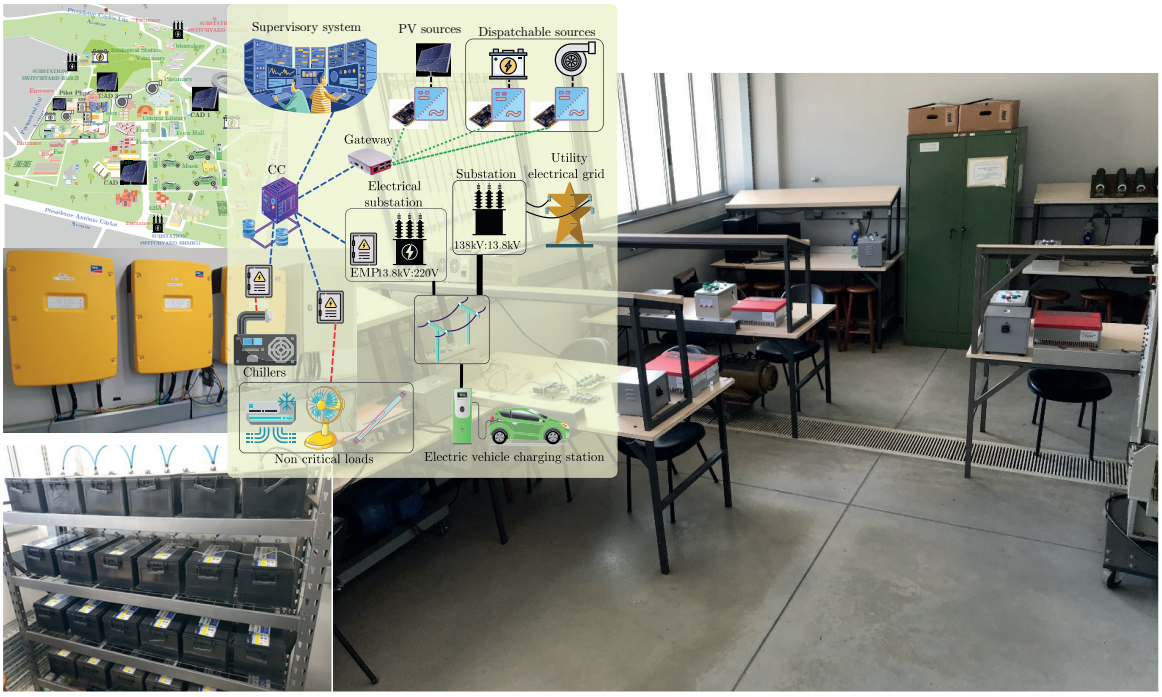

Fig. 1. Macroscopic view of the UFMG Pampulha campus in the upper left corner, highlighting the installed renewable energy resources. Immediately to the right, an artistic view of the Oasis-UFMG minigrid control. UFMG^{2}Lab facilities as a deliverable from Oasis project is shown more centered.

allows the university's researchers to use the electricity grid itself as an educational tool and research platform. A real-world MG application is described in [9], where a condominium has installed four 100 kW combined heat and power hybrid generators. It was shown a plug-in-play functionality that reduces engineering costs.

The report released by the Smart Grid Laboratories Inventory (SGLI) aggregates information on smart grid research topics, shows trends of the research community, and addresses important information about the state-of-the-art in the field [10]. Among the 86 research laboratories computed in [10], 65 are located in Europe and 21 are located outside Europe. About 84% of the laboratories are specialized in the integrated grid research category, in which 70% work on MGs. Two Brazilian laboratories are reported in the SGLI: Research Center in Smart Energy Grids (NAPREI) [11] and Smart Grids Laboratory (LabREI) [12] located at the University of São Paulo and University of Campinas, respectively. Still in this context of smart grids, other MG research laboratories can be found in the following Brazilian institutions: Federal University of Santa Catarina [13], Federal University of Santa Maria [14], Federal University of Maranhão [15], Federal University of Uberlândia [16], and others.

LabREI described in [12] allows performing critical tests that precede field applications, in addition to training specialized human resources. Reference [13] addressed the main components of an experimental MG in Brazil, also describing aspects such as MG control and implementation of high-level supervisory algorithms. The disclosure of didactic and flexible experimental testbeds in other areas of knowledge has also been a motivating factor for many papers [17]–[21]. Reference [17] builds a didactic platform that allows a gradual and assisted interaction of the student from the design of the controllers to experimental proof of the dynamic characteristics of dc motor control. The authors of [18] and [19] develop an electronic PV emulator with a graphical interface used to teach undergraduate and graduate courses. Reference [20] describes a didactic platform for thyristor-based circuits, more flexible than off-the-shelf solutions on the market. The work [21] shows a teaching platform to enhance education in power electronics, detailing some possible experiments to be carried out.

B. Challenges, contribution, and organization

In view of the aforementioned, the benefits that MG can bring to end users are numerous, although their practical integration into current distribution grids is still at an early stage [22]–[24]. The lack of expertise needed by practitioners to design a MG is one of the reasons why practical applications are still at their initial stage. Another factor is the insufficient knowledge of the main technical challenges encountered during MG integration into distribution grids [22]. Thus, this paper shows some challenges, practical aspects, and experimental results to reduce the distance between MG prototypes and practical MG, while still contributing to research and educational purposes.

This paper approaches an experimental flexible fully-dispatchable three-phase MG validation structure for educational and research purposes. The hierarchical three-layer centralized control architecture is employed, where the inverters are coordinated by means of the Power-Based Control (PBC) algorithm [25]. It is noteworthy that UFMG^{2}Lab is flexible to use other secondary layer control formulations, not being restricted to the algorithm adopted herein for proof of concept purposes. At the current stage of development, UFMG^{2}Lab integrates an advanced MG testbed tool to support the Oasis-UFMG project. At the end of this project, UFMG^{2}Lab facilities will be framed as a didactic

laboratory for training specialized human resources and for teaching undergraduate/graduate courses. This paper shares all the constructed infrastructure and design considerations with the research community, highlighting the flexibility of the experimental tool as many parts can be reconfigured.

The rest of this paper is organized as follows: Section II presents the laboratory facilities, the programmable single-phase inverter, and the advanced MG control organization. Details of the communication infrastructure are shown as well. Section III shows some ASs that the UFMG^{2}Lab advanced MG can provide according to tertiary layer interests. Section IV shows the obtained experimental results, while conclusions are stated in Section V.

II. UFMG2Lab FACILITIES AND STRUCTURES

The physical facilities of the UFMG^{2}Lab are shown in Figure 2 and in Table I. The laboratory comprises 35 m^2 with 5 workstations (WSs) organized as shown in Figure 2.a. There are two three-phase galvanically-isolated circuits available in the UFMG^{2}Lab, derived from the main switchboard. The auxiliary three-phase circuit supplies the diode rectifier-based dc power source and protection boards. The main three-phase four-wire low-voltage circuit of UFMG^{2}Lab is shown in Figure 2.b, in which loads and inverters are connected. This is a 7-node system, where the WSs are strategically located on the system nodes. The unbalanced and balanced linear loads are dispersedly connected in the UFMG^{2}Lab grid, whose values are shown in Table I. The laboratory also has a motor drive test bench, where the motor can be driven by means of a CFW08 variable frequency drive (VFD) or direct on-line (DOL) start. The VFD+motor typically behaves like a non-linear constant-current load. The exclusive MG power circuit is distributed throughout the laboratory from the main switchboard. Voltage and current measurements are performed at the MG point of common coupling (PCC), while the signal conditioning boards are arranged in the electrical panel of the central controller (CC).

The MG power nodes for connection of loads and inverters are accessed through banana terminals close to each WS, as shown in Figure 2.a. Similarly, the shielded/twisted cabling of the CAN network is distributed in cable ducts throughout the UFMG^{2}Lab. Access to the communication infrastructure is via RJ45 connectors close to the workstations. Each WS is composed of a notebook, an off-the-shelf commercial single-

TABLE I
Line and Load Parameters of the UFMG^{2}Lab

Parameter	Label	Value
RMS voltage	V_n	220 V
Line impedance 0	R_0; L_0	9.8 Ω; 53.96 μH
Line impedance 1	R_1; L_1	12.9 mΩ; 11.71 μH
Line impedance 2	R_2; L_2	7.1 mΩ; 6.41 μH
Line impedance 3	R_3; L_3	5.6 mΩ; 5.07 μH
Line impedance 4	R_4; L_4	33.1 mΩ; 29.96 μH
Line impedance 5	R_5; L_5	5.7 mΩ; 5.12 μH
Line impedance 6	R_6; L_6	5.7 mΩ; 5.12 μH
Line impedance 7	R_7; L_7	5.7 mΩ; 5.12 μH
Unbalanced load 1	$Z_{l1,abc}$	0; 10+j75.39; 10+j75.39 Ω
Balanced load 2	$Z_{l2,abc}$	96.58 Ω

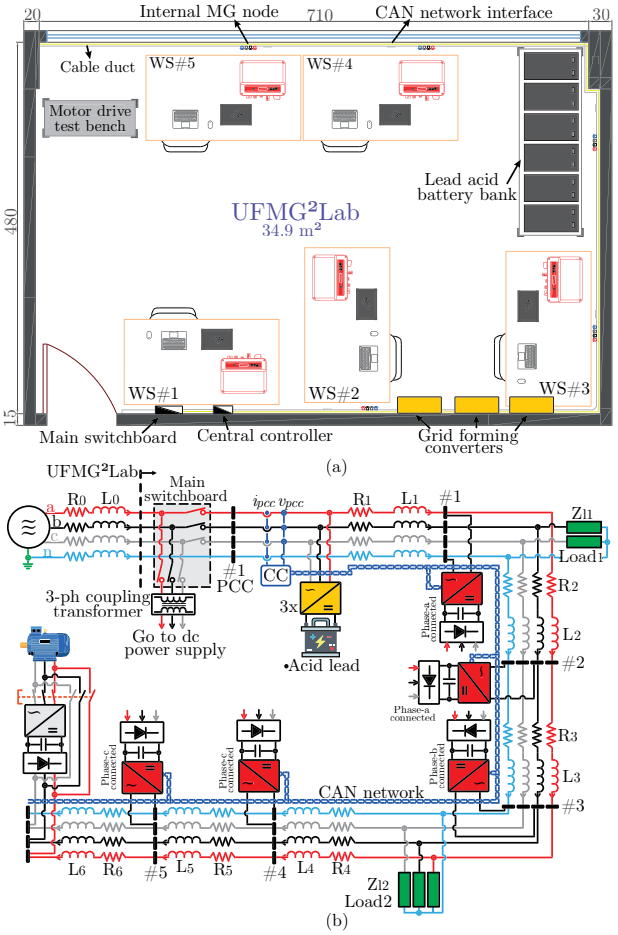

Fig. 2. (a) Floor plan of the UFMG^{2}Lab, highlighting the layout of the WSs (dimensions in cm). (b) Electrical schematic of the UFMG^{2}Lab facilities and structures.

phase PHB 1500-NS inverter equipped with communication units, the necessary apparatus for their connection to the grid (i.e., power cables, dc power source, etc.), Typhoon hardware-in-the-loop controller for real-time testing of developed algorithms, suitable debug probes and 200 MHz 4-channel oscilloscope equipped with A612 and P5200A probes. The UFMG^{2}Lab also has three off-the-shelf single-phase grid-forming Sunny Island 6.0H inverters (from SMA), supplied by 2 strings of 4 series-connected lead-acid 12MS234 Moura batteries each (48 V-440 Ah). These SMA inverters are delta-connected forming a three-phase grid in a master-slave configuration.

A. Programmable single-phase inverter

The PHB 1500-NS inverter available in UFMG^{2}Lab is shown in Figure 3.a. Figure 3.b shows the inverter printed circuit board (PCB) with the embedded power electronic components. Emphasis is given to the dc input and ac output, power circuits on the PCB periphery, and conditioning/processing circuits at the PCB central region. The three-phase diode rectifier is built-in inside the electrical box of Figure 3.c, as well as the protection circuits, on/off, and emergency buttons. The ac side of the electrical box is powered by the galvanically isolated laboratory auxiliary grid, while its dc side is connected to the PHB 1500-NS inverter.

Figure 3.d shows the hardware schematic, which consists

TABLE II
Parameters of the Single-Phase PHB 1500-NS Inverter

Parameter	Label	Value
Inverter rated power	S_n	1.5 kVA
Switching frequency	f_{sw}	15 kHz
Sampling frequency	f_s	15 kHz
LC filter inductance	L_f	1 mH
LC filter internal resistance	r_f	77.10 Ω
LC filter capacitance	C_f	3.3 μF
Grid voltage (RMS)	V_g	127 V
Grid angular frequency	ω	377 rad/s
dc-link voltage	v_{dc}	310 V
dc-link capacitance	C_{dc}	1.17 mF

of a current-controlled dc-ac full-bridge converter with a passive LC output filter to suppress the harmonic components produced by the switching. The inverter parameters are given in Table II. The primary energy source consists of a three-phase non-controlled rectifier, powered by a laboratory auxiliary grid. The PHB 1500-NS inverter is designed to operate as a standalone unit, i.e., regardless of external power supplies. As observed in Figure 3.d, the power supply of the instrumentation circuits is obtained from the input dc-side stage, using a flyback converter and voltage regulators to generate different levels of dc voltage.

The factory firmware is deleted and flexible control strategies for all desired applications are programmed in the Texas Instruments 60 MHz 32-bit TMS320F28034 fixed-point digital signal controller (DSC), as depicted in Figure 3.e. All peripheral circuits required to implement the control structure

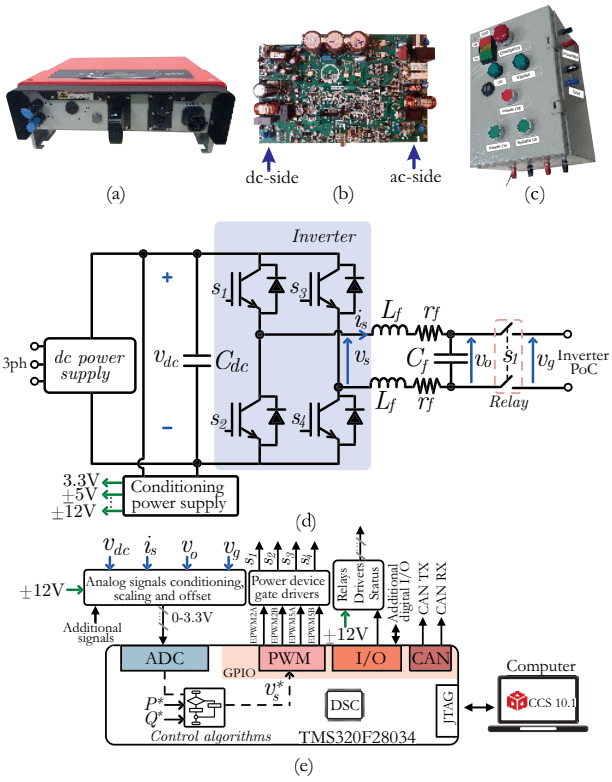

Fig. 3. (a) Front view of PHB 1500-NS inverter hardware. (b) Inverter PCB with embedded power electronic components. (d) Circuit protection box and dc power supply. (d) Inverter power circuit schematic. (e) Schematic of connection between hardware and DSC.

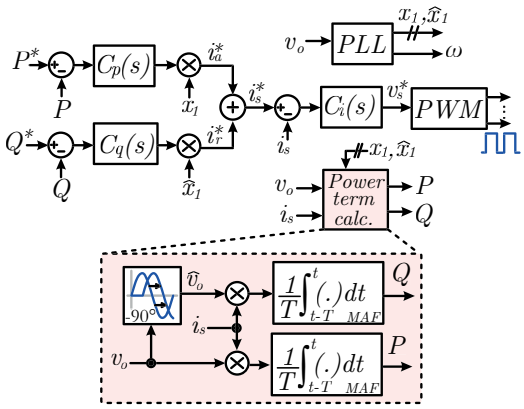

Fig. 4. Control block diagram implemented at the PHB 1500-NS inverter. Emphasis on the MAF-based power calculation algorithm.

are present in this DSC, namely: 12-bit analog-to-digital converters (ADCs), PWM units, and configurable general-purpose input/output (GPIO) pins.

Converter-controlled operation requires measurement of many electrical analog variables, such as: dc-link voltage (v_{dc}), injected current (i_s), output voltage (v_o), and point of connection (PoC) voltage (v_g). Acquiring these signals requires adequate conditioning of electronic circuits, filtering capability and scaling. Regarding this topic, two concerns must be noted: (i) the sensor signal is scaled to fully exploit the ADC voltage range (0-3.3 V), maximizing the number of effective bits of the analog signal representation in the digital domain; (ii) application of 1.65 V offset on ac-nature signals since the ADC does not accept negative voltage values.

Regarding communication with notebook, the DSC is programmed and debugged via a XDS110 JTAG controller. Code Composer Studio software from Texas Instruments is used for algorithm development, debugging, and online visualization of the desired variables from the running code in the DSC. Finally, the standard 2.0B controller area network (CAN) module is configured to communicate serially with other MG units (including other inverters and CC). The initial choice for the CAN network is based on its reliability and robustness in electrically noisy environments.

Figure 4 shows the programmed grid-feeding inverter control block diagram, which consists of two-cascaded loops: (*i*) an outer active (P) and reactive (Q) power control loop for current reference (i_s^*) generation; and (*ii*) an inner current control loop for output current (i_s) tracking. $C_p(s)$ and $C_q(s)$ are the active and reactive power controllers, respectively, while $C_i(s)$ is the inner current controller. The synthesized voltage reference v_s^* calculated by the cascade control is applied to the uniformly sampled, single-update, unipolar, and symmetrical PWM with triangular carrier, which generates the suitable gate pulses for inverter switching. The outcomes of $C_p(s)$ and $C_q(s)$ are multiplied by unit in-phase and 90°-phase-shifted sinusoidal signals, x_1 and $\hat{x}_1$, respectively. These unit signals are generated by means of a robust-distortion PLL-based algorithm proposed in [26] and are synchronized with the fundamental component of the inverter PoC voltage.

The algorithms to calculate the active and reactive power terms are based on moving-average filters (MAF) [27], as shown in Figure 4. The controller tuning procedure follows

TABLE III
Parameters of the Current/Power Controllers

Parameter	Label	Value
Inner loop: proportional gain	K_{pi}	16 Ω
Inner loop: integral gain	K_{ii}	1000 Ω/s
Inner loop: crossover freq.	f_{ci}	1000 Hz
Inner loop: phase margin	PM_i	60 deg.
Outer loop: proportional gain	K_{pp}	0.0079 V^{-1}
Outer loop: integral gain	K_{ip}	1.29 V^{-1}/s
Outer loop: crossover freq.	f_{cp}	15 Hz
Outer loop: phase margin	PM_p	75 deg.

the guidelines of [28]: (*i*) current loop gains (K_{pi} and K_{ii}) are designed for a compensated open loop with 60 deg. phase margin (PM_i) and 1 kHz crossover frequency (f_{ci}), due to output filter limitations of the commercial inverter; and (*ii*) power loop gains (K_{pp} and K_{ip}) are tuned with 75º phase margin (PM_p) and 15 Hz crossover frequency (f_{cp}) due to the dynamics of the MAF-based power calculation algorithm. More details about the inverter embedded control strategy can be found in [29]. All controllers and PLL gains are summarized in Table III.

B. Microgrid control organization

The devices in Figure 2.b are organized in a hierarchical control for a centralized advanced MG model, which must comply with (*i*) inherit an efficient power sharing among the inverters, for efficient operation; (*ii*) regulate the power exchanged with the upstream grid to be seen as a single-controllable entity; and (*iii*) have the capability of operating in both grid-connected and islanded modes to guarantee high operation reliability [30], [31]. To achieve these tasks, the MG hierarchical control architecture shown in Figure 5 is adopted to coordinate the inverters and to provide specific ASs [32].

The different control layers communicate with each other through a low-bandwidth communication infrastructure. The primary hierarchical control is responsible for the embedded operation of the inverters, through basic (i.e., current/voltage control, grid synchronization) and specific (i.e., anti-islanding, and reactive power injection) functions. These functions do not rely on communication, which means the MG stability is not impaired under faults in the communication network infrastructure.

Secondary control aims at efficiently managing the active/reactive power on MG nodes. The PBC algorithm is employed in the LAUNCHXL-F28379D CC, as a specific

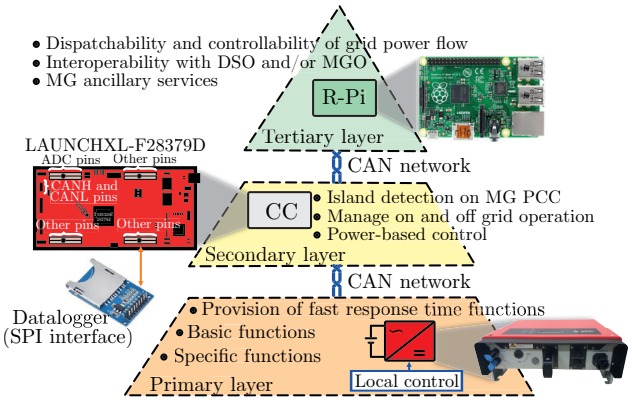

Fig. 5. Microgrid hierarchical control organization.

secondary layer tool for the UFMG^{2}Lab MG [33]. Multiple targets are fetched in this control layer: (*i*) proportional power sharing among inverters, (*ii*) power flow control at the MG PCC, and (*iii*) unwanted unbalance mitigation. Still in this layer and to mount a MG database, a microSD card-based datalogger is developed in the LAUNCHXL-F28379D CC SPI interface. The sampling period is set to acquisition every 5 sec. The tertiary layer performs the interoperability between the MG CC and the MG operator (MGO) and/or distribution system operator (DSO). This interaction allows the scheduling of AS at the MG level.

It is worth remarking that the use of communication is limited to MG support functions. Thus, if communication failures occur, the basic and specific functions of inverters, as well as all the functions that are performed autonomously, keep on running normally. Thus, the primary control layer still guarantees system operation within grid-code requirements, and the MG stability is not compromised. On the other hand, proportional power sharing, and grid power flow control might be lost in case of communication failure.

C. Communication Infrastructure

Figure 6 shows the communication infrastructure between CC and spread inverters. The controller area network (CAN) uses a serial multimaster communication protocol that efficiently supports MG control with a communication rate of 125 kbps. The CAN network uses two shielded/twisted pair wires as the physical transmission link (i.e., CANH and CANL). The network nodes communicate through the differential voltage between CANH and CANL. All devices share the same data channel, where 120 Ω terminator resistors are installed at the beginning and end of the network. Each network microcontroller is equipped with a CAN controller, while the external CAN transceiver performs the interface between the microcontroller and the physical network. LAUNCHXL-F28379D CC already has the built-in CAN transceiver.

A Raspberry Pi (R-Pi) 3, model B, is employed as a network sniffer for monitoring and supervision purposes. As the R-Pi does not have CAN bus support, its SPI pins are configured to connect with the CAN bus using MCP2515 CAN controller and transceiver [34].

Figure 7 shows the CAN 2.0B data frame, which contains 108 bits. The data frame is formed by start, identification, control, data, cyclic redundancy check (CRC), acknowledge, and end-of-frame fields. Except for data, all fields are CAN frame overhead bits. Through the mailbox concept, sent and received messages are identified by IDs. For instance, inverters are configured to receive and send data frames with ID 0 and N $\in \{1,..,5\}$, respectively. CC sends data with ID 0 and receives data with ID 0∼15, allowing to receive data frames from all inverters.

Finally, data fields hold up to 8 bytes. The data is encoded in positive-integer type, according to its 1- or 2-byte sizes. Transmitted scaled variables of magnitude less than 2^7-1 (127) and 2^{15}-1 (32,767) use 1 and 2 bytes of the data field, respectively. The encoding process requires offset and scaling to improve the transmitted effective number of bits. After receiving, the 1- or 2-byte data is decoded according to the examples shown in Figure 7.

III. ANCILLARY SERVICES PROVIDED BY ADVANCED MICROGRIDS

The advanced MG structure of the UFMG²Lab can be configured to provide different ASs according to tertiary layer commands. The coordinated PBC algorithm employed at the MG second layer for proof of concept purposes is capable of regulating the grid active/reactive power flow and sharing power proportional to the inherent capability of each inverter [33]. Due to the flexibility offered by the UFMG²Lab, other secondary layer control formulations can be easily implemented for advanced MG experimental tests.

Among the possible ASs provided by the advanced MG, self-consumption and PCC power factor correction are interests of this work, as shown in Figure 8. Actual per-phase active P_{nm} and reactive Q_{nm} power, maximum per-phase active P_{nm}^{max} and reactive Q_{nm}^{max} power capability must be exchanged between the n-th $\in \{1,..,N\}$ inverter (connected in phase m) and CC. Total per-phase active $P_{L,m}$ and reactive $Q_{L,m}$ power drained at the internal MG nodes is computed in the CC, considering an exchange of per-phase active $P_{pcc,m}$ power and reactive $Q_{pcc,m}$ power with the upstream grid. Finally, the per-phase active α_m and reactive β_m power scaling coefficients are broadcast to the inverters via the CAN network, according to the power exchanged commands with the grid ($P^*_{0,m}$ and $Q^*_{0,m}$).

Self-consumption: the power flow exchanged between the MG and the upstream grid is zero, efficiently exploiting the use of MG renewable energy sources [35]. Under such a scenario, the upstream grid only provides voltage and frequency reference to the MG. This condition is reached when tuning the per-phase references $P^*_{0,m}$ and $Q^*_{0,m}$ equal to zero at the PBC algorithm, as highlighted in position ① of Figure 8. If the power ratings of the inverters are not exceeded (i.e., -1 < α < 1 and -1 < β < 1), self-consumption is suitably achieved.

Power factor correction: consist in the utilization MG for compensation of the reactive power demand in the PCC. The

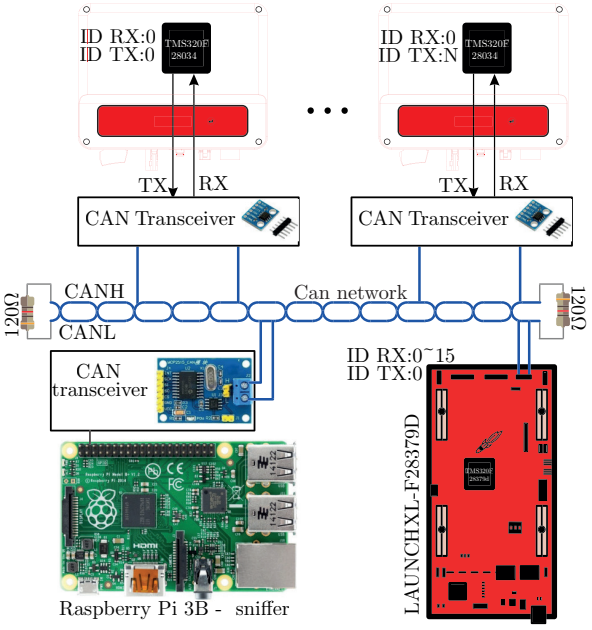

Fig. 6. Structure of CAN network installed on UFMG²Lab.

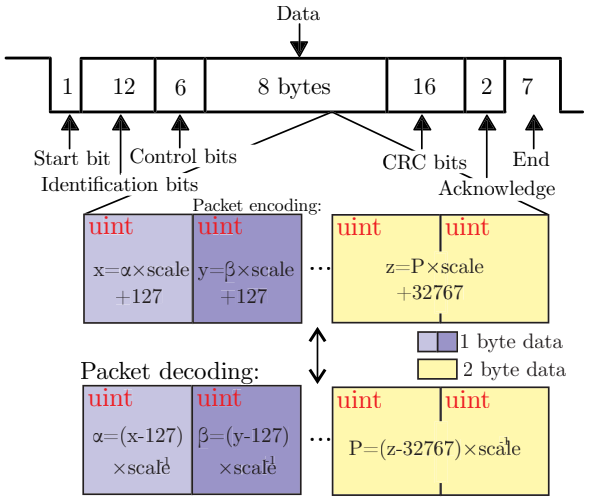

Fig. 7. CAN 2.0B data frame.

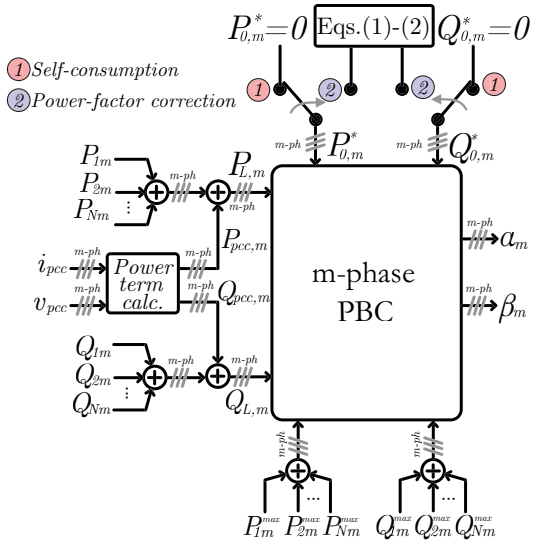

Fig. 8. Flowchart of the PBC algorithm implemented in the CC to provide different AS according to tertiary layer interests.

correction will prevent the industrial customer from paying fines. This service has the execution dynamics of 1 to 15 minutes, where the communication time is not critical. PCC power factor must be controlled above the limit established by the power distribution company (i.e., 0.92), avoiding fines paid by the MGO. Accordingly, this scenario is reached tuning the per-phase references $P^*_{0,m}$ and $Q^*_{0,m}$ by:

$$P^*_{0,m} = P_{L,m}, \tag{1}$$

$$Q^*_{0,m} = \frac{P^*_{0,m}}{PF^*}\sqrt{1-(PF^*)^2}, \tag{2}$$

where PF^* is the desired PF at the MG PCC that can be flexibly changed according to the MGO interests. The switch is selected in position ② of Figure 8 to achieve power factor correction unless the inverters power ratings are not exceeded.

IV. EXPERIMENTAL RESULTS

The experimental results of the UFMG²Lab consider the inverters located in WS#1, #2, #3 and #5 of Figure 2, grid-

connected mode, hierarchical control of Subsection II.B and communication infrastructure described in Subsection II.C. The ASs provided by the MG are described in Section III.

A. Self-consumption and controlled PCC power flow

Figure 9 shows the experimental power terms collected at the MG PCC and at the inverter's terminals for seven different events that occur in the following sequence: (*i*) at $0 \leq t <$ 505 s, the inverters operate in stand-by mode with zero power injection terms. MG control is disabled; (*ii*) at $505 \leq t <$ 1005 s, MG control is enabled with self-consumption mode; (*iii*) at $1005 \leq t <$ 1500 s, DOL induction motor start is performed with the MG in self-consumption mode; (*iv*) at $1500 \leq t <$ 2000 s, resistive load 1 is disconnected from the MG; (*v*) at $2000 \leq t <$ 2500 s, $Q^*_{0,abc}$ is changed from 0 to 300 var to import reactive power from the grid; (*vi*) at $2500 \leq t <$ 3000 s, $P^*_{0,abc}$ is changed from 0 to -300 W to export active power to the grid; and (*vii*) at $3000 \leq t <$ 3500 s, the motor is disconnected while $P^*_{0,abc}$ =-300 W and $Q^*_{0,abc}$ =300 var.

Figures 9.a and 9.b show the per-phase active and reactive power terms exchanged between the MG and the upstream

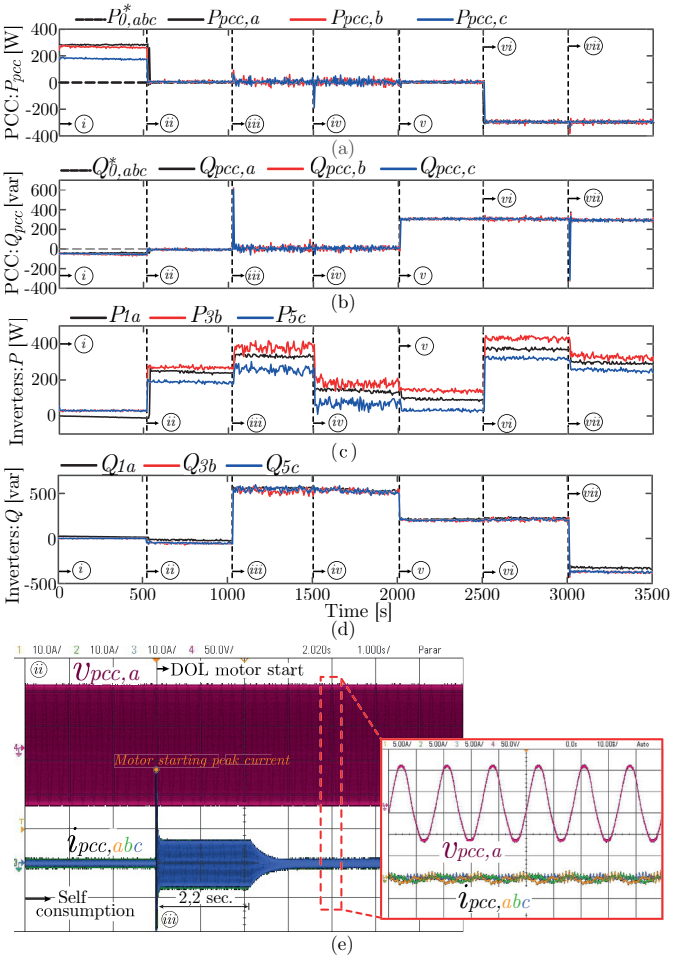

Fig. 9. Per-phase (a) active and (b) reactive power flow at the MG PCC; (c) Active and (d) reactive power processed by inverters 1, 3 and 5 (WS#1, #3 and #5); (e) a-phase voltage and three-phase currents before and after DOL motor start (per-phase currents [10 and 5 A/div]; a-phase PCC voltage [50 V/div]; and time [1000 and 10 ms/div]). Zoomed view highlighting the self-consumption achievement after motor start.

grid. Figures 9.c and 9.d show the active and reactive power processed by inverters 1, 3, and 5 (WS#1, #3, and #5), respectively. From (*i*), the inverters are in standby mode (null reactive and active power processing), while the upstream grid supplies per-phase unbalanced power terms ($P_{pcc,abc} = [285, 263, 173]$ W and $Q_{pcc,abc} = [-50, -49, -50]$ var). From (*ii*), the centralized-based MG control algorithm is enabled in self-consumption mode. The inverters operate according to the fully explored PBC algorithm, steering null grid power. From (*iii*), a 1.5 hp motor is DOL connected. Inductive reactive power (positive sign) is demanded to magnetize the motor, which is initially supplied by the upstream grid as noted in Figure 9.b until the secondary MG layer control operates. Then, the inverters are driven to inject capacitive reactive power (positive sign) from -50 to 534 var, to regulate the null PCC power terms even under load variations. Figure 9.e shows that the MG control requires 2.2 s to reach the self-consumption state again after DOL motor start. From (*iv*) and (*vii*), it is noticed that the MG control behaves properly under load shedding, being also able to dispatch active (*v*) and reactive (*vi*) power at the MG PCC.

B. Power factor correction

Figure 10 shows the experimentally measured PCC power factor, power terms collected at the MG PCC and at the inverter's terminals for six events: (*i*) at $0 \leq t <$ 500 s, the inverters operate in standby mode, MG control is disabled and only resistive load is grid connected. Figure 10.a shows the PCC three-phase power factor close to unity, with an active and reactive power flow of $[336, 326, 246]$ W and $[19, -3, -5]$ var, respectively (vide Figure 10.b and 10.c; (*ii*) at $500 \leq t <$ 1000 s, VFD-driven motor starts under 50% axle load, while the MG centralized control with power factor correction is set to 0.9 (inductive). As noted, the PCC power factor drops to 0.9, as the reactive power increases from $[19, -3, -5]$ to $[137, 137, 137]$ var. (*iii*) at $1000 \leq t <$ 1520 s, PF^* is configured to 0.92 inductive. As expected in Figure 10.d and10.e, the inverters inject practically null active power and start to absorb reactive power (negative sign) to achieve PF^* = 0.92 (inductive); (*iv*) at $1520 \leq t <$ 2010 s, the unbalanced inductive load 2 is grid-connected, which alleviates the reactive power absorption of the phase-b and -c connected inverters; (*v*) at $2010 \leq t <$ 2510 s, PF^* is varied from 0.92 (inductive) to 0.925 (capacitive). Reactive power processed by inverters increases from $[-12, -12, -120]$ (absorbed) to $[500, 465, 346]$ var (injected). Despite the current harmonics generated by the grid-side VFD rectifier, the a-phase PCC current is slightly displaced compared to the a-phase voltage in Figure 10.f. Furthermore, no unbalance currents are noted due to suitable MG control; and (*vi*) at $2510 \leq t <$ 3000 s, PF^* = 1 is set, while the MG control properly reaches this reference as shown in Figure 10.a. Figure 10.g shows that the a-phase current is in phase with the a-phase voltage.

C. Advanced MG tests to assess the effect of communication infrastructure non-idealities

Figure 11 shows the experimental power terms collected at the MG PCC and at the inverters 1 and 2 (WS#1, and #2) terminals for twelve different events (i.e., (*i*)–(*xii*)). Both inverters are connected to the same phase, sharing power to

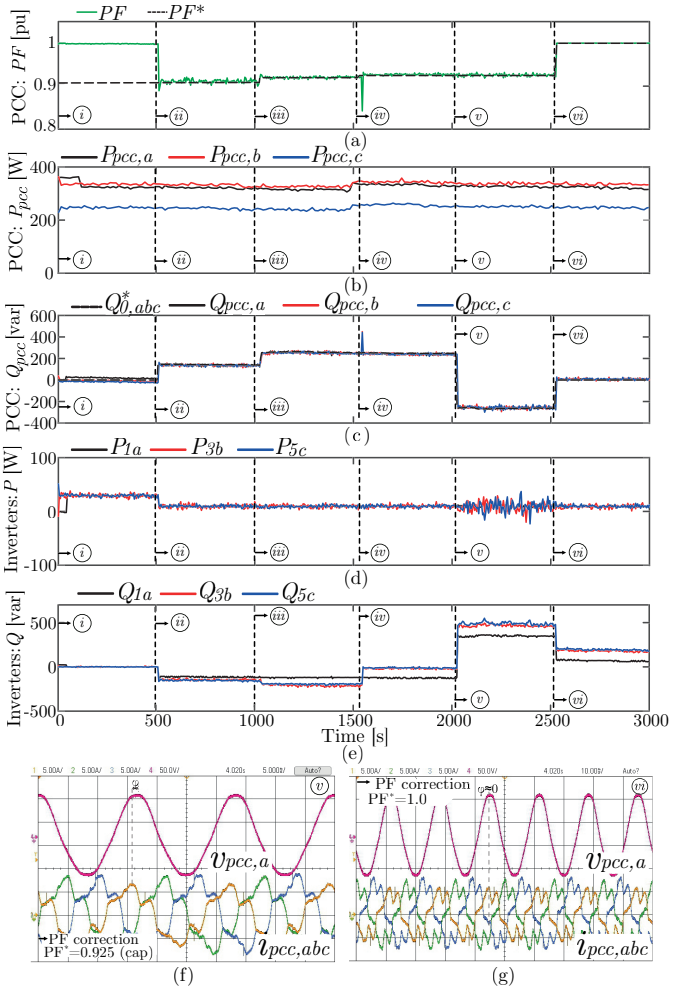

Fig. 10. (a) Reference and measured three-phase PCC PF, disregarding the influence of current harmonics; Per-phase (b) active and (c) reactive power flow at the MG PCC; (d) Active and (e) reactive power processed by inverters 1, 3 and 5 (WS#1, #3 and #5); a-phase voltage and three-phase currents for PCC PF regulation at (f) 0.925 (cap.) and (g) 1.0 (per-phase currents [5 A/div]; a-phase PCC voltage [50 V/div]; and time [500 and 100 ms/div]).

regulate $P^*_{0,a}$ and $Q^*_{0,a}$ at the MG PCC. Figure 11.a shows the secondary-layer references (i.e., $P^*_{0,a}$ and $Q^*_{0,a}$) and measured active and reactive power terms at the MG PCC terminals. Figures 11.b and 11.c show the active and reactive power terms injected by inverters 1 and 2 during the aforementioned events, respectively. D_1 and D_2 are values of delays in receiving packages from the CC to inverters 1 and 2, respectively.

During the event (*i*), the MG control is disabled and the inverters operate in stand-by mode with null power injection. The MG control is enabled with self-consumption mode in (*ii*), in which inverters share power to regulate null PCC active and reactive power terms. During events (*iii*) and (*iv*), $Q^*_{0,a}$ is changed from 0 to 500 var to absorb reactive power from the grid (i.e., inductive reactive power, vide the zoomed view of Figure 11.d), and subsequently from 500 to 0 var to once again achieve self-consumption. In such scenarios, D_1 and D_2 are set to 0 ms. The zoomed view of Figure 11.a shows that the reactive power quickly tracks the reference when the delays in receiving packets are negligible compared to the PBC control cycle (i.e., 5 s) – there is a very small inherent latency of the

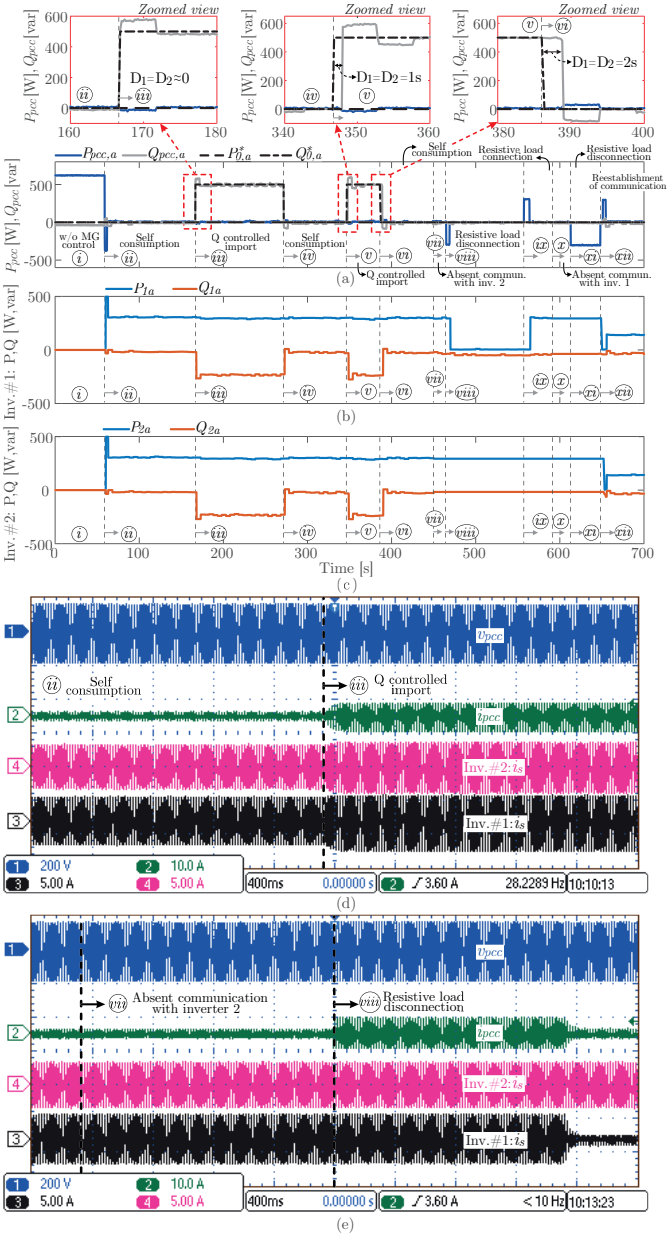

Fig. 11. Communication link effects: (a) Active and reactive power flow at the MG PCC; Active and reactive power terms processed by inverters (b) 1 and (c) 2; (d) PCC voltage and inverter 1 and 2 currents before and after $Q^*_{0,a}$ change from 0 to 500 var to absorb reactive power from the grid (i.e., inductive reactive power); (e) PCC voltage and PCC, inverter 1 and 2 currents before and after communication failure between CC and inverter 1; (currents [10 and 5 A/div]; PCC voltage [200 V/div]; and time [400 ms/div]).

CAN communication link.

During events (*v*) and (*vi*), $Q^*_{0,a}$ is changed from 0 to 500 var and from 500 to 0 var, respectively. Both delays are flexibly set to 1 s and 2 s at (*v*) and (*vi*), respectively. The zoomed view of Figure 11.a shows a delayed transport on $Q_{pcc,a}$ related to the reference tracking $Q^*_{0,a}$ when there is a delay in receiving packets. Due to delayed action, the inverters take longer to respond to the new coefficients – vide also Figures 11.b and 11.c. Such delays do not affect the overall ability of the coordinated control to steer inverters for PCC power flow regulation.

At the event (*vii*), communication failure between CC and inverter 2 is emulated. Since communication is absent, inverter 2 continues to operate normally with the last received coefficient – vide Figure 11.e. By still having inverter 1 participating in the coordinated power sharing, the CC adjusts the scaling coefficients transmitted to inverter 1 to maintain power controllability at the MG PCC. Inverter 1 reduces and increases power injection when the resistive load is disconnected and then connected at events (*viii*) and (*ix*), respectively, while inverter 2 maintains the same power injected before the loss of communication. During the event (*x*), communication between CC and all inverters is lost, which is evidenced by the absence of self-consumption at the MG PCC during the resistive load disconnection in (*xi*). Despite the absence of PCC dispatchability, a stable operation is achieved even under such faulty conditions since the embedded control algorithms are responsible for maintaining the safe and reliable operation of the inverters regardless of the secondary layer availability. Finally, communication is reestablished between CC and both inverters at the event (*xii*). Power sharing and PCC self-consumption are once again achieved, reinforcing the UFMG^{2}Lab operational ability to develop advanced MG experimental tests.

V. CONCLUSIONS

This paper introduced the UFMG^{2}Lab facilities for educational and research purposes, highlighting the experimental testbed for validation of ac advanced microgrids. The combination of hardware, communication infrastructure, and properly sized three-layered hierarchical control is used as a flexible experimental platform for microgrid-related studies. The experimental results showed the microgrid control capable of reaching the self-consumption condition at 60 Hz regardless of rotary and linear load variations. The controlled active and reactive power dispatchability at the microgrid point of common coupling was also verified, as well as the accurate regulation of the steady-state power factor without any knowledge of the system topology and parameters. The effect of communication infrastructure non-idealities was also assessed, highlighting the flexibility presented by the UFMG^{2}Lab in performing advanced MG tests. Finally, UFMG^{2}Lab microgrid proved to be a suitable tool for research developments, flexible experimental tests, and didactic purposes.

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