FEEDBACK LINEARIZATION CONTROL FOR A CLASS OF TRANSFORMERLESS COMMON-GROUND VSI

Gabriel de O. Assunção[1], Ivo Barbi[2], Daniel J. Pagano[2]
[1]Toronto Metropolitan University (TMU), Toronto – ON, Canada
[2]Federal University of Santa Catarina (UFSC), Florianópolis – SC, Brazil
e-mail: gabriel.assuncao@torontomu.ca, ivobarbi@gmail.com, daniel.pagano@ufsc.br

***Abstract* – As is well known in practice, conventional transformerless inverters may suffer the risk of high-frequency leakage currents between the photovoltaic (PV) array or battery energy storage systems (BESS) and the ground due to the stray capacitances. This operational condition can generate several electrical problems. Recently, we proposed in [1] a new method for designing transformerless topologies of single-phase voltage source inverters (VSI) with common ground derived from four classical DC-DC converters. As a sequence of that previous work, a novel control technique based on a feedback linearization approach is proposed to control that class of transformerless VSI with common ground in this paper. Unlike the classical local linearization techniques commonly used in the technical literature, this approach allows to obtain large-signal linear equations, by means of the feedback linearization of the non-linear terms. Real-time simulation results using Hardware-in-the-Loop allow validation of the proposed discrete control technique applied to this class of VSI topologies.**

***Keywords* – Feedback Linearization Control, Inverter Topologies, Leakage Current, Transformerless Inverter.**

I. INTRODUCTION

Voltage source inverters (VSI) without galvanic isolation in the connection of energy storage and photovoltaic systems to the electrical grid can be used to reduce costs and to increase the efficiency of this class of systems [1]. However, conventional transformerless inverters are not suitable due to the generation of floating voltages which can induce the circulation of high-frequency leakage currents through the parasitic capacitors since the frame of PV modules or battery arrays are required for safety reasons to be grounded [2], [3]. Topologies with galvanic isolation avoid the existence of this leakage current, however, they entail higher costs and loss of efficiency of the converter, approximately 2% [3]. On the other hand, transformerless converters have a cost reduction of about 25% [3].

The common mode current problem, as it is also known, has generally been addressed in photovoltaic systems, although it can also be found in BESS [2]. Parasitic or stray capacitances

Manuscript received 09/05/2023; first revision 10/30/2023; accepted for publication 12/28/2023, by recommendation of Associate Editor Heverton Pereira. http://dx.doi.org/10.18618/REP.2023.4.0026

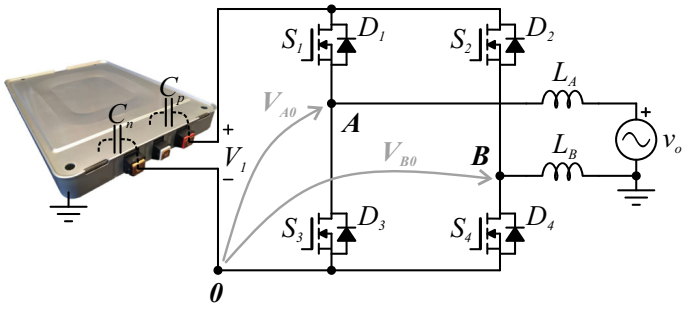

Fig. 1. Full-bridge VSI used to connect a DC power source (Lithium-ion battery pack) to an AC electrical grid.

appear between the terminals and the grounded frame in Lithium-ion battery packs as shown in Figure 1. In this circuit, the voltage between the DC link and the AC link depends on the voltages V_{A0} and V_{B0} across the power semiconductors, C_p and C_n stand for the parasitic capacitances connected to the positive and negative terminals, as also shown in Figure 1. Therefore, the DC link voltage V_1 is floating with respect to the ground point. The grounding of the modules is done through their metallic structure. This structure and other factors, such as battery or PV cell fabrication methods, cell surface area, distance between cells, weather conditions, among others, affect the value of stray capacitance.

Typically, parasitic capacitances range from $70 - 100nF/kW$ in standard PV modules [2]. These capacitances are charged and discharged at the frequency of the common mode voltage. In this way, high leakage currents may arise varying from some nano-amperes to mili-amperes or even amperes depending on the parasitic capacitance value usually related to (i) the rated power of the system, (ii) the modulation strategy, (iii) the applied voltage values, and (iv) the switching frequency.

Leakage currents are a concern of inverter manufacturers and can be extremely harmful, causing considerable performance losses in a distributed generation system using BESS or PV modules. A leakage current through stray capacitances and device grounding can generate electrical problems such as (i) risk of electric shock, (ii) emergence of electromagnetic interference (EMI), (iii) increased total harmonic distortion (THD), (iv) reduced quality of generated power and power losses and (v) possible tripping of the earth fault protection devices [2], [3], [4], [5], [6]. The leakage currents effect is analyzed in detail in [2], [3] showing how the power semiconductor switching strategy affects this floating voltage.

Recently, we proposed a novel methodology for deriving transformerless VSI topologies with common ground from

four classical DC-DC converters, see [1]. This method provides the possibility of deriving a family of inverter topologies that allow to mitigate leakage current through the common ground. However, this class of VSI presents a non-linear dynamic behavior with strong interaction of resonant frequencies due to the inductances and capacitances of the circuit. In this context, proportional-integral (PI) current controllers do not guarantee consistent and stable current tracking to connect the VSI to the grid. For the sake of the limited number of pages, these results are not presented here. On the other hand, this problem is solved in this work by the proposed controller based on a feedback linearization approach.

As is well known, VSI mathematical models represented by nonlinear differential equations are time-varying dynamical systems and, therefore, do not present equilibrium points. Hence, small-signal models of DC-AC voltage source inverters (VSI) cannot be derived directly from the average systems equations in the same way that in DC-DC converters. Furthermore, it is not mathematically appropriate to apply classical linearization techniques around an equilibrium point for this class of time-varying systems. The classical linearization method when applied to these inverters at different points of the sinusoidal signal, considered as operating or equilibrium points of the system, can lead to mathematically inaccurate models and, therefore, it is not appropriate to apply this local linearization technique when the systems are time-varying.

An alternative procedure could be to linearize the system over a given sinusoidal trajectory considered as a solution of the system equations. Other approach leads to modeling the system using time-varying phasors [7]. Both procedures, despite being feasible in theory, are difficult to implement in practice given the complexity of the nonlinear equations of the studied system. On the other hand, *dq* transformations can solve this problem for three-phase inverters, allowing to analyze them as two coupled DC-DC converters, one for the *d*-axis and the other for the *q*-axis. The application of the *dq* transform to single-phase VSI needs an artificial orthogonal component of the grid voltage. This approach introduces delays and degrades the performance of the dynamic response [8]. In general, *dq* frame control of single-phase inverters is more complicated compared with three-phase systems and therefore will not be used here.

The alternative proposed in this work is to linearize the nonlinear equations of the system through a feedback control action. This technique called feedback linearization control (FLC) differs from the classical linearization technique around an equilibrium point as it allows the system to be linearized in the equations themselves, canceling, exactly or partially, the nonlinear terms present in the model equations. The main idea of this technique is to algebraically transform the dynamics of the nonlinear system partially or completely, so that linear control methods can be applied.

It is noteworthy that this concept is different from linearization around an equilibrium point leading to linear models of small signals, since linearization by feedback is obtained by exact transformations of the states and not by linear approximations of the dynamics of the system. For more theoretical details about this technique see [9], [10]. Although this technique is well known, it has recently gained a new impetus and has been successfully applied to different electronic power converters [11], [12], [13], [14], [15].

TABLE I
GATE SIGNAL VSI TOPOLOGIES

Gate signal	buck-boost	SEPIC	Zeta	boost-buck
V_{g_1}	S_1, S_4	S_2	S_2	S_2, S_4
V_{g_2}	S_2, S_3	S_1	S_1	S_1, S_3

In this paper, a method for controlling a common ground transformerless VSI family used to connect a DC power supply to an AC power grid is proposed. The main contribution of this work is the development of a novel control technique based on an input-output feedback linearization approach that can be applied to all converters derived in [1], overcoming the limitations of conventional control techniques.

The remainder of this paper is organized as follows. Section II presents the mathematical modeling of the converter family studied in this work. The proposed feedback linearization control is addressed in Section III. Section IV presents the linear control design after applying the FLC strategy. Section V shows the experimental validation through hardware-in-the-loop (HIL) real-time experiments using the Typhoon-402 system. Finally, Section VI presents the main conclusions.

II. MODELING VSI TOPOLOGIES

The common ground VSI topologies are shown in Figure 2. This family of VSI was obtained from (a) the non-isolated buck-boost with positive output, (b) SEPIC, (c) zeta, and (d) boost-buck bidirectional converters, see [1]. The topologies shown in Figures 2.b and 2.c were originally published in [16].

As shown in [1], the static gain of the four converters is as given in (1). Assuming that the desired output voltage is a sine waveform as in (2), to achieve it, without a voltage control loop, a static linearizing function is employed for all VSI topologies of Figure 2, resulting in a time-varying duty cycle given by (3).

$$\frac{v_o(t)}{V_1} = \frac{2d(t)-1}{d(t)} \tag{1}$$

$$v_o(t) = V_{opk}\sin\omega t \tag{2}$$

$$d(t) = \frac{1}{2-\alpha\sin\omega t} \tag{3}$$

where ω is the angular frequency, in radians per second, of the AC output voltage v_o and $\alpha = V_{opk}/V_1$ is the ratio between the peak output voltage V_{opk} and the DC voltage source V_1.

This open-loop modulator signal is used in the inverters startup procedure (see [1]). The bipolar PWM modulation strategy is shown in Figure 3. As the converters necessarily operate in continuous conduction mode, for each of them there are two topological states in a switching period. The gate signals are indicated in Table I, where V_{g_1} defines the duty cycle d while V_{g_2} stands for the complementary duty cycle $(1-d)$. Moreover, v_o stands for the output voltage, i_{L_1}, i_{L_2} are the currents through L_1, L_2 inductances, respectively, C_1 is the

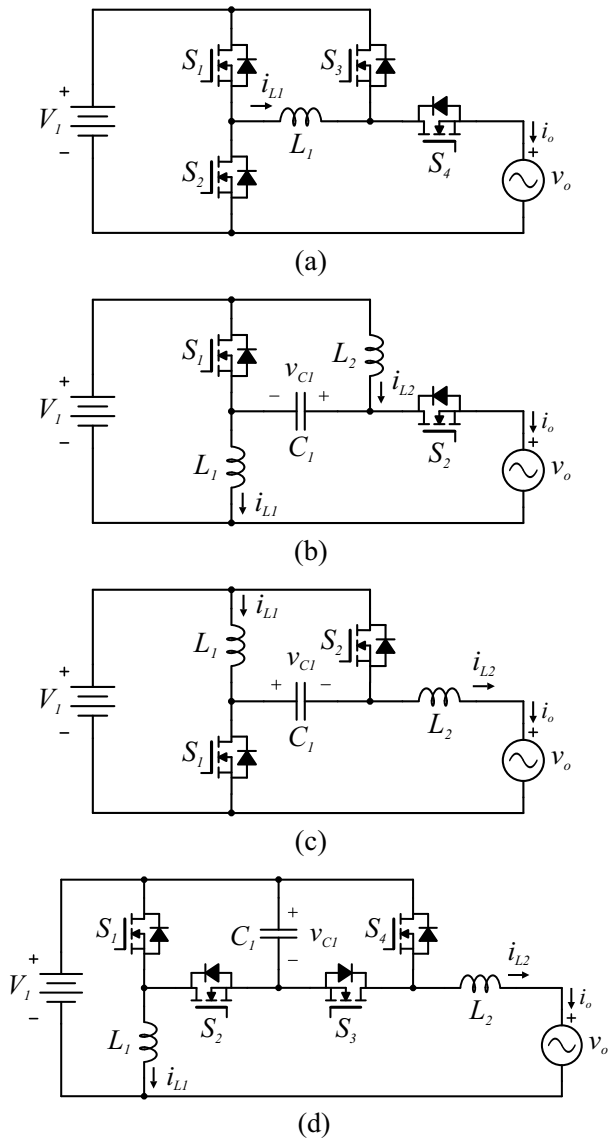

Fig. 2. Transformerless common-ground VSI connected to the grid: (a) bidirectional buck-boost; (b) bidirectional SEPIC; (c) bidirectional Zeta; (d) bidirectional boost-buck.

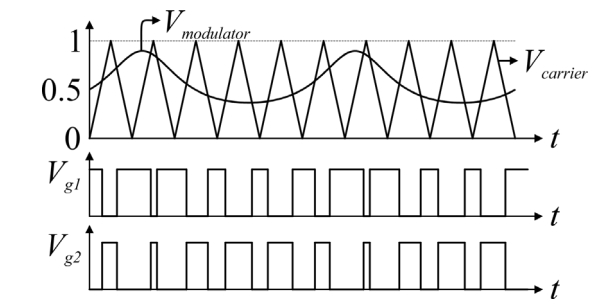

Fig. 3. Bipolar PWM modulator signals applied to generate the power semiconductor gate signals for the family inverters.

circuit capacitance and v_{c_1} is the capacitance voltage. Since input and output filters practically do not affect the behavior of the system, as long as the cutoff frequency of these filters is high with respect to the cutoff frequency of the control, they are suppressed to simplify the circuit and thus the model of each VSI. The average models developed for each topology studied in this work are presented below.

A. Buck-Boost Based Inverter

The buck-boost inverter is shown in Figure 2.a. The averaged model of this system is given by

$$L_1 \frac{di_{L_1}}{dt} = -V_1 + d\,(2V_1 - v_o)\,. \tag{4}$$

B. SEPIC Inverter

The SEPIC inverter circuit is shown in Figure 2.b. The average model equations are given by

$$\begin{aligned} L_1 \frac{di_{L_1}}{dt} &= V_1 - d\,(V_1 + v_{c_1} - v_o) \\ L_2 \frac{di_{L_2}}{dt} &= -v_{c_1} + d\,(V_1 + v_{c_1} - v_o) \\ C_1 \frac{dv_{c_1}}{dt} &= i_{L_2} + d\,(i_{L_1} - i_{L_2})\,. \end{aligned} \tag{5}$$

C. ZETA Inverter

The ZETA inverter is shown in Figure 2.c and the average model equations are given by

$$\begin{aligned} L_1 \frac{di_{L_1}}{dt} &= V_1 - d\,(V_1 + v_{c_1}) \\ L_2 \frac{di_{L_2}}{dt} &= -v_o - v_{c_1} + d\,(V_1 + v_{c_1}) \\ C_1 \frac{dv_{c_1}}{dt} &= i_{L_2} + d\,(i_{L_1} - i_{L_2})\,. \end{aligned} \tag{6}$$

D. Boost-Buck Inverter

Figure 2.d shows the boost-buck inverter circuit and the averaged model is given by

$$\begin{aligned} L_1 \frac{di_{L_1}}{dt} &= V_1 - d\,v_{c_1} \\ L_2 \frac{di_{L_2}}{dt} &= V_1 - v_o - v_{c_1} + d\,v_{c_1} \\ C_1 \frac{dv_{c_1}}{dt} &= i_{L_2} + d\,(i_{L_1} - i_{L_2})\,. \end{aligned} \tag{7}$$

III. FEEDBACK LINEARIZATION CONTROL

The FLC technique is associated with the design of a control law that allows to cancel totally or partially the nonlinearities of the model equations. Let us consider a generic nonlinear system given by (8)

$$\begin{aligned} \dot{x}(t) &= f(x) + g(x)\,d(t) \\ y(t) &= x(t) \end{aligned} \tag{8}$$

where $d(t)$ is the control variable, $x(t)$ stand for the state variables and $y(t)$ is the system output signal, the FLC law given in (9)

$$d(t) = \frac{u(t) - f(x)}{g(x)} \tag{9}$$

where $g(x) \neq 0$ must be fulfilled, is applied to obtain

$$\dot{x}(t) = u(t) \tag{10}$$

that represents the linearized system with $u(t)$ being the new control variable that can be now designed by using classic control techniques. In what follows, we apply the FLC technique to the inverter topologies.

A. FLC for Buck-Boost Based Inverter

From (4), compared to (8), $f(x)$ and $g(x)$ are found and it is deduced that

$$d(t) = \frac{L_1\,u(t) + V_1}{2V_1 - v_o}. \tag{11}$$

Therefore, by substituting (11) in (4), the linearized system is expressed as

$$\frac{di_{L_1}}{dt} = u(t). \tag{12}$$

Note for this inverter that the output current will be indirectly controlled through the control of i_{L_1} since

$$\begin{array}{ll} i_o = & d(t)\,i_{L_1} \\ i_o = & I_{opk}\sin(\omega t + \phi). \end{array} \tag{13}$$

Thus, to obtain a sinusoidal output current, (3) is utilized in (13), which results in the current reference as follows

$$i_{L_{1ref}} = \frac{i_o}{d(t)} = I_{opk}\sin(\omega t + \phi)(2 - \alpha\sin\omega t) \tag{14}$$

where ϕ is the phase angle of the current, considering that the main voltage is the zero phase angle reference. Figure 4.a shows the control block diagram for the buck-boost inverter taking into account the generation of the control reference $i_{L_{1ref}}$ from the desired output current i_{oref} according to (14). The control loop can be seen in Figure 4.b, being system (4) fully linearized as shown in (12).

B. FLC for SEPIC Inverter

The controlled variable is defined as the current i_{L_2} and the duty cycle derived from (5) is given by

$$d(t) = \frac{L_2\,u(t) + v_{c_1}}{V_1 + v_{c_1} - v_o}. \tag{15}$$

Since the high-frequency voltage oscillation in the capacitor C_1 is attenuated by the dynamics of the control loop, it can be neglected. In this sense, the quasi-instantaneous average value of the voltage across the capacitor C_1 is equal to the input voltage V_1 and (15) can be rewritten as

$$d(t) = \frac{L_2\,u(t) + V_1}{2V_1 - v_o}. \tag{16}$$

From (5) and (16) we obtain the linearized system given by

$$\begin{array}{rcl} \frac{di_{L_1}}{dt} & = & -\frac{L_2}{L_1}u(t) \\ \frac{di_{L_2}}{dt} & = & u(t) \\ \frac{dv_{c_1}}{dt} & = & \frac{1}{C_1}\left[i_{L_2} + \frac{L_2\,u(t)+V_1}{2V_1 - v_o}\,(i_{L_1} - i_{L_2})\right]. \end{array} \tag{17}$$

Note that in this case the system (5) was partially linearized with only the first two equations being linearized and the third equation remaining non-linear.

C. FLC for ZETA Inverter

The controlled output current is also i_{L_2}, therefore,

$$d(t) = \frac{L_2\,u(t) + v_o + v_{c_1}}{V_1 + v_{c_1}}. \tag{18}$$

Since the quasi-instantaneous average value of v_{c_1} in this inverter is the difference between the input and output voltages, (18) is rewritten as

$$d(t) = \frac{L_2\,u(t) + V_1}{2V_1 - v_o} \tag{19}$$

and the resulting linearized system is given by (17).

D. FLC for Boost-Buck Inverter

Similarly to the previous topologies, the output current to be controlled is i_{L_2}. The FLC is given by

$$d(t) = \frac{L_2\,u(t) - V_1 + v_o + v_{c_1}}{v_{c_1}}. \tag{20}$$

Now, as the quasi-instantaneous average voltage across capacitor C_1 of this topology is given by $v_{C_1} = 2V_1 - v_o$, (20) can be rewritten as

$$d(t) = \frac{L_2\,u(t) + V_1}{2V_1 - v_o}. \tag{21}$$

By substituting (21) in (7), and considering the quasi-instantaneous average value of the voltage in capacitor C_1, we find a partially linearized system similar to that described for the SEPIC and zeta inverters given by (17).

E. Internal Dynamics

By applying the FLC to the four topology models, the buck-boost inverter is fully linearized by means of this technique, while the other three inverters are only partially linearized. However, it is obtained for the four topologies the same equation for the duty cycle $d(t)$ given in (11), (16), (19), (21). The control block diagram of FLC and the linear control for i_{L_2} current used in SEPIC, Zeta and boost-buck inverters is shown in Figure 5.a. It is worth mentioning that compared to a traditional linear control structure, only the FLC block has been added since the PI and PR controllers are the conventional ones.

Notice that the same partially linearized system (PLS) after the feedback linearization, given in (17), is found for these three topologies. Figure 5.b shows a schematic block diagram of the system after applying the FLC and also the linear control that will be explained in section IV.Furthermore, it is observed that the input and output voltages, V_1 and v_o, represent feedforward control actions in the FLC block, contributing to compensating disturbances for these variables through the control action.

To connect the inverters with the electrical grid only the i_{L_2} current is controlled. Therefore, to validate the internal dynamics stability of the system, it is necessary to ensure that the other variables i_{L_1} and v_{c_1} are bounded signals and the resulting system remains stable. From the first and second equations of (17), it can be deduced that

$$\frac{di_{L_1}}{di_{L_2}} = -\frac{L_2}{L_1} \tag{22}$$

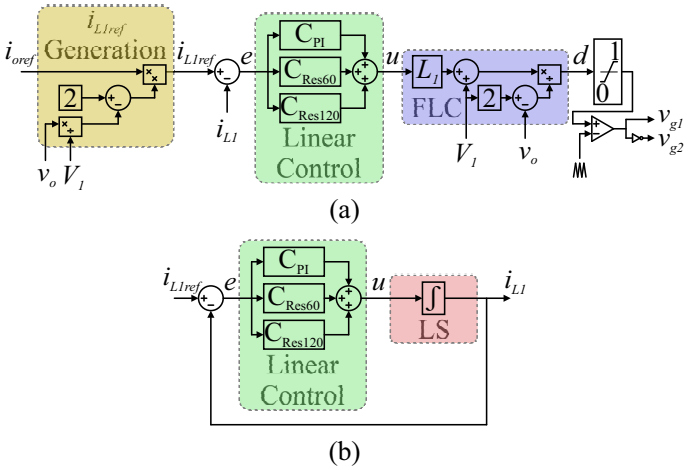

Fig. 4. (a) Control block diagram for i_o current used in the buck-boost inverter showing the block generation of $i_{L_{1ref}}$ reference current and (b) the control loop for the buck-boost inverter showing the linear control and the linearized system (LS) after FLC.

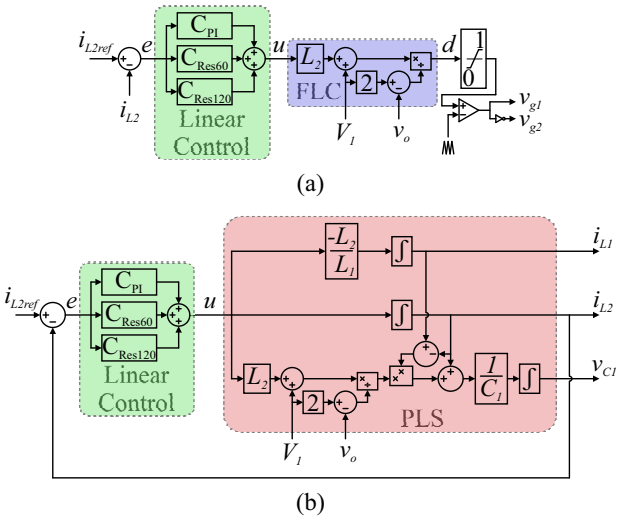

Fig. 5. (a) Control block diagram of FLC and linear control for i_{L_2} and (b) the partially linearized system (PLS) given in (17) after apply the FLC to SEPIC, ZETA and boost-buck inverters.

and by integrating (22) it is obtained

$$i_{L_1} = -\frac{L_2}{L_1} i_{L_2}. \tag{23}$$

Now, by substituting (23) in the third equation of (17)

$$C_1 \frac{dv_{c1}}{dt} = i_{L_2} \left[1 - \frac{L_2 u(t) + V_1}{2V_1 - v_o} \left(\frac{L_1 + L_2}{L_1} \right) \right]. \tag{24}$$

Assuming that system (17) is in steady-state thus $e(t) \to 0$. Therefore $u(t)$ is bounded and its mean value is approximately zero, so that $\langle u(t) \rangle \approx 0$ in (24) yields

$$C_1 \frac{dv_{c_1}}{dt} \approx i_{L_2} \left[1 - \frac{V_1}{2V_1 - v_o} \left(\frac{L_1 + L_2}{L_1} \right) \right]. \tag{25}$$

Since i_{L_2} is a controlled variable, then the internal stability condition is given by

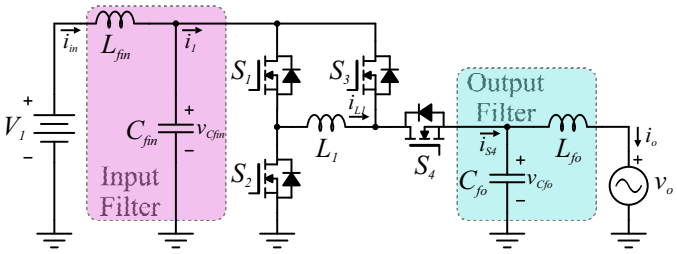

Fig. 6. Buck-boost-based inverter with input and output filters.

$$1 - \frac{v_o}{V_1} < \frac{L_2}{L_1}. \tag{26}$$

Moreover, as the mean value of $v_o = V_{opk} \sin(\omega_0 t) \approx 0$, the internal stability condition can expressed by $L_1 < L_2$.

IV. LINEAR CONTROL DESIGN

In this section, a linear control for the current i_{L_2} is designed from the linearized model obtained after applying the FLC method to the inverter nonlinear models. It is assumed that the inverters operating in bidirectional mode are connected to the power grid and the $i_{L_2 ref}$ current reference is generated by a PLL-based grid synchronization system as will be presented in subsection C.Control objectives are defined as: (i) tracking of the current sinusoidal reference ($i_{L_2 ref}$) generated by the PLL-based grid synchronization with null error; (ii) rejection to disturbances of power step changes and phase inversion; (iii) transient regime with minimum overshoot and maximum setting-time of 0.25 seconds (equivalent to 15 grid cycles).

A. Transformerless Common-Ground VSI Design Specifications

The design inverter specifications are given in Tables II and III. Moreover, *LC* and *CL* filters were considered to eliminate high-frequency ripple at the input and output of inverters as shown in Table III. As an example, the buck-boost inverter that needs both filters is shown in Figure 6.

B. PI and Resonant Controllers

The PI controller and the resonant controller, tuned to 60 Hz, are designed to guarantee null steady-state error to track a sinusoidal current reference ($i_{L_2 ref}$) and optimize the transient time response. The discrete controllers were designed using the root-locus method in the z-plane. It is observed that the resulting plant, after applying the FLC, to be controlled

TABLE II
DESIGN VSI SPECIFICATIONS

Symbol	Description	Value
V_1	DC input voltage	400 V
$V_{o_{rms}}$	Electrical grid voltage (RMS)	220 V
P_o	Output power	1 kW
f_s	Switching frequency	50 kHz
f_o	Output voltage frequency	60 Hz
f_{fin}	Input filter cut frequency	5 kHz
Δi_{L_1}	Current ripple in L_1	20%
Δi_{L_2}	Current ripple in L_2	5%
Δi_o	Output current ripple	5%
Δi_{C_1}	Voltage ripple across C_1	5%
$\Delta i_{C_{fin}}$	Voltage ripple across C_{fin}	1%

TABLE III
VSI PASSIVE COMPONENTS

	buck-boost	SEPIC	ZETA	boost-buck
L_1	1.43mH	10.24mH	10.24mH	10.24mH
L_2	-	15.93mH	15.93mH	15.93mH
C_1	-	$4.11\mu F$	$2.31\mu F$	$1.48\mu F$
L_{fin}	$24.63\mu H$	$49.25\mu H$	$49.25\mu H$	-
C_{fin}	$41.14\mu F$	$20.57\mu F$	$20.57\mu F$	-
L_{fo}	$560.19\mu H$	$560.19\mu H$	-	-
C_{fo}	$1.14\mu F$	$1.14\mu F$	-	-

in the four cases can be reduced to an integrator that is described through discretization by mapping poles and zeros and assuming the sampling frequency equal to the switching frequency $f_s = \frac{1}{T_s} = 50$ kHz, as

$$G(z) = \frac{k\,T_s}{z-1} = \frac{I_{L_2}(z)}{U(z)} \tag{27}$$

where T_s stands for the sampling time, k is the plant gain and $U(z) = U_{PI}(z) + U_{Res}(z)$. The transfer function of the PI controller is described in (28), where k_p and k_i are the proportional and integrative gains, respectively, and with $E(z) = I_{L_2 ref}(z) - I_{L_2}(z)$.

$$C_{PI}(z) = k_p + k_i \frac{T_s}{z-1} = \frac{U_{PI}(z)}{E(z)} \tag{28}$$

The discrete resonant controller, $U_{Res}(z) = C_{Res}\,E(z)$, as developed in [17], is given by

$$C_{Res} = k_r\,T_s \frac{\cos(N\omega_0 T_s) - z^{-1}\cos((N-1)\omega_0 T_s)}{1 - 2z^{-1}\cos(\omega_0 T_s) + z^{-2}} \tag{29}$$

where k_r is the resonant controller gain, $\omega_0 = 2\pi f_o$ [rad/sec] stands for the resonant frequency, with $f_o = 60$Hz, and N is the delay compensation, chosen as the number of sampling periods to be compensated. In addition, after performing the fast Fourier transform (FFT) on the output current of these inverters, it was detected the presence of harmonics at 120Hz and 180Hz, with the largest component at 120Hz. Thus, another resonant controller tuned to 120Hz was later added to reduce the effects of this harmonic on the time response. As SEPIC, Zeta and boost-buck inverters present some dynamic interactions not captured by the plant model, some parameters must be considered to assist in the design of the linear controllers. In particular, two resonant frequencies due to capacitance C_1 associated with one of the inductors (L_1, L_2) in each topological state can be observed in the circuit. The resonance frequencies for each inverter topology as shown in Table IV are calculated by $f_{LC} = \frac{1}{2\pi\sqrt{L_{1,2}C_1}}$ using the parameter values given in Table III. Notice that low resonance frequencies were found. Hence, the controllers will not be able to have a fast response as the crossover frequency must be very

TABLE IV
RESONANCE FREQUENCIES

Resonant Frequency	SEPIC	Zeta	boost-buck
$f_{L_1C_1}$	775Hz	1.03kHz	1.29kHz
$f_{L_2C_1}$	622Hz	829Hz	1.04kHz

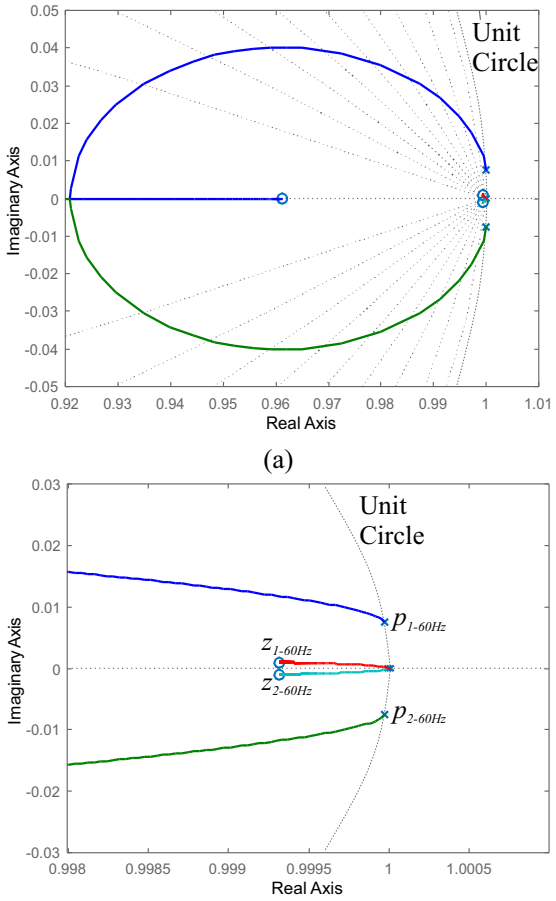

Fig. 7. Root locus of system (30) for parameter k, with resonant controller at 60Hz in z-plane: (a) root-locus diagram showing the location of poles and zeros and (b) poles and zeros near $z = 1$.

close to 60Hz. Disregarding the resonant controller at 120Hz, the open-loop transfer function (F_{ol}) is given by

$$F_{ol}(z) = G(z)\,(C_{PI}(z) + C_{Res}(z)) \tag{30}$$

and by substituting (27), (28) and (29) in the former equation

$$F_{ol}(z) = \frac{k\,T_s\,\left(a\,z^3 + b\,z^2 + c\,z + d\right)}{(z-1)^2\,[z^2 - 2\cos(\omega_0 T_s)\,z + 1]} \tag{31}$$

$a = [k_p + k_r T_s \cos(\omega_0 T_s)]$,
$b = -(2k_p + k_r T_s)\cos(\omega_0 T_s) - k_p - k_r T_s$,
$c = 2\,(k_p - k_i T_s)\cos(\omega_0 T_s) + k_p + k_r T_s$,
$d = -k_p T_s + k_i T_s^2$.
The closed-loop system characteristic equation is given by

$$1 + F_{ol}(z) = 1 + G(z)\,(C_{PI}(z) + C_{Res}(z)) = 0. \tag{32}$$

The PI controller and the resonant controllers are designed by applying the root-locus method to eq. (32). First notice that $F_{ol(z)}$ has two poles in $z = 1$, coming from the plant model after applying feedback linearization and the integrator of the PI controller, and two complex conjugated poles from the resonant controller. It also has three zeros, two resonant controller zeros, and a PI controller zero whose placement depends on the design of controller parameters.

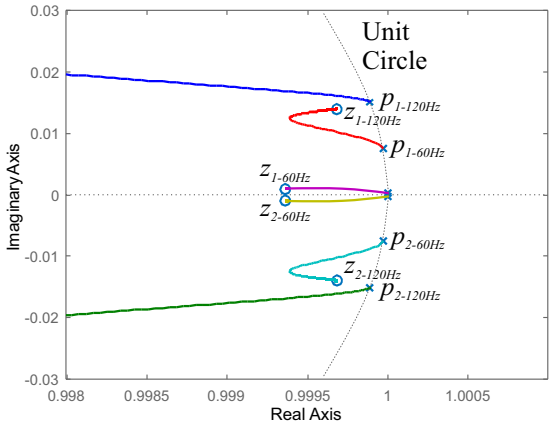

Fig. 8. Root-locus diagram of system (30) with addition of a resonant controller at 120 Hz, showing poles and zeros near $z = 1$.

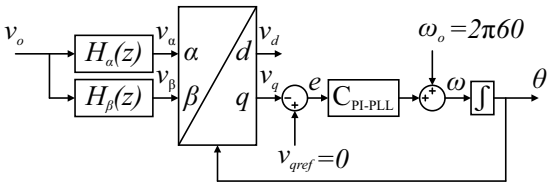

Fig. 9. General structure of the single-phase PLL with generation of the orthogonal system used in this work.

Thus, considering that the desired frequency for the resonant controller is 60Hz and that the switching frequency is 50kHz, so the sampling period is $T_s = 20\mu s$, the gains $k_p = 40$, $k_i = 2 \cdot 10^3$ and $k_{r60} = 80 \cdot 10^3$ are designed using the root-locus method. The root-locus diagram is shown in Figure 7.a for the designed control gains. Note that because the sampling frequency (50kHz) is much higher than the resonant frequency of 60Hz, the poles are located very close to the real axis near $z = 1$. Notice also that two poles are located at $z = 1$ and two poles are complex at $1 \pm j0.0075$. One zero is on the real axis at 0.9619 and two complex zeros at $0.9993 \pm j0.001$ are near to the two poles at $z = 1$ (see Figure 7.b. Since the complex poles of the resonant controller are on the unit circle, a small gain allows to place the closed-loop poles inside the unit circle. The resonant controller at 120Hz introduces in the previously carried out design another pair of new complex conjugated poles at $0.9999 \pm j0.0151$, and two zeros whose allocation must be designed. The gain of this controller was chosen as a function of the amplitude relationship between the 120Hz harmonic and the fundamental component, being of $k_{r120} = 20 \cdot 10^3$. Zeros of the open-loop transfer function are placed at 0.9531, $0.9997 \pm j0.014$ and $0.9994 \pm j0.001$, as shown in Figure 8.

C. PLL-Based Grid Synchronization

In order to connect the inverter to the electrical grid, it must be synchronized through a phase-locked loop (PLL) designed by adopting the technique presented in [18]. Generally, single-phase PLL techniques have the same general structure, as shown in Figure 9, their main differences are usually in the generation of the orthogonal system. In this work a *trapezoidal method* was chosen. Transfer functions H_α, H_β are given by

$$H_\alpha(z) = \frac{v_\alpha}{v_o}(z) = \frac{b_0\left(1 - z^{-2}\right)}{1 - a_1 z^{-1} - a_2 z^{-2}} \tag{33}$$

$$H_\beta(z) = \frac{v_\beta}{v_o}(z) = \frac{b_1\left(1 + 2z^{-1} + z^{-2}\right)}{1 - a_1 z^{-1} - a_2 z^{-2}} \tag{34}$$

where $b_0 = \dfrac{2k\omega_0 T_s}{2k\omega_0 T_s + \omega_0^2 T_s^2 + 4}$, $b_1 = \dfrac{k\omega_0^2 T_s^2}{2k\omega_0 T_s + \omega_0^2 T_s^2 + 4}$,

$$a_1 = \frac{2(4 - \omega_0^2 T_s^2)}{2k\omega_0 T_s + \omega_0^2 T_s^2 + 4}, \; a_2 = \frac{2k\omega_0 T_s - \omega_0^2 T_s^2 - 4}{2k\omega_0 T_s + \omega_0^2 T_s^2 + 4}.$$

From the generated orthogonal system, the $\alpha\beta$ to dq transform is performed as

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{35}$$

and for the *PI* controller (C_{PI-PLL} in Figure 9), $k_p = 0.72011$ and $k_i = 111.9771$ were used. The angle θ resulting from this loop is synchronized with the grid voltage and, from it, it is possible to set the reference for the output current as $i_{L_2 ref} = \hat{I}_{L2ref} \cos(\theta + \phi)$ where $\hat{I}_{L_2 ref}$ and ϕ are the desired amplitude and phase, respectively.

V. EXPERIMENTAL HIL RESULTS

This section discusses the performance of the proposed FLC scheme applied to the transformerless common-ground VSI topologies considering (i) a power step change, going from rated power to 50% of it and returning to rated power; (ii) a phase inversion test to demonstrate the ability of this inverter to operate with positive and negative power flow. The proposed control scheme is validated using the Typhoon-402 hardware-in-the-loop platform, as shown in Figure 10. The transformerless common-ground VSI topologies are modeled in the Typhoon-402 real-time simulation system. The proposed control algorithm is implemented on a digital signal processor (DSP) F28069M board interfaced with the Typhoon through an interface board. Real-time simulations and harmonic analysis of each VSI topology are performed

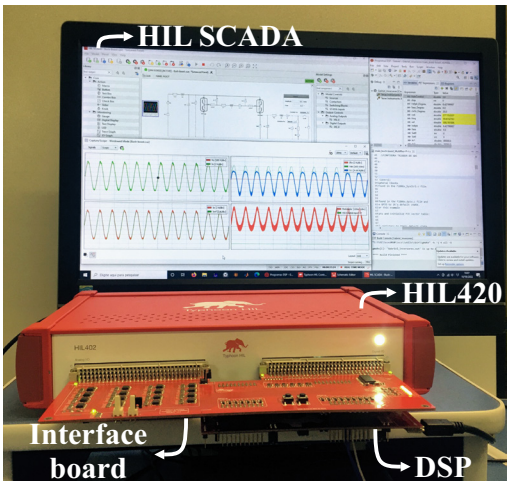

Fig. 10. Typhoon-HIL 402 real-time simulation system with DSP below the interface board.

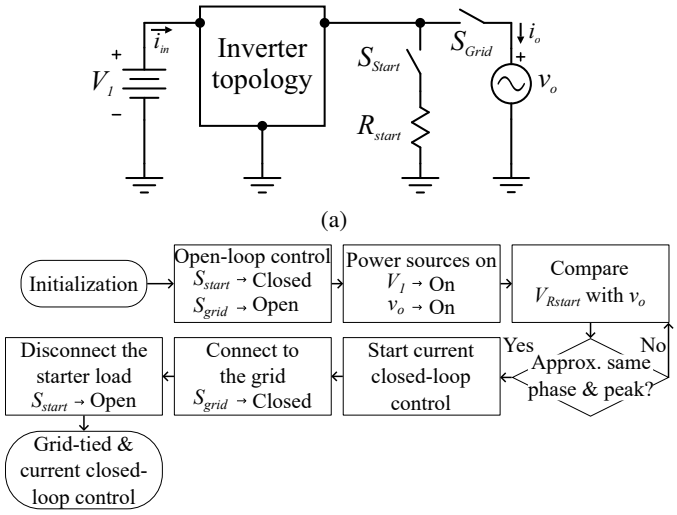

Fig. 11. Startup in real-time simulation experiments (a) VSI circuit and (b) flowchart.

with internal resistances of inductors and transistors as $R_L = R_{DSon} = 0.1\Omega$.

A. VSI Startup in Real-Time Simulation Experiments

In real-time simulation experiments to carry out the startup of each inverter, the following steps were followed: (1) switch S_{Start} is closed, S_{Grid} is open, the PLL finds the synchronization angle θ by sensing the voltage of the electrical grid; the DSP operates in open-loop with the angle θ provided by the PLL; (2) after the inverter starts operating, the DSP starts operating in current closed-loop; (3) S_{Grid} switch is closed; (4) switch S_{Start} is opened. Figure 11 shows the startup setup used in the experiments and a flowchart detailing the steps.

B. Real-Time HIL Simulation

The input and output voltages and currents are shown in Figure 12. Voltages across the input and output filter capacitors are also shown. Through the harmonic analysis of the output currents, THDs of 7.69%, 4.99%, 4.84% and 4.95% were measured for the buck-boost, SEPIC, zeta and boost-buck inverters, respectively. In Figure 13, a power step change is performed, going from the rated power to 50% of it and returning to the rated power. Note that approximately four cycles are required for buck-boost inverter stabilization, ten cycles for SEPIC, Zeta, and boost-buck.

The phase inversion response is depicted in Figure 14 showing the capacity of this inverter to operate with positive and negative power flows although a few more grid cycles are required to stabilize the system. A high overshoot signal is also noticed, but this can be minimized by optimizing the controller or making it slower.

VI. CONCLUSIONS

This paper addresses the control design for a novel class of transformerless common-ground VSI developed in [1]. This class of bidirectional VSI has a structure with few components, a simple modulation strategy, the capacity to suppress leakage current, double grounding, and satisfactory

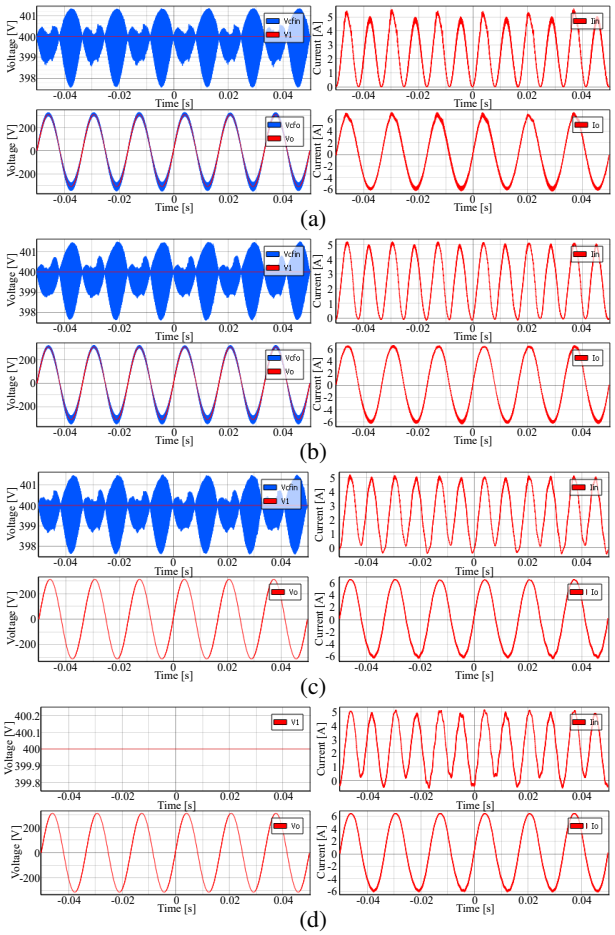

Fig. 12. Input and output voltages (V_1, v_o in red color) and current time-responses (I_{in}, i_o in red color) for VSI (a) buck-boost; (b) SEPIC; (c) Zeta; (d) boost-buck. Output and input filter capacitor voltages, (v_{cfin}, v_{cfo} in blue color) and $V_1 = 400V$ are also shown.

performance. Thus, they are suitable to interconnect a DC voltage source with the grid, being able to operate with both positive and negative power flow, in addition to processing reactive power like a conventional VSI full bridge inverter.

The feedback linearization approach presented a superior solution to classical modeling and control techniques since the non-linearities of the system were linearized in the equations themselves and not around an equilibrium point. The FLC technique allowed partially or fully linearizing the four VSI nonlinear models. The steps to achieve it were presented, implemented, and the control objectives were accomplished.

The proposed control architecture was validated using the real-time HIL Typhoon platform proving to be suitable for controlling this class of VSI connecting small power photovoltaic generators and battery energy storage systems to the electrical grid. The FLC technique allowed the design of the controller without studying the small-signal converter transfer functions, typically considered for this task. This fact represents a formidable advantage, as it greatly simplifies the analysis, disregarding the problem that the small-signal transfer function of the classical converter changes according to the steady-state operating point.

The strategy of linearizing the equations facilitates the design of the controller since instead of a long not-precise and complex transfer function, the resulting controlled plant in

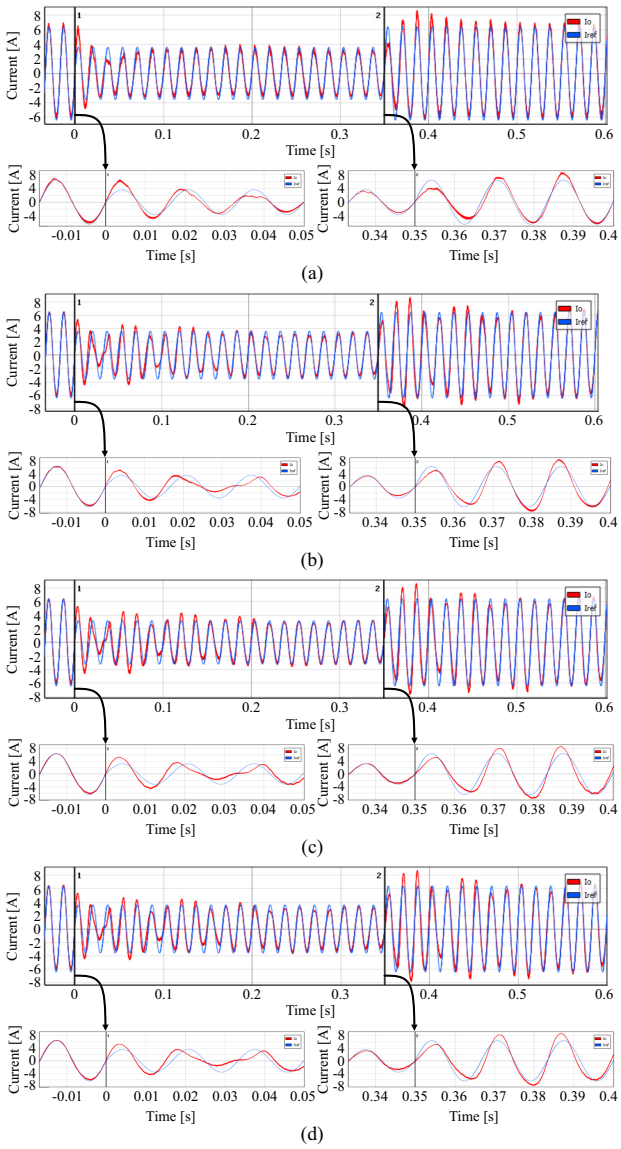

Fig. 13. Output (i_o red color) and reference current (i_{ref} blue color) time-responses for a power step-change of 50% applied to VSI (a) buck-boost; (b) SEPIC; (c) Zeta; (d) boost-buck.

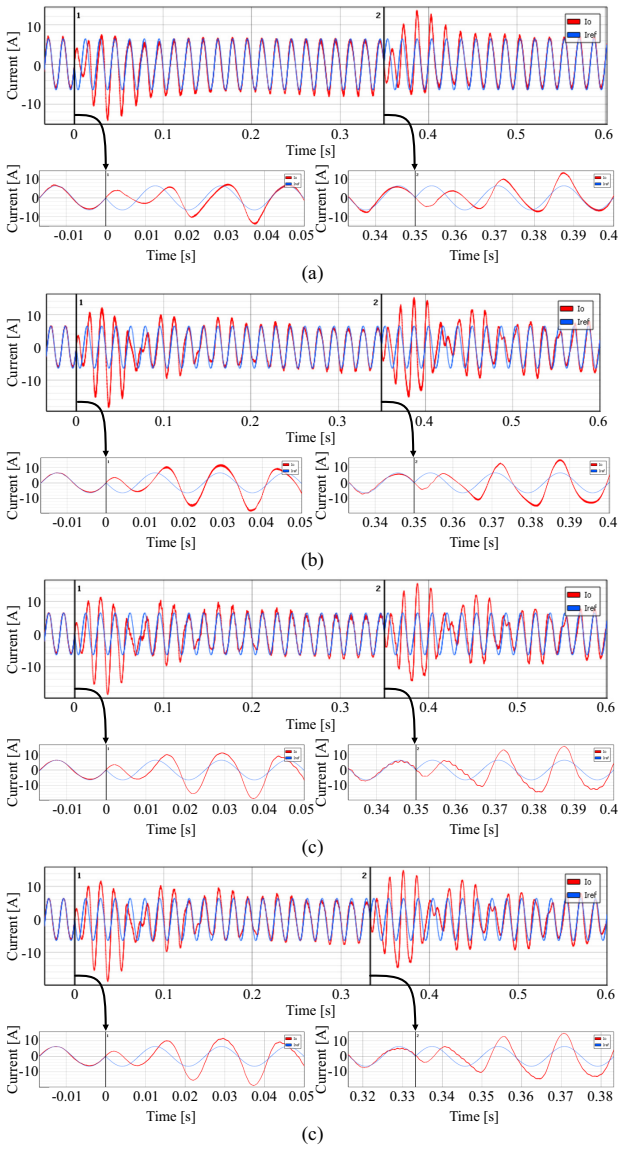

Fig. 14. Output (i_o red color) and reference current (i_{ref} blue color) time-responses for phase inverter power flow applied to VSI (a) buck-boost; (b) SEPIC; (c) Zeta; (d) boost-buck

this case is a pure integrator. As for implementation, assuming that both approaches lead to a controller equation that requires approximately the same capacity from the microcontroller, the only difference would be changing the new control variable u(t) to the previous control variable d(t), which can be solved in just 1 line of code.

ACKNOWLEDGEMENTS

This work was supported by CAPES Brazilian Federal Agency for Support and Evaluation of Graduate Education within the Ministry of Education of Brazil under Grant 88882.344611/2019-01, and by the Federal University of Santa Catarina. D. J. Pagano acknowledges CNPq/Brazil for funding his work under Grant Grant PQ-307529/2021-5.

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BIOGRAPHIES

Gabriel de O. Assunção, was born in Londrina, Brazil, in 1988. He received his B.S. degree in electronic engineering and M.S. degree in electrical engineering from the Federal University of Technology – Paraná (UTFPR), Ponta Grossa, Brazil, in 2013 and 2016, respectively, and the Ph.D. degree in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianopolis, Brazil, in 2022.

He is currently working as a Postdoctoral Fellow Researcher at the Toronto Metropolitan University (TMU). His research interests include power electronics, rectifiers, inverters, power converters for storage systems, and renewable energy sources.

Ivo Barbi, was born in Gaspar, Santa Catarina, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr. Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society, the Brazilian Power Electronics Conference, in 1990, and the Brazilian Institute of Power Electronics and Renewable Energy, in 2016. He is currently a Researcher with the Solar Energy Research Center, Florianópolis, SC, Brazil, and a Professor Emeritus of electrical engineering with UFSC.

Dr. Barbi was a recipient of the 2020 IEEE William E. Newell Power Electronics Award. He was an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS for several years.

Daniel J. Pagano, was born in La Plata, Argentina, in 1961. He received the B.Sc. degree in telecommunications engineering from the National University of La Plata, Argentina, in 1985, the M.Sc. degree in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1989, and the Ph.D. degree in robotics, automation, and electronics from the University of Seville, Seville, Spain, in 1999.

He is currently a Full Professor with the Department of Automation and Systems, Federal University of Santa Catarina, Florianópolis, Brazil. From September 2006 to October 2007, he was a Visiting Professor with the Department of Engineering Mathematics, University of Bristol, Bristol, U.K. From January 2016 to December 2016, he was a Visiting Professor with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW, Australia. His main research interests include nonlinear dynamical systems, bifurcation analysis, nonlinear control, and power electronics.