GENERATION OF DC-DC CONVERTERS WITH WIDE CONVERSION RANGE BASED ON THE MULTISTATE SWITCHING CELL

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Abstract – **This paper presents the conception of six nonisolated dc-dc converters with wide conversion range based on the multistate switching cell. In order to achieve wide conversion range, the multiphase transformer that is part of the multistate switching cell aggregates coupled secondary windings with controlled rectifiers, which are then connected in series. Then, it is possible to minimize the voltage stresses across the switches, allowing the use of MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) with reduced on-resistance $R_{DS(on)}$, thus implying the significant improvement of the converter efficiency. The operation principle, qualitative analysis, quantitative analysis, and design procedure are properly presented. A 3 kW experimental prototype is also developed, with input and output voltages equal to 84 V and 400 V, respectively. Some important results are then discussed in order to validate the theoretical assumptions.**

Keywords – **Nonisolated Dc-dc Converter, Multi-state Switching Cell (MSSC), Wide Conversion Range Converters.**

I. INTRODUCTION

Modern applications such as photovoltaic systems, fuel cell systems, and small wind energy conversion systems typically involve low voltages (12 Vdc – 48 Vdc) due to presence of a dc-link composed by filter capacitors or back-up batteries. They are supposed to be stepped up to levels ranging from 200 Vdc to 800 Vdc to supply single-phase or three-phase voltage source inverters typically found in off-grid and on-grid systems, submerged water pumps, motor drives, among others [1]. For this purpose, the classical nonisolated dc-dc converters are not a good choice, considering that the operation at very low or high duty cycles is not possible in practice due to the inherent non idealities. An alternative lies in the use of cascaded converters, although in some cases this solution implies reduced efficiency due to the existence of several power processing stages in series [2]. In order to overcome this disadvantage, some solutions using step-up converters capable of operating with high voltage gain have been proposed and analyzed in the literature [3]-[9]. However, many topologies are only suitable to process powers lower than 1 kW, while there is the need to develop dc-dc converters with wide conversion range for higher power levels.

Aiming to achieve good current sharing through the semiconductor devices in dc-dc converters, the MSSC shown in Figure 1.a has been widely studied and employed in the conception of novel topologies [10]-[13]. On the other hand, the resulting dc-dc converters have the same static gain of the classical ones. Considering the automatic current sharing feature and the presence of a transformer in the MSSC, it is possible to couple secondary windings with rectifier stages as shown in Figure 1.b. Within this context, this paper proposes generalized dc-dc converters with wide conversion range, where were obtained by adding secondary windings to the autotransformer of the multistate switching cell (MSSC) proposed in [10], [11] and after were connected their respective rectifier stages in series. Novel converters with wide conversion range based on the MSSC, named of WCR-MSSC converters were derived, as presented in [14]. It is worth to mention that they can be employed in the development of UPS (Uninterruptible Power Systems) with common-neutral-point using few batteries in series. For this condition, a bi-directional dc-dc converter operating as step-up and as step-down is necessary. Therefore, the study converter can operate in either buck or boost mode when the battery is charged or discharged, respectively.
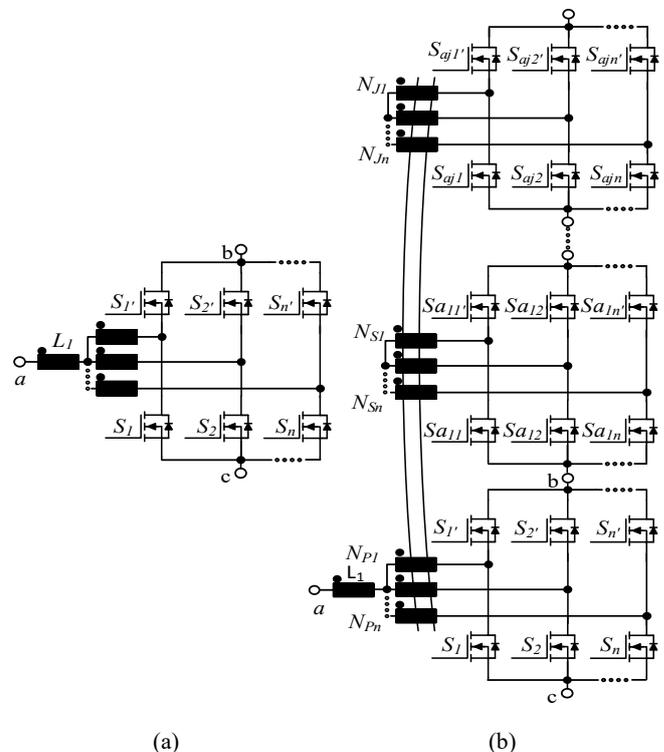
(a)   (b)
Fig. 1. (a) MSSC; (b) WCR-MSSC.

II. GENERATION OF NEW CONVERTER TOPOLOGIES

The cell shown in Figure 1.b can be applied to the six classical dc-dc converters, so that new topologies with wide conversion range can be obtained, as illustrated in Figure 2. They are so-called WCR-MSSC dc-dc buck, boost, buck-boost, Ćuk, SEPIC (single-ended primary inductance converter), and zeta converters.

The main features addressed to the aforementioned converters are [11]:

- Reduced current stress through the switches if compared to the classical topologies with high voltage gain [15],
- since the current is equally shared among the existing multiple phases;
- Possibility of adding several secondary windings to extend the conversion range;
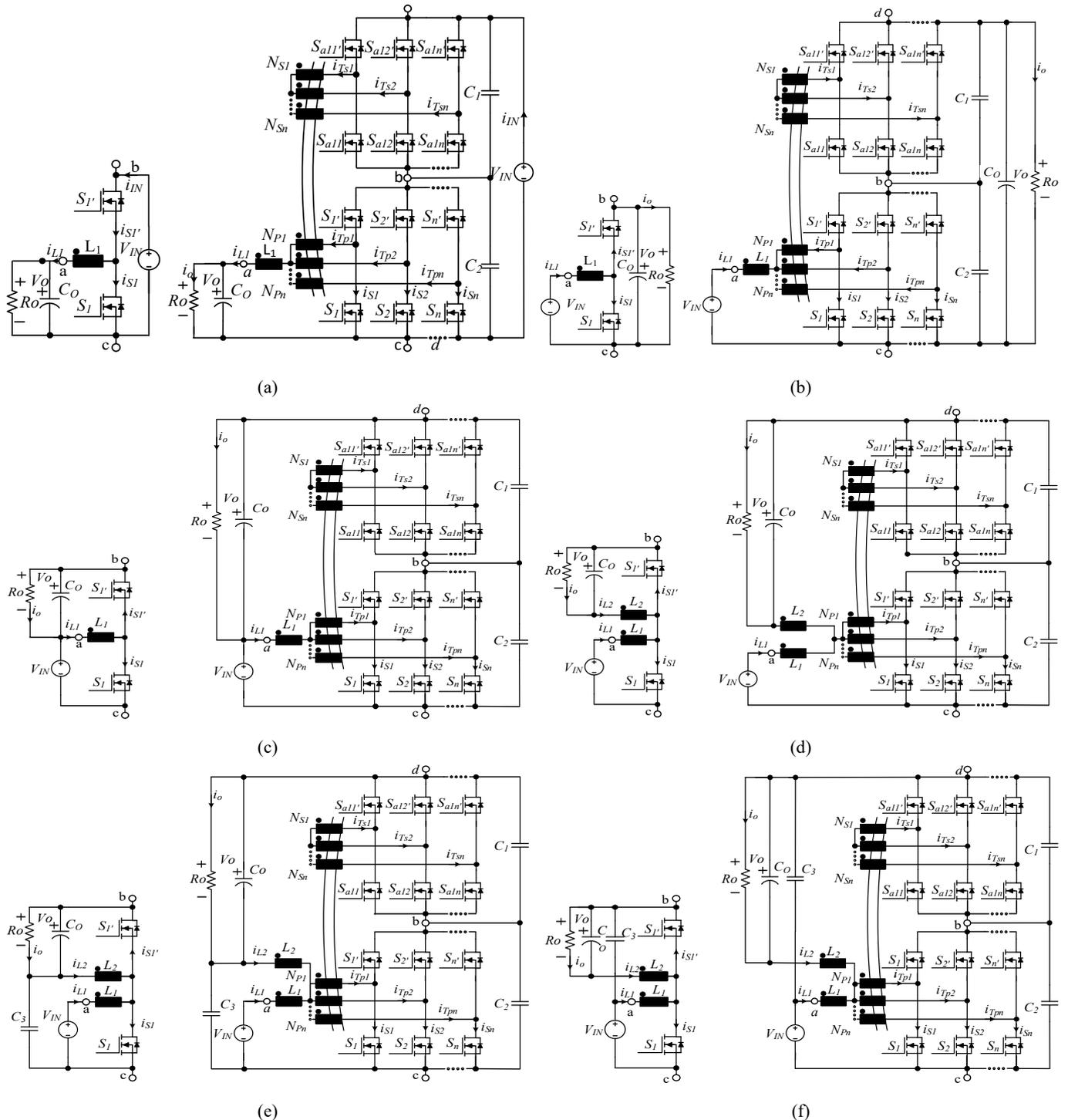
Fig. 2. WCR-MSSC dc-dc converters; (a) buck, (b) boost, (c) buck-boost, (d) Ćuk, (e) SEPIC, and (f) zeta topologies.

- The multiphase transformer allows achieving higher power handling capability;
- The operation frequency of the input storage inductor L_1 is equal to the switching frequency multiplied by the number of legs in the cell, with consequent reduction of size;
- The secondary side of the multiphase transformer can be connected in delta, star, zigzag, or polygon. The detailed analysis of other connection types is not part of the paper scope and will be analyzed in future works.
- By using the multiphase transformer, the voltage ripple across the output filter capacitor is reduced, and consequently its size;
- Considering the particular case of unity turns ratio (n=1), the voltage across the switch is half of the total output voltage, thus, allowing conduction losses reduction when used low voltage MOSFETs.

The transformer turns ratio is defined as $n=N_S/N_P$. The phase-shift for the PWM (pulse width modulation) gating signals in each leg is given by:

$$\phi_{PWM(phase-shift)} = \frac{360°}{\text{number of legs}}. \qquad (1)$$

III. STATIC GAIN OF THE RESULTING DC-DC CONVERTERS

The static gain analysis derived in this section considers that the dc-dc converter shown in Figure 3 operates in continuous conduction mode (CCM) of the current through the storage inductor L_1, when one secondary winding is coupled to the transformer.

A. Buck Converter
The static gain of the classical buck converter is given by:

$$G_V = \frac{V_O}{V_{IN}} = D \qquad (2)$$

where D is the duty cycle.
On the other hand, the static gain of the WCR-MSSC buck converter shown in Figure 2.a is given by:

$$G_V = \frac{V_O}{V_{IN}} = \frac{D}{(1+n)}. \qquad (3)$$

B. Boost Converter
The static gain of the classical boost converter is given by:

$$G_V = \frac{V_O}{V_{IN}} = \frac{1}{(1-D)}. \qquad (4)$$

The static gain of the WCR-MSSC boost converter shown in Figure. 2.b is defined by:

$$G_V = \frac{V_O}{V_{IN}} = \frac{(1+n)}{(1-D)}. \qquad (5)$$

C. Buck-Boost, Ćuk, SEPIC and Zeta Converters
The static gain of the classical indicated converters is given by:

$$G_V = \frac{V_O}{V_{IN}} = \frac{D}{(1-D)}. \qquad (6)$$

On the other hand, the WCR-MSSC indicated converters shown in Figures 2.c, 2.d, 2.e, and 2.f., have similar static gain given by:

$$G_V = \frac{V_O}{V_{IN}} = \frac{(D+n)}{(1-D)}. \qquad (7)$$

It is worth to mention that the duty cycle must be higher than 1/3 in the WCR-MSSC dc-dc converters. Otherwise the voltage induced across the secondary winding of the transformer is not high enough to ensure the energy transfer, thus not allowing the achievement of the desired wide conversion range. However, this issue does not affect the converter operation during startup since the control circuit performs the automatic adjustment of the duty cycle to a given value higher than 1/3. It is only necessary to choose an appropriate turns ratio for this purpose. The PWM signals in the dc-dc converter using the four-state switching cell are displaced by 120°. Therefore, the duty cycle of the switches comprehend the following intervals as explained in [11]: 0 to 1/3, 1/3 to 2/3, and 2/3 to 1. The converter analyzed in this work operates when the duty cycle varies from 1/3 to 2/3 and 2/3 to 1, thus implying that at least two switches are turned on simultaneously during the steady-state operation.

IV. ANALYSIS OF THE WCR-MSSC BOOST CONVERTER

A unidirectional version of the WCR-MSSC dc-dc boost converter shown in Figure 2.b is analyzed in detail in this section. The boost converter has been chosen in this case since it is quite popular in many practical applications if compared with other similar step-up converters. The resulting topology is presented in Figure 3 and comprises the following components: input voltage source V_{IN}; storage inductor L_1; three-phase high frequency transformer with star-star connection T_r; controlled switches S_1-S_3; rectifier diodes D_1-D_9; output filter capacitors C_1, C_2, and C_o; and load resistance R_o. The analysis is performed in steady-state condition considering CCM operation. According to Figure 3, the converter has three legs, as the PWM gating signals are displaced by 120 electrical degrees according to (1).
The main theoretical waveforms of the WCR-MSSC dc-dc boost converter are represented in Figure 4, while some of them are supposed to be presented in Section V in order to validate the converter operation. Besides, it can be seen that star-star (Y-Y) connection is used in the three-phase transformer according to Figure 3.

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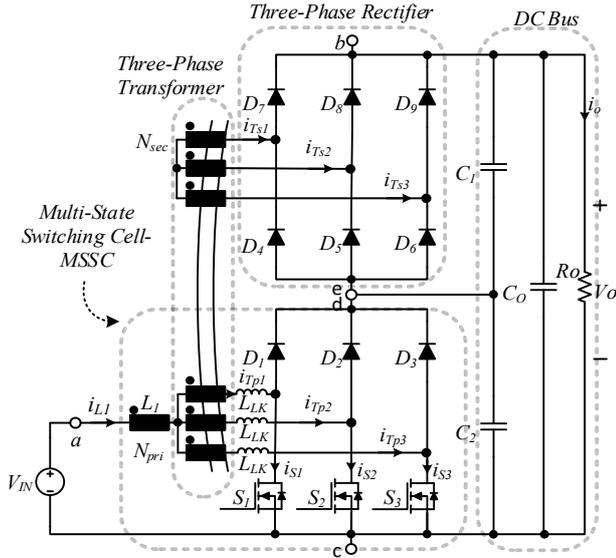
Fig. 3. Unidirectional WCR-MSSC dc-dc boost converter.
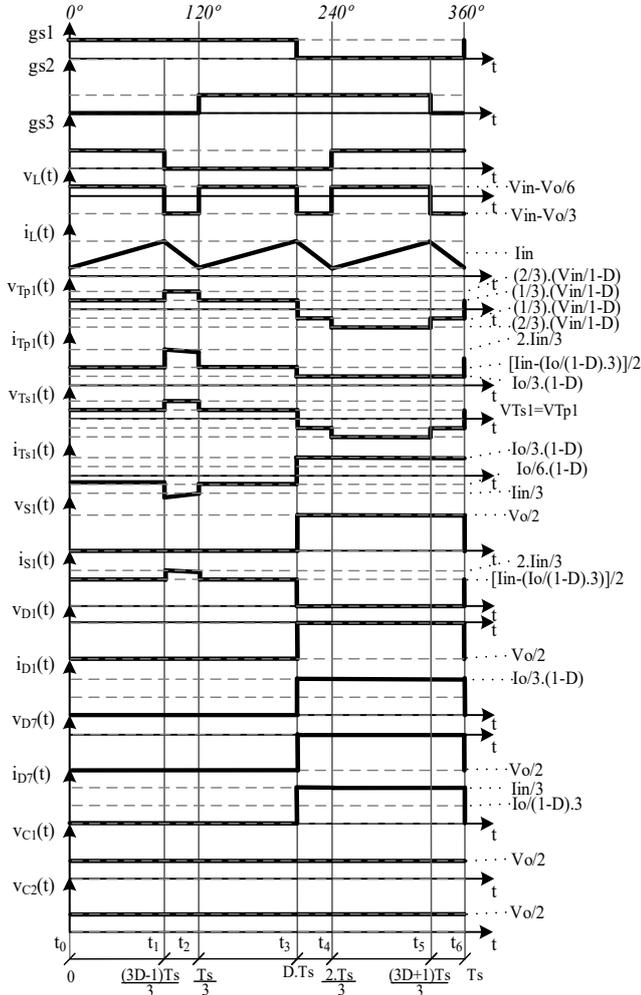
Fig. 4. Main theoretical waveforms.

V. QUANTITATIVE ANALYSIS

In order to design an experimental prototype of the proposed converter, the design specifications given in Table I are considered.

TABLE I
Design Specifications

Description	Parameters
Dc input voltage	$V_{IN} = 86$ V
Output power	$P_O = 3$ kW
Dc output voltage	$V_O = 400$ V
Transformer turns ratio	$n = 1$
Switching frequency	$f_s = 35$ kHz
Inductor current ripple	$\Delta I_{L1} = 0.15 I_I$ A
Duty cycle considering the transformer leakage inductance ($L_{lkg} = 1.3$ µH)	$D = 0.572$
Duty Cycle	$D = 0.57$

A. Duty Cycle

Isolating the duty cycle and substituting the parameters defined in Table I in (5), it is possible to obtain:

$$D = 1 - \frac{V_{IN}(1+n)}{V_O}. \qquad (8)$$

The leakage inductance has little influence on the static gain of the converter, as it can be seen in expression:

$$D_{LK} = 1 + \frac{nP_o f_s L_{LK}}{2V_{IN}V_O} - \frac{V_{IN}(1+n)}{V_O}. \qquad (9)$$

The static gain curves as a function of the duty cycle are shown in Figure 5. If $n=0$, a boost converter using a four-state switching cell is obtained, whose static gain is the same as that of the classical dc-dc boost topology. On the other hand, if $n=1$ or $n=2$, high voltage step-up is achieved. Figure 5 also shows good match between the theoretical and experimental curves.
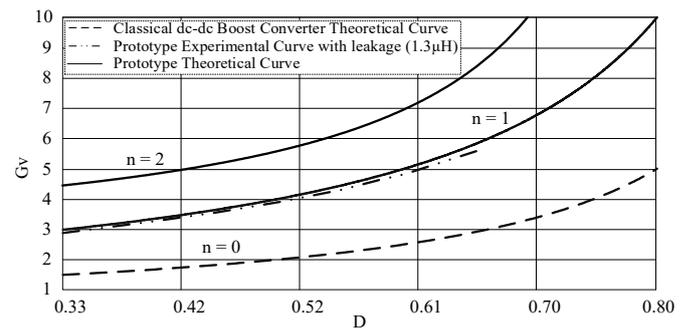
Fig. 5. Theoretical and experimental static gain curves.

B. Three-Phase Transformer

The apparent power of the transformer is given by (10), while its normalized value is defined by (11). Both expressions are valid for duty cycles within the range defined as $1/3<D<2/3$. It is worth to mention that the transformer is responsible for processing 100% of the load power in isolated dc-dc converters, while the transformer in the WCR-MSSC dc-dc boost converter process about 72% of the total power for $n=1$ as shown in Figure 6.

$$S_{T(Appar.)} = \frac{P_o \sqrt{\frac{3 \cdot (5-3D)}{(1-D)^2}}}{6} S_{T(Norm.)} \quad (10)$$

$$S_{T(Norm.)} = \frac{1}{2} - \frac{\sqrt{3 \cdot (7-9D)}\left(1 - \sqrt{(1-n)^2}\right)}{3\sqrt{(5-3D)(1-n)^2}} \quad (11)$$
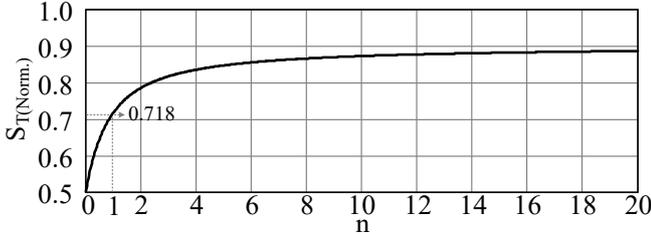
Fig. 6. Normalized apparent power of the transformer for proposed converter when D=0.57.

Ferrite cores IP12 by Thornton were used in the design of the three-phase transformer. Two NC cores are used in the right and left columns, while an NI core is placed at the center position. During the physical implementation, the windings are interleaved between the primary and secondary sides in order to reduce the leakage inductance. Detailed design guidelines are given in [16].

Eventual asymmetries in the converter operation is due to slight differences among the duty cycles of the switches and/or impedances of the transformer windings, which may cause some current imbalance and the consequent causing transformer saturation. In order to minimize such undesirable effects, the technique proposed in [17] can be used, which uses small inductances between the legs of each phase.

The rms currents across the primary and secondary windings of the transformer can be calculated respectively by:

$$I_{Tpef} = \frac{\sqrt{6I_{IN}^2(5-3D)}}{12} \quad (12)$$

$$I_{Tsef} = \frac{\sqrt{\frac{2I_O^2(7-9D)}{(1-D)^2}}}{6} \quad (13)$$

where I_O is the output current.

C. Boost Inductor L_1

The normalized current ripple through the boost inductor L_1 is given by (14) and (15). The curve shown in Figure 6 is plotted according to (14), where it is observed that the current ripple is maximum for D=0.5, and null for D=1/3 and D=2/3.

$$\overline{\Delta I_{L1}} = (2-3D)(3D-1) \quad (14)$$

$$\overline{\Delta I_{L1}} = \frac{9\Delta I_{L1} f_s L_1 (1+n)}{V_0} \quad (15)$$
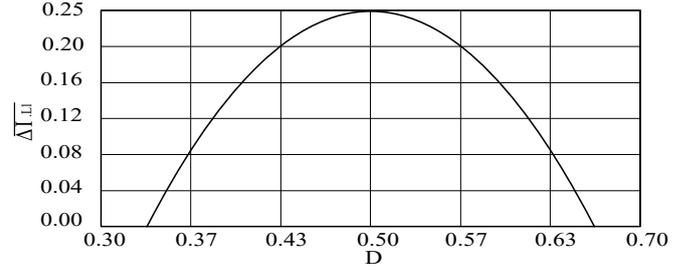
Fig. 7. Normalized current ripple through boost inductor L1.

The inductance is estimated for the maximum normalized current ripple i.e. $\overline{\Delta I_{L1}} = 0.25$, which occurs for D=0.5 as shown in Figure 7. By rearranging (15), the inductance can be determined by:

$$L_1 = \frac{V_O \overline{\Delta I_{L1}}}{9\Delta I_{L1} f_S (1+n)} \quad (16)$$

D. Capacitors C_O, C_1, and C_2

The output filter capacitance can be determined by (17) considering the following parameters: hold-up time t_H =8.33 ms, output power P_o=3000 W, maximum output voltage V_{omax}=400 V, and minimum output voltage V_{omin}=350 V [14].

$$C_O = \frac{2P_O t_H}{(V_{O\max}^2 - V_{O\min}^2)} \quad (17)$$

Capacitors C_1 and C_2 act as voltage dividers, whose capacitances have been chosen as $C_1=C_2$=2.2 μF/400 V. The voltages across the capacitors are then given respectively by:

$$V_{C1} = \frac{V_{IN}}{1-D} \quad (18)$$

$$V_{C2} = \frac{nV_{IN}}{1-D}. \quad (19)$$

E. Switches S1, S2, and S3

The maximum voltage, the rms current and the average current for the active switches are then given respectively by:

$$V_{S1} = V_{S2} = V_{S3} = \frac{V_{IN}}{1-D} \quad (20)$$

$$I_{S1rms} = \frac{\sqrt{2I_{IN}^2(13-7D)}}{12} \quad (21)$$

$$I_{S1avg} = \frac{I_{IN} \cdot (1+D)}{6}. \quad (22)$$

F. Rectifier Diodes $D_1 - D_9$

The maximum reverse voltage, rms current and average current for rectifier diodes D_1-D_9 can be calculated by expressions (23) to (27):

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$$V_{REV(D1-D3)} = \frac{V_{IN}}{(1-D)} \qquad (23)$$

$$V_{REV(D4-D9)} = \frac{nV_{IN}}{(1-D)} \qquad (24)$$

$$I_{RMS(D1-D3)} = \frac{I_O}{3}\sqrt{\frac{1}{(1-D)}} \qquad (25)$$

$$I_{AVG(D1-D3)} = \frac{I_O}{3} \qquad (26)$$

$$I_{RMS(D4-D9)} = \frac{\sqrt{\dfrac{2I_O^2(5-7D)}{(1-D)^2}}}{6}. \qquad (27)$$

VI. EXPERIMENTAL RESULTS

In order to validate the theoretical analysis carried out for the WCR-MSSC dc-dc boost converter, a laboratory prototype rated at 3 kW was implemented and tested, whose component specifications are presented in Table II. Some important results are presented and discussed as follows.

TABLE II
Power Stage Components

Components	Code
Diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9	30CTH03
Switches S_1, S_2, S_3	IRFP4768PbF
Inductor L_1	L_1 = 29.6 µH, δ=3.16 mm (gap) NEE - 65/33/26 (Thornton) N_{L1}= 12 turns (58x25AWG)
Capacitor C_O	08 × 680 µF parallel-connected electrolytic capacitors
Capacitors C_1, C_2	2.2 µF/400 V polyester capacitors
Three-phase Y-Y transformer	2 x NC 100/57/25 and 1 x NI-100/24/25 (Thornton) N_p=N_s=12 turns (22×25AWG)

Figure 8 shows a photograph of the experimental setup.
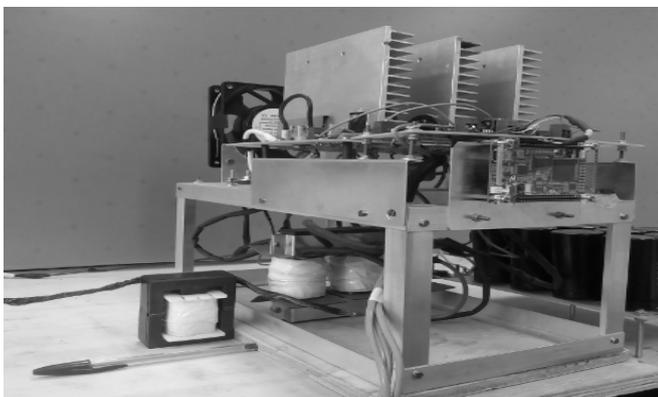
Fig. 8. Picture of the assembled prototype.

Firstly, it is worth to mention that the experimental voltage and current waveforms are somewhat different than those predicted in the theoretical analysis due to the transformer leakage inductance.

Figure 9 shows the current through boost inductor L_1 (CH3), and the currents through the primary windings of the three-phase transformer ((CHR3), (CHR2), and (CHR1), respectively), which are displaced by 120°. It is noteworthy that the operating frequency of the boost inductor is three times the switching frequency, with consequent reduction of its size, weight, and volume.
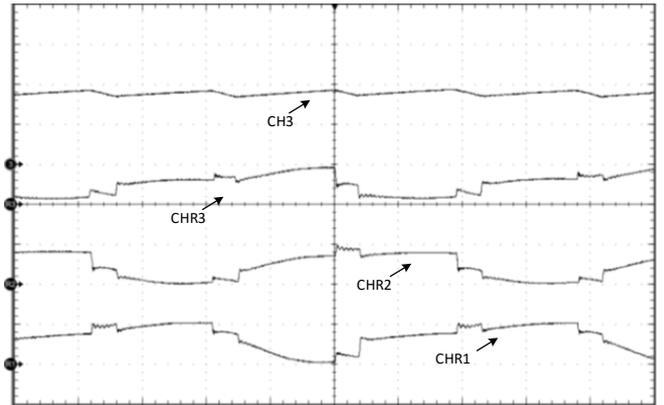
Fig. 9. Current through boost inductor L_1 (CH3, 30 A/div.) and current through primary windings of the three-phase transformer (CHR3, CHR2, CHR1, 20 A/div.) (5 us/div.).

Figures 10 and 11 show the waveforms for the voltage and current in the primary and secondary windings of the three-phase transformer, whose operating frequency is equal to the switching frequency.

Figure 12 presents the voltage and current waveforms in active switch S_1. The voltage across the switches is clamped at the maximum theoretical value $Vo/2$ for n=1 due to the presence of capacitor C_2, which is part of the WCR-MSSC.

In order to verify the voltage balance across capacitors C_1 and C_2, the corresponding waveforms in Figure 13 were obtained.

Finally, Figure 14 represents the converter efficiency as a function of the output power, which is about 96% at the rated power condition.
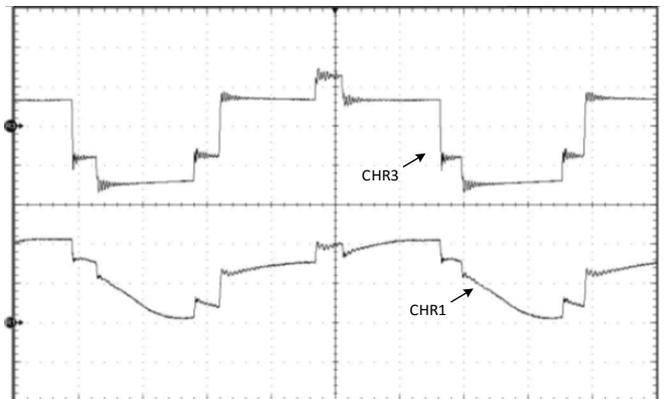
Fig. 10. Voltage (CHR3, 100 V/div.) and current (CHR1, 10 A/div.) in the primary winding of the three-phase transformer (5 µs/div.).

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Fig. 11. Voltage (CHM1, 100 V/div.) and current (CHM2, 10 A/div.) in the secondary winding of the three-phase transformer (5 μs/div.).

Fig. 12. Voltage (CH2, 100 V/div.) and current (CH4, 10 A/div.) in switch S_1 (5 μs/div.).

Fig. 13. Total output voltage (CHR4, 200 V/div.), and voltages across C_1 (CH4, 100 V/div.) and C_2 (CHR3, 100 V/div.) (5 μs/div.).

Fig. 14. Efficiency as a function of the output power for the proposed dc-dc converter with wide conversion range based on the MSSC.

VII. CONCLUSION

This paper has presented six novel nonisolated dc-dc converters with wide conversion range based on the MSSC. It is worth to mention that the topologies are derived from classical buck, boost, buck-boost, Ćuk, SEPIC, and zeta converters. Potential applications include power supply systems using photovoltaic modules, small wind energy conversion systems, and fuel cells. That is, dc-dc converters are, typically, input stages of grid-tie inverters.

The advantages of the proposed converters are: low voltage stresses across the switches, thus allowing the use of switches with reduced on-resistance; wide conversion range depending on the number of secondary windings with series-connected rectifier stages; distribution of the load current among several semiconductors thus allowing achieving power levels higher than 5 kW; the current through the primary winding is nearly null during a given time interval (1-D), which implies the minimization of current unbalance among the branches due to small variations of the duty cycle applied to the switches. However, a possible disadvantage of the proposed approach lies in high component count.

In order to verify the claimed advantages, a WCR-MSSC dc-dc boost converter has been thoroughly analyzed, while the quantitative analysis, and experimental results have been presented. Considering the experimental results obtained in steady-state condition, it has been shown that no voltage and current overshoot occur in the waveforms. Besides, the voltages across the switches are naturally clamped by the voltage divider composed of capacitors C_1 and C_2. The efficiency measures at rated power condition is about 96%, even though it can be further improved with the use of high quality devices. After a brief literature review on similar approaches [18], [19], it has been found typical efficiencies range from 95% to 98% considering the adopted power levels, what also occurs in the proposed converter.

ACKNOWLEDGMENT

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BIOGRAPHIES

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