COUPLED-INDUCTOR HIGH STEP-UP INTEGRATED TOPOLOGIES: SYNTHESIS, ANALYSIS AND EXPERIMENTAL RESULTS

Jacson R. Dreher[1], António M. S. S. Andrade[2], Luciano Schuch[2], Mário L. da S. Martins[2]
[1]Federal Institute of Santa Catarina, Chapecó – SC, Brazil
[2]Federal University of Santa Maria – UFSM, Santa Maria – RS, Brazil
e-mail: antoniom.spencer@gmail.com

***Abstract* – This paper presents a new integration concept to generate high voltage step-up non-isolated DC/DC converters with the aid of coupled-inductors. The integration concept relies on the separation of the converter circuit into two or three parts named input, middle and output sections. Hence, any basic converter can partially or fully share one of its sections with another basic converter since both circuits comply with the integration rules. The merged converters become an integrated topology with fewer components. According to this paper, for the input section parallel integration, the circuits remaining output sections can be associated in three different ways, in a series, parallel or cascaded connection. These output sections associations allow for a merged topology to enhance their voltage gain that becomes the sum of the voltage gains of the former topologies alone. An example of integration of the boost and flyback converter is provided to illustrate the theory. The resulting integrated topologies are theoretically and experimentally evaluated. The results prove that the integration methodology is an effective way to obtain high voltage conversion ratio circuits and that the derived topologies are highly efficient due to their low converter series resistances.**

***Keywords* - DC-DC Converters; High Voltage Gain, Integration of Converters.**

I. INTRODUCTION

In recent years, most of the renewable resources have been successfully explored with the aid of highly efficient power processing systems comprised by electronic power converters that convert the maximum available power into electricity. Electricity is fed directly to the grid or converted into a high density storage system [1, 2]. In photovoltaic and fuel cell resources, for instance, as well as in batteries and other storage systems, there is a large variety of DC voltage levels to fit in the AC grid specifications, making the integration of the renewable resource to the grid a cumbersome and challenging task [3]. Since the development of PV system technologies is driven by the reduction of the cost per watt of the produced electricity, more decentralized topologies have been proposed. Many of them present an individual Maximum Power Point Tracking (MPPT) feature [4]. In addition, aiming to reduce the losses that many power conversion stages will produce, the minimum number of power converters in the power flow is preferable, as it maximizes power conversion efficiency. However, it yields more complex integrated circuits for power converters.

In applications where a low DC voltage is available (small photovoltaic arrays, fuel cell stacks, super capacitors or battery sources), a high voltage step-up is often required in order to provide the possibility to connect a standard H-bridge inverter to the grid (usually 110V or 220V). As a result of such high voltage gain in a single standard power stage, the converter series resistances (CSR) of the converter circuit components degrade the system efficiency and voltage gain [5, 6].

To overcome this drawback presented by the boost and buck-boost topologies, the high step-up voltage gain is accomplished by means of a number of non-isolated high step-up DC/DC converters that employ a sort of modification that minimizes the CSR effect over the converter characteristics by means of the reduction of the MOSFET RMS current or duty-cycle. The former approach is achieved introducing interleaved PWM cells to share the converter current (non-isolated [7]-[8], and isolated [9]-[10]), meanwhile the latter is accomplished by a plenty of different ways, such as introducing switched inductors [11]-[12], switched capacitors (passively [11],[13]-[14] and actively [15]), cascaded [16]-[17] or stacked PWM cells [18-19], magnetic coupling of transformers [20]-[22], or a combination of two or more techniques [23]-[26].

One simple approach to achieve voltage adjustment is to employ the turns ratio of some magnetic component, such as

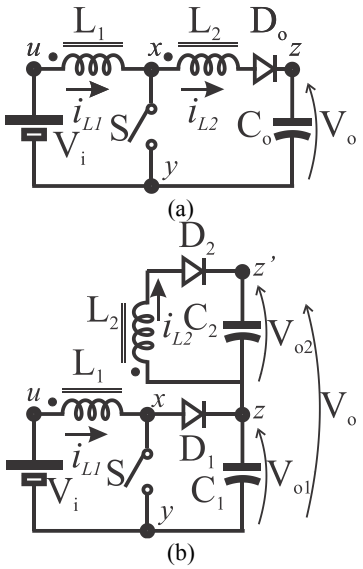


Fig. 1. Coupled-Inductor Boost-flyback converter. (a) Coupled inductor boost converter [30]; (b) Integrated boost flyback [31].

[1]Manuscript received 07/08/2015; first revision 05/11/2015; second revision 08/04/2016, accepted for publication 08/04/2016, by recommendation of Editor Henrique A. C. Braga.

a transformer [20]-[22] or a coupled-inductor [27]-[29]. Since isolation is not required, the turns ratio of the coupled-inductor is used to provide high voltage gain as illustrated in Figure 1, [30] and [31]. In spite of its simplicity, this solution for the high voltage gain has some drawbacks, most of which are relative to concerning the leakage of the coupled-inductor.

The use of the coupled-inductor is not new; it was already used to integrate two converter circuits in [31]. In the integrated topology, the coupled-inductor is shared by the boost and the flyback circuits whose outputs are connected in series. Other topologies can be also integrated by means of the operation of coupled-inductors [32]-[35].

This paper presents a novel methodology to generate high voltage gain non-isolated DC/DC converters based on the integration of two standard DC/DC converters. It permits to generate an entire family of converters with high voltage gain feature. Besides the high voltage gain, some of the generated DC/DC topologies present a natural voltage clamping for the MOSFET, avoiding the necessity of extra auxiliary clamping or snubbing circuitry.

II. THE GENERAL INTEGRATION CONCEPT

DC/DC power converters are comprised by a set of components located in a well-known distribution that must agree with a set of network rules as described in [36]. In that study, the most fundamental converters are defined and hereafter they are named standard DC/DC converters. Such topologies are constituted by one pair of PWM switches and a set of energy storage components. They are supplied by a single power source and provide support to a single load, maintaining a unidirectional power flow from the source to the load.

As explained in detailed in [36], the converter components are arranged in a ladder structure that can be grouped into three parts or sections named as follows, Input, Middle and Output sections (Figure 2). Each section can be characterized as a voltage or current type circuit for the input and output sections, and as an inductive or capacitive buffer for the middle section. Thus, the ladder structure is formed by a sequence of consecutive voltage-current-voltage type sections or current-voltage-current type sections.

TABLE I
Section types of Eleven Standard DC/DC converters

Standard DC/DC converts	DC/DC Converter Sections Type		
	Input	Middle	Output
Buck	Voltage	----	Current
Boost	Current	----	Voltage
Buckboost	Voltage	Inductive	Voltage
SEPIC	Current	Capacitive + Inductive	Voltage
Zeta	Voltage	Inductive + Capacitive	Current
Cuk	Current	Capacitive	Current
Forward (*)	Voltage	----	Current
Flyback (*)	Voltage	Inductive	Voltage
Cúk (*)	Current	Capacitive	Current
SEPIC (*)	Current	Inductive + capacitive	Voltage
Zeta (*)	Voltage	Inductive + capacitive	Current

(*) Isolated topologies

The Input section consists of a voltage source or a current source and a semiconductor (switch). The current source is formed by a voltage source in series with a large inductor. By contrast, other hand, the middle section consists of one or more energy storage elements (inductors and/or capacitors). Therefore, the middle section with an inductor works like a current buffer and the middle section with a capacitor works like a voltage buffer. It should be noticed that the middle section can consist of one or more energy buffers. Finally, as like the input section, the output section can be a voltage type or current type. The current type is formed by a large inductor followed by a parallel connection between a capacitor and a resistive load, while the voltage type only has the parallel connection of capacitor and a resistive load.

Table I shows the eleven standard DC/DC converters and their respective sections type.

A. The Integration Property of the Input Section

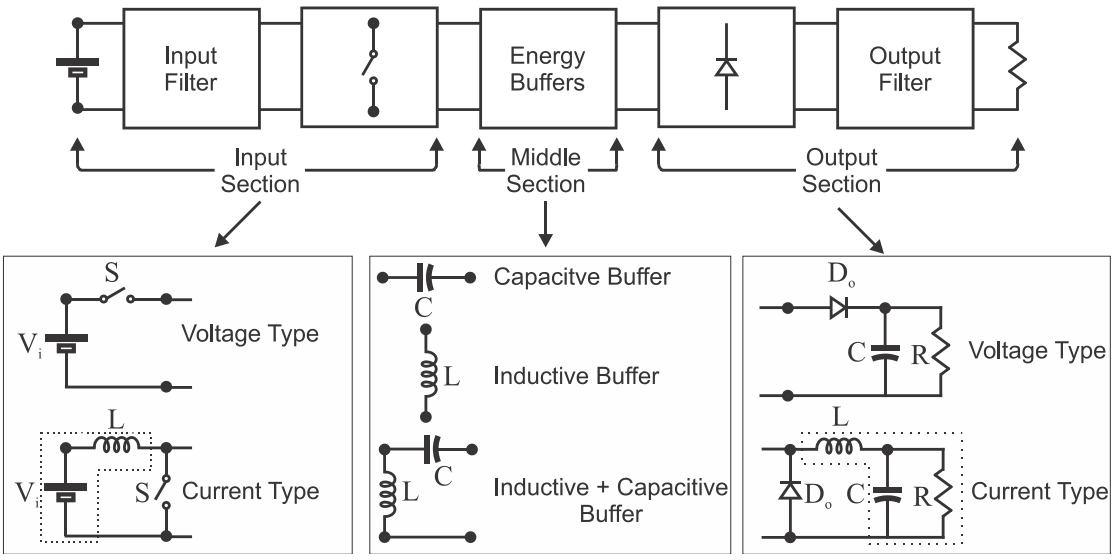


Fig. 2. Input, Middle and Output sections

From the previous section, it became evident that some topologies present the same sections type, i.e., boost and SEPIC converters present the same current type input section. Therefore, one can state that:

Integration concept: *"Any identical section of two distinct converters that could be shared produces a merged topology. Such topology that complies with the constraints defined in [36] is considered an integrated topology."*

And also limiting the concept to the Input section is the,

Input section integration concept:

1. *"Any **identical** current type input section of two distinct converters that could be shared produces a merged topology. Such topology that complies with the constraints defined in [16] is considered an integrated topology. Hitherto, this kind of merged topology will be referred of Identical integrated converter resultant of the **Identical integration**"*
2. *"Any current type input section that could be shared with a voltage type input section followed by an inductive buffer (**similar** circuit) produces a merged topology. Such topology that complies with the constraints defined in [16] is considered an integrated topology. Hitherto, this kind of merged topology will be referred of Similar integrated converter resultant of the **Similar integration**".*

In the flowchart shown in Figure 3, the input sections of two standard DC/DC converters are analyzed in details. For the flowchart it is assumed that 'Converter A' is a non-isolated converter and 'Converter B', is an isolated converter. Taking into account that both converters belong to those described in Table 1, the integration process is explained as follows.

In the first flowchart test, the 'Converter A' is tested for current type Input section. If it is positive, the topology is labeled with numeral "1", otherwise, Input section is of the voltage type, and thus, it is tested again for inductive buffer (Middle section). If the second test answer is positive, the topology is labeled with numeral "2". If both tests are negative, the flow output is labeled with "5", where "1" stands for current type input section, "2" for voltage type

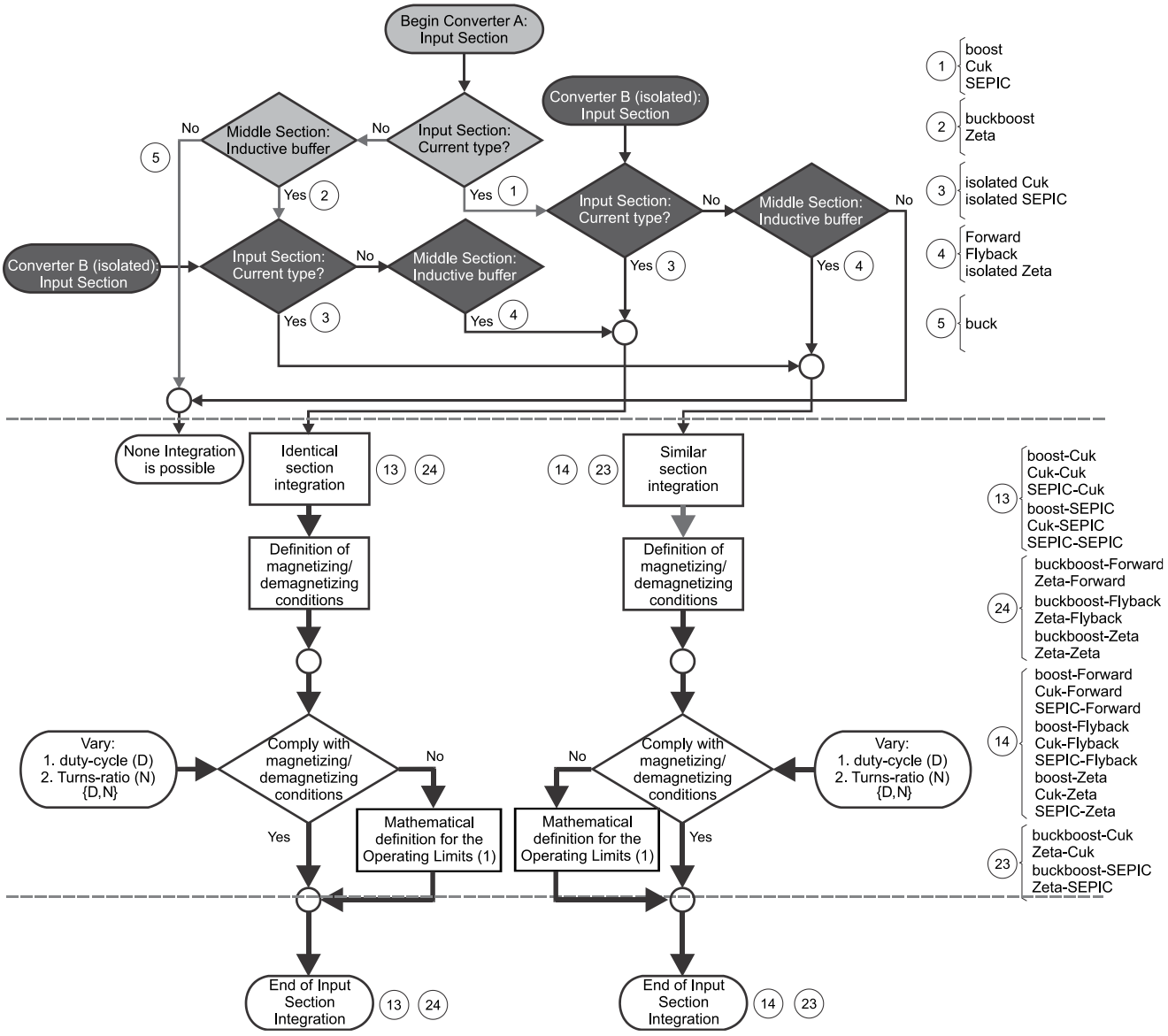


Fig. 3. Flowchart of input section integration applied to standard DC/DC converters.

input section followed by inductive buffer and “5” stands for voltage type without inductive buffer. For any ‘Converter A’ labeled with “1” or “2”, provides possible Input section integration, since it obeys the concept defined previously.

A Similar procedure is followed for the ‘Converter B’, i. e., it is tested for current type Input section yielding in label “3” for a positive answer. On the contrary, Input section is of voltage type, and, thus, it is tested again for inductive buffer in the Middle section. If the second test is positive, the topology is labeled with numeral “4”, where “3” stands for current type input section, “4” for voltage type input section followed by inductive buffer. For any ‘Converter B’ labeled with “3” or “4”, the integration is possible. If both tests are negative there is no possible integration for the input section.

As can be seen on the right side of the flowchart (Figure 3) all the standard DC/DC converters defined in Table I are classified according to the flowchart labels. After classifying the Input section, one can see that there are four possible paths to follow to achieve an Input section integration, and they form the numbers “13”, “14”, “23” and “24”. Numbers “13” and “24” result from two identical current and voltage type input sections, respectively. Meanwhile, numbers “14” and “23” yield a similar current with voltage type input section integration. Once again, on the right side of the flowchart (Figure 3), all the possible identical and similar integrations for the input section are listed.

The possible merged topologies are summarized in Figure 4, where Figure 4(a) and Figure 4(b) represent the converters labelled as “13” and “24” (Identival integration); and Figure 4(c) represents the converters labelled “14” and “23” (Similar integration).

With the input circuit merged, the magnetizing and demagnetizing condition for each converter are defined and tested for parametric variations of the converter duty-cycle and transformer (coupled-inductor) turns ratio (N).

The magnetizing and demagnetizing condition of the inductor are given by (1) and (2), respectively:

$$V_L = V_i > 0 \; for \; \forall \; group \tag{1}$$

$$V_L = \begin{cases} V_i - V_{xy} < 0, & for\ group\ \text{“13” and “14”} \\ V_{ux} < 0, & for\ group\ \text{“24” and “23”} \end{cases} \tag{2}$$

B. Association of the Output Section

From the previous section, it can be seen that in any of the three diagrams of Figure 4, the Output sections are independent from each other. In other words, they can supply different isolated loads. Nevertheless, the output sections of a merged converter can be combined to provide an enhancement in the output current or the output voltage. This section will show that there are actually three possible combinations, named series association, parallel association and cascaded association, as shown in the general diagrams of Figure 5. As can be seen, in the series association (Figure 5(a)), the output capacitors C_{o1} and C_{o2} are in series, providing the sum of their voltages to the load R. On the other hand, capacitors C_{o1} and C_{o2} are in parallel association in the circuit of Figure 5(b), thus, both output section currents contribute in an additive way to their charge, as well as for the load R. In the cascade association (Figure 5(c)), the output capacitor C_{o1} contributes additively to the capacitor

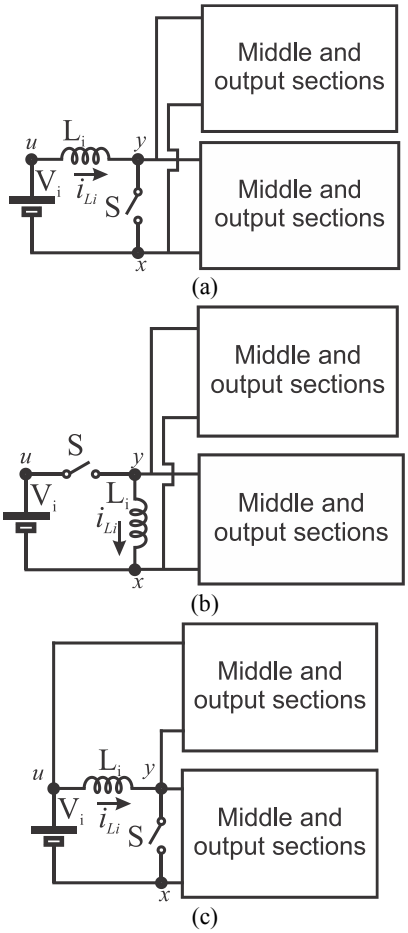


Fig. 4. Possibility of Integration.

C_{o2} circuit loop, yielding a similar result when the output sections are connected in series.

In order to derive the possible integrated circuits with the association of their output sections, the flowchart shwon in Figure 6 has been developed.

For the first flowchart test, ‘Converter A’ is tested for current type output section. If it is positive, the topology is labeled with “C”, where “C” stands for current. On the other way, the output section is of voltage type and labeled with “V”, where “V” stands for voltage. A similar test is conducted for ‘Converter B’.

After classifying the Output sections, one can see that there are four possible paths to follow, and they form “CV”, “CC”, “VV” and “VC”. Labels “CC” and “VV” result from two identical current and voltage type output sections, respectively. Meanwhile, labels “CV” and “VC” yield a combined current and voltage type output section association.

After the Output section of the converters has been defined, then the output section association is tested. Initially it is tested for series association. If it is positive, the association is labeled with “SO”. Alternatively, it is not a “SO” then it is tested for parallel association. If the test answer is positive, the association is labeled with “PO”. If not it must be a cascade association and is labeled with “CO”.

As can be seen on the right side of flowchart of Figure 6, all the standard DC/DC converters defined in Table 1 are

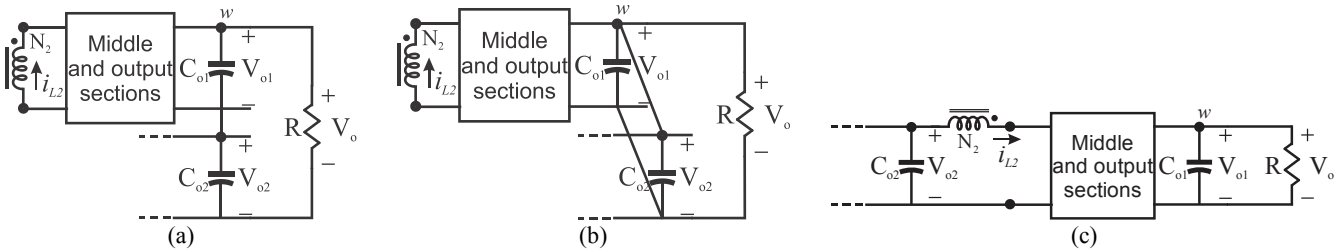


Fig. 5. Diagrams for the possible association of the two outputs of the integrated converters (a) Series association of the outputs; (b) Parallel association of the outputs; (c) Cascade association of the outputs.

classified according to the flowchart labels, and all the possible associations for their output section are listed.

After the output sections connection has been defined, the relationship of the integrated topology output variables with former converters are given as follows.

For the integrated converter with series output sections (SO), the output voltage V_o is the sum of voltages V_{oA} and V_{oB}, while the average values of the output currents i_{DoA} and i_{DoB} must be equal, so only the ripple current passes through the output capacitors. Thus,

$$V_o = V_{oA} + V_{oB} \quad (3)$$

$$I_o = I_{oA} = I_{oB} \quad (4)$$

The voltage stress across the output diodes D_{oB} and D_{oA} is dependent of V_{oA} and V_{oA}, respectively. It means that none must be rated for the entire output voltage V_o, which can be advantageous.

For the integrated converter with parallel output sections (PO), the output voltage V_o is equal to any of the voltages V_{oA} and V_{oB}, while the average values of the output currents i_{DoA} and i_{DoB} are summed through the load R. Hence,

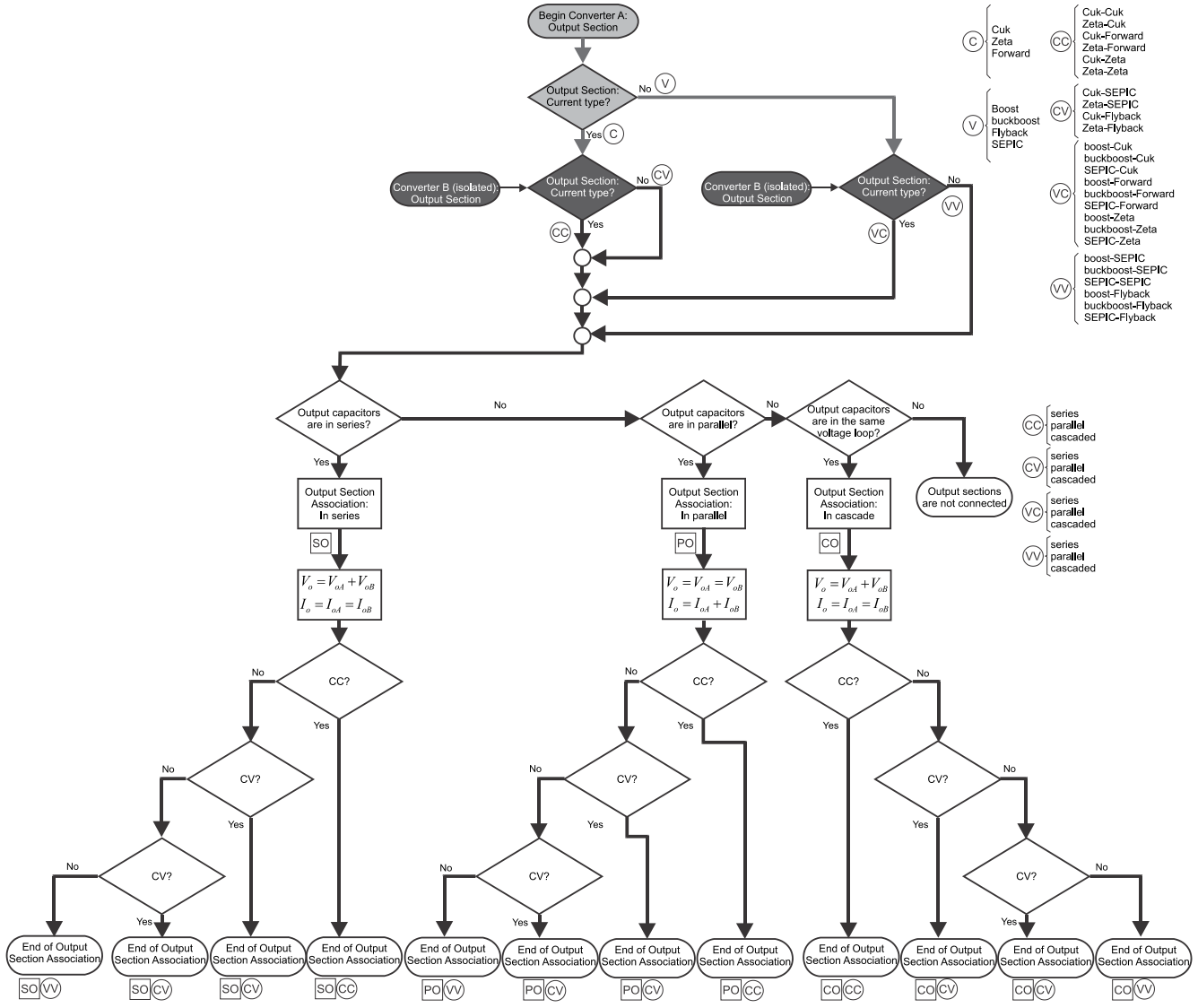


Fig. 6. Flowchart of output section association applied to standard DC/DC converters.

$$V_o = V_{oA} = V_{oB} \quad (6)$$

$$I_o = I_{oA} + I_{oB} \quad (7)$$

It can be observed that the current stress through the output diodes D_{oA} and D_{oB} is dependent of the current gain of each converter. In other words, none of the output diodes must be rated for the entire output current.

Finally, for the integrated converter with cascade output sections (CO), the output voltage V_o is the sum of the voltages V_{oA} and V_{oB}, while the average values of the output currents i_{DoA} and i_{DoB} must be the same since only the ripple of the currents pass through the capacitors. Like the series association of the Output Sections, the voltage stress across the output diodes D_{oA} and D_{oB} is dependent of V_{oA} and the difference between V_{oB} and V_{oA}, respectively. Hence, none of them must be rated for the entire output voltage V_o. For the cascaded association of the outputs, the expressions (3) and (4) are also applied.

At the end of the flowchart of Figure 6, any pair of tested converter yields an integrated topology with precisely defined output variables.

Table II and Table III summarize the results of the flowcharts shown in Figure 5 and Figure 6.

Note that, in addition, many integrated converters are described in Tables II and III, but due to operating condition limitations, number of components and other characteristics, some of them are noteworthy to be developed.

The next section explores mathematical definitions for the Boost and Flyback converter integration as a case study

III. CASE STUDY: INTEGRATED BOOST-FLYBACK

According to Table II, the boost-flyback input section integration is one case of Similar integration (label 14 from flowchart in Figure 5) where a current type input section (from boost) is merged with a voltage type input section (from flyback), as long as it is followed by an inductive buffer. Their output sections are both of voltage type (label VV from flowchart in Figure 6) with low voltage ripple and

TABLE II
Summary of possibility of integration of standard converters (Part 1)

Type of Input Section (Converter A)	Type of Input Section Integration	Type of Merged Converter	Type of Output Section	Type of Output Section Association	Integrated Converter
1	13	Boost-Cuk	VC	SO	Boost-Cuk with Series Output
				PO	Boost-Cuk with Parallel Output
				CO	Boost-Cuk with Cascaded Output
		Cuk-Cuk	CC	SO	Cuk-Cuk with Series Output
				PO	Cuk-Cuk with Parallel Output
				CO	Cuk-Cuk with Cascaded Output
		SEPIC-Cuk	VC	SO	SEPIC-Cuk with Series Output
				PO	SEPIC-Cuk with Parallel Output
				CO	SEPIC-Cuk with Cascaded Output
		Boost-SEPIC	VV	SO	Boost-SEPIC with Series Output
				PO	Boost-SEPIC with Parallel Output
				CO	Boost-SEPIC with Cascaded Output
		Cuk-SEPIC	CV	SO	Cuk-SEPIC with Series Output
				PO	Cuk-SEPIC with Parallel Output
				CO	Cuk-SEPIC with Cascaded Output
		SEPIC-SEPIC	VV	SO	SEPIC-SEPIC with Series Output
				PO	SEPIC-SEPIC with Parallel Output
				CO	SEPIC-SEPIC with Cascaded Output
	14	Boost-forward	VC	SO	Boost-forward with Series Output
				PO	Boost-forward with Parallel Output
				CO	Boost-forward with Cascaded Output
		Cuk-forward	CC	SO	Cuk-forward with Series Output
				PO	Cuk-forward with Parallel Output
				CO	Cuk-forward with Cascaded Output
		SEPIC-forward	VC	SO	SEPIC-forward with Series Output
				PO	SEPIC-forward with Parallel Output
				CO	SEPIC-forward with Cascaded Output
		Boost-flyback	VV	SO	Boost-flyback with Series Output
				PO	Boost-flyback with Parallel Output
				CO	Boost-flyback with Cascaded Output
		Cuk-flyback	CV	SO	Cuk-flyback with Series Output
				PO	Cuk-flyback with Parallel Output
				CO	Cuk-flyback with Cascaded Output
		SEPIC-flyback	VV	SO	SEPIC-flyback with Series Output
				PO	SEPIC-flyback with Parallel Output
				CO	SEPIC-flyback with Cascaded Output
		Boost-Zeta	VC	SO	Boost-Zeta with Series Output
				PO	Boost-Zeta with Parallel Output
				CO	Boost-Zeta with Cascaded Output
		SEPIC-Zeta	VC	SO	SEPIC-Zeta with Series Output
				PO	SEPIC-Zeta with Parallel Output
				CO	SEPIC-Zeta with Cascaded Output

TABLE III
Summary of possibility of integration of standard converters (Part 2)

Type of Input Section (Converter A)	Type of Input Section Integration	Type of Merged Converter	Type of Output Section	Type of Output Section Association	Integrated Converter
2	23	Buckboost-Cuk	VC	SO	Buckboost-Cuk with Series Output
				PO	Buckboost-Cuk with Parallel Output
				CO	Buckboost-Cuk with Cascaded Output
		Zeta-Cuk	CC	SO	Zeta-Cuk with Series Output
				PO	Zeta-Cuk with Parallel Output
				CO	Zeta-Cuk with Cascaded Output
		Buckboost-SEPIC	VV	SO	Buckboost-SEPIC with Series Output
				PO	Buckboost-SEPIC with Parallel Output
				CO	Buckboost-SEPIC with Cascaded Output
		Zeta-SEPIC	CV	SO	Zeta-SEPIC with Series Output
				PO	Zeta-SEPIC with Parallel Output
				CO	Zeta-SEPIC with Cascaded Output
	24	Buckboost-forward	VC	SO	Buckboost-forward with Series Output
				PO	Buckboost-forward with Parallel Output
				CO	Buckboost-forward with Cascaded Output
		Zeta-forward	CC	SO	Zeta-forward with Series Output
				PO	Zeta-forward with Parallel Output
				CO	Zeta-forward with Cascaded Output
		Buckboost-flyback	VV	SO	Buckboost-flyback with Series Output
				PO	Buckboost-flyback with Parallel Output
				CO	Buckboost-flyback with Cascaded Output
		Zeta-flyback	CV	SO	Zeta-flyback with Series Output
				PO	Zeta-flyback with Parallel Output
				CO	Zeta-flyback with Cascaded Output
		Buckboost-Zeta	VC	SO	Buckboost-Zeta with Series Output
				PO	Buckboost-Zeta with Parallel Output
				CO	Buckboost-Zeta with Cascaded Output
		Zeta-Zeta	CC	SO	Zeta-Zeta with Series Output
				PO	Zeta-Zeta with Parallel Output
				CO	Zeta-Zeta with Cascaded Output

thus, suited for output section series connection (VV-SO). Nevertheless they can also be associated in parallel (VV-PO) and cascaded (VV-CO) connections.

A. Parallel input integration condition

An analysis of the boost and flyback Input sections is made at following to give more details about the input section integration, the boost and flyback Input sections. Figure 7(a) shows both Input Sections combined in parallel, i.e., sharing the same input voltage V_i. Considering that the switches of each Input Section operate simultaneously, the Input Section components may be re-organized as depicted in Figure 7(b). It is also possible to note that the inductors voltage for boost and flyback, respectively, are given by,

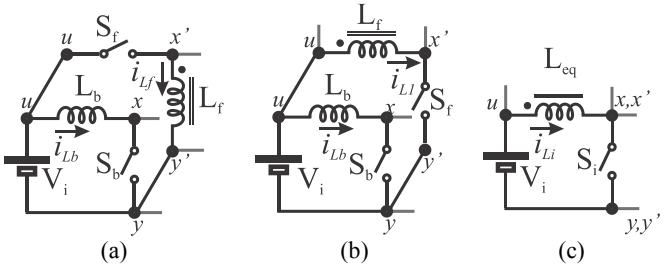


Fig. 7. Integration of the Input Sections for the boost and flyback converters. (a) Same input voltage; (b) Input Section components re-arranged; (c) Integration completed.

$$V_{LB} = \begin{cases} V_i, & for\ S_{B(on)} \\ V_i - V_{oB}, & for\ S_{B(off)} \end{cases} \tag{8}$$

And

$$V_{LF} = \begin{cases} V_i, & for\ S_{F(on)} \\ -\dfrac{V_{oF}}{N}, & for\ S_{F(off)} \end{cases} \tag{9}$$

Given that,

$$V_{oB} = \frac{V_i}{1-D} \tag{10}$$

And

$$V_{oF} = \frac{V_i D}{1-D} \tag{11}$$

Expressions (8) and (9) become,

$$V_{LB} = V_{LF} = \begin{cases} V_i, & for\ S_{B,F(on)} \\ \dfrac{-V_i D}{1-D}, & for\ S_{B,F(off)} \end{cases} \tag{12}$$

Hence, it can be observed that the inductances L_B and L_F are both magnetized and demagnetized by the same voltages. This result ensures that both inductances may be shared, as well as the switches. It leads to the circuit in Figure 7(c), where the expression (13) is valid.

$$i_i = \frac{2V_i}{L_{eq}} t + i_i(t_0) \tag{13}$$

where, $i_i(t_0) = i_{LB}(t_0) = i_{LF}(t_0)$ and $L_{eq} = \frac{L_B L_F}{L_B + L_F}$.

From (8) through (13) it can be seen that the magnetizing and demagnetizing voltages of inductance L_{eq} are the same as for separate inductances L_B and L_F, which ensures the condition to merge both Input sections into a single Integrated Input section.

B. Principle of Operation

In order to perform the theoretical analysis of the integrated boost-flyback converters and access their characteristics, the Boost-flyback with Series Output (Table II) has been chosen to demonstrate the principle of operation for the integrated topologies. For information on the principle of operation of the Boost-flyback with Parallel Output and Boost-flyback with Cascade Output (Table II), see [37].

Aiming to make the following analyses simpler, some assumptions are made as follows. The coupled-inductor is modeled by the N-port representation of the Cantilever model, which comprises a magnetizing inductance L_1, a leakage inductance L_{o2}, and an ideal transformer, with a turns ratio given by *N*. The capacitors are large enough so that the voltages V_{oB} and V_{oF} can be considered constant in a switching period. The semiconductors are ideal (lossless).

The Boost-flyback with Series Output converter operating in continuous conduction mode (CCM) assumes four power stages for a switching period. The equivalent circuit stages are shown in Figure 8 and are briefly described as follows.

1) Stage 1 - At instant t_0, switch *S* is turned on, the voltage across the magnetizing inductance is positive and the magnetizing current increases with a slope of V_i / L_m. Diode D_{oB} is reverse biased and the current through diode D_{oF} (i_{oF}) reduces linearly.

2) Stage 2 - At instant t_1, current i_{oF} reaches zero and diode D_{oF} turns off. Since both diodes are off, the output capacitors supply the load. This is a magnetizing interval that lasts until the switch is turned off.

3) Stage 3 - From instant t_2, the switch S is turned off, forcing the diodes D_{oF} and D_{oB} to conduct. Initially, D_{oB} assumes all the current. Nevertheless, i_{DoB} decreases linearly, and the D_{oF} current increases in the same proportion.

4) Stage 4 - At t_4, diode D_{oB} turns off. From this instant, diode D_{oF} conducts the demagnetizing current of the coupled-inductor.

The key waveforms of the converter are shown in Figure 9. It can be noticed that, although the input current i_1 is discontinuous, the magnetizing current i_{L1} is continuous, ensuring the CCM characteristics to the converter. The magnetizing process of L_1 begins at t_0 and lasts until t_2. Nevertheless, this process is quite dependent on the MOSFET on state that determines the interval from t_1 to t_2, where the converter duty-cycle is given by $D=D_1+D_2$. On the other hand, the demagnetizing process depends on two stages, the stage governed by D_{oB} conduction (t_2 through t_3) and a second stage governed by D_{oF} conduction (t_3 through t_0). The demagnetizing process can be related to the converter duty-cycle as $(1-D)=D_3+D_4$.

C. Steady-state analysis

In the steady state, the time integral of the primary winding voltage V_1 of the coupled-inductor over one time period must be zero, that is:

$$\int_0^{T_s} V_1 dt = 0 \therefore \int_0^{t_2} V_i dt + \int_{t_2}^{t_3} (V_i - V_{oB}) dt + \int_{t_3}^{T_s} k_1 V_{oF} dt = 0 \qquad (14)$$

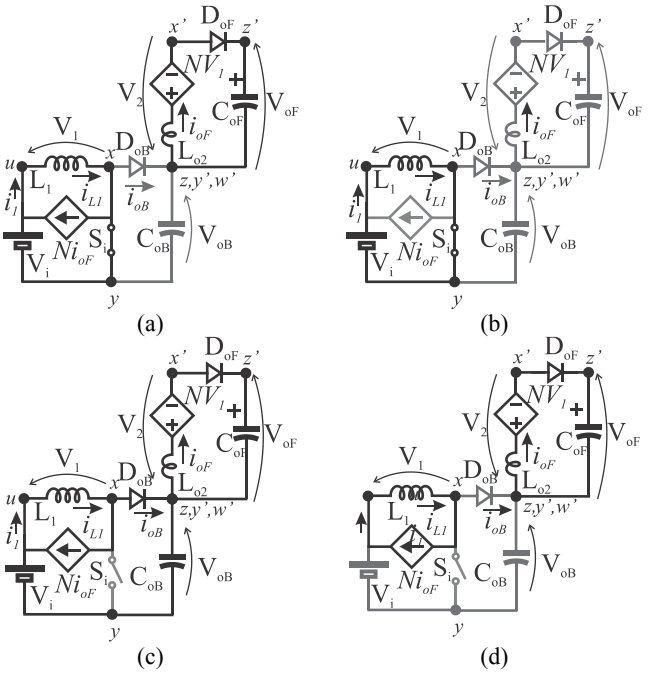


Fig. 8. Boost-Flyback with Series Output converter. (a) Converter Stage 1; (b) Converter Stage 2; (c) Converter Stage 3; (d) Converter Stage 4.

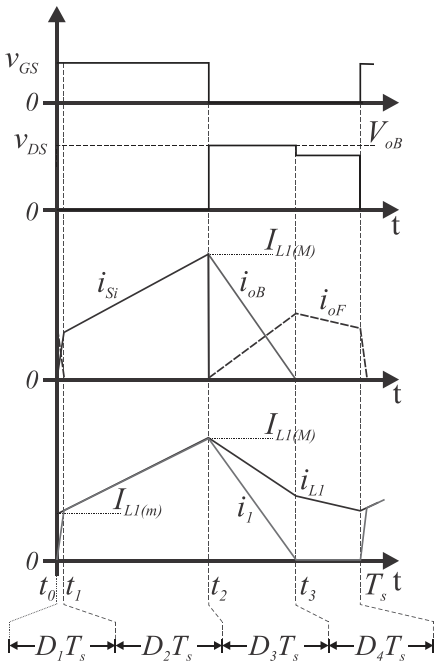


Fig. 9. Boost-Flyback with Series Output converter main waveforms.

where,

$$\int_0^{t_2} V_i dt = V_i D T_s , \tag{15}$$

$$\int_{t_2}^{t_3} \left(V_i - V_{oB}\right) dt = \frac{-\left(V_i - V_{oB}\right) L_{o2} I_{L1(M)}}{\left(\left(\frac{L_{o2}}{L_1}\right) + N^2\right)\left(V_i - V_{oB}\right) + N V_{oF}} , \tag{16}$$

$$\int_{t_3}^{T_s} k_1 V_{oF} dt = -\frac{L_1 N V_{oF}}{\left(L_{o2} + L_1 N^2\right)}\left(T_S - t_3\right) \tag{17}$$

and

$$t_3 = D T_S + \frac{L_{o2} I_{L1(M)}}{\left(\left(\frac{L_{o2}}{L_1}\right) + N^2\right)\left(V_i - V_{oB}\right) + N V_{oF}} \tag{18}$$

Substituting (15) through (18) in (14) the voltage V_{oF} can be found as,

$$V_{oF} = V_i \frac{ND}{(1-D)}\left(1 + \frac{L_{o2}}{N^2 L_1} - \frac{L_{o2} I_{L1(M)}}{N V_i (1-N) T_s}\right) \tag{19}$$

From the definition of the given by (4), it can be found that,

$$I_{oB} = I_o \therefore \frac{1}{T_s}\int_{t_2}^{t_3} i_{oB} dt = \frac{I_{L1(M)}\left(t_3 - t_2\right)}{2T_s} = I_o \tag{20}$$

Reorganizing (20) yields in,

$$\left(t_3 - t_2\right) = \frac{2T_s I_o}{I_{L1(M)}} \therefore \left(t_3 - t_2\right) = \frac{2T_s I_1}{I_{L1(M)}}\left(\frac{1-D}{ND+1}\right) \tag{21}$$

Since t_3-t_2 is obtained from (18), it can be written,

$$\frac{2T_s I_1}{I_{L1(M)}}\left(\frac{1-D}{ND+1}\right) = \frac{-L_{o2} I_{L1(M)}}{\left(\left(\frac{L_{o2}}{L_1}\right) + N^2\right)\left(V_i - V_{oB}\right) + N V_{oF}} \tag{22}$$

Finally, substituting (19) in (22) and solving it for V_{oB}, results in

$$V_{oB} = \frac{V_i}{(1-D)}\left(1 + \frac{L_{o2} I_{L1(M)}}{V_i T_s} \frac{\left(\left(\frac{I_{L1(M)}(ND+1)}{2I_1}\right) - 1\right)}{\left(\frac{L_{o2}}{L_1}\right) + N^2}\right) \tag{23}$$

Hence, the output voltage of the Boost-Flyback converter with Series Output, operating in continuous conduction mode (CCM) is obtained by,

$$V_o = V_{oB} + V_{oF} \tag{24}$$

By (19) and (23) it can be noticed that the output voltage (24) depends on coupled-inductor parameters L_{o2}, L_1 and N; as well as converter parameters $I_{L1}(M)$, I_1 and the switching period T_s. Figure 10 shows the influence of L_{o2} and N on the converter voltage gain, (24). The numerical simulation parameters are V_i=25V, I_1=7.35A, L_1=40µH, L_k=2µH and T_s=20µs. It became evident that the converter voltage gain increases exponentially with the coupled inductor turns ratio. On the contrary, the voltage gain is reduced by the increase of the leakage inductance L_{o2}. For low duty-cycle values, this behavior is more expressive.

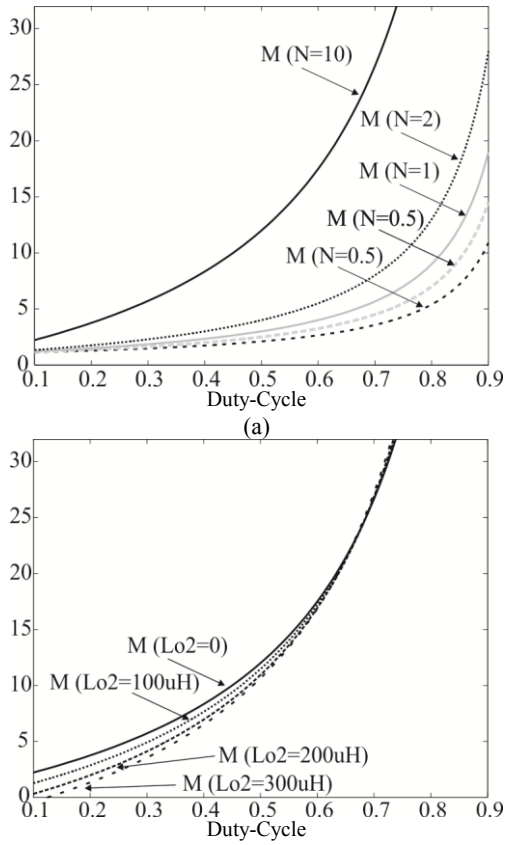


Fig. 10. Boost-Flyback with Series/Cascaded Output converter voltage gain in function of duty-cycle. (a) For L_{o2}=0 and a set of values of N; (b) For N=10 and a set of values for L_{o2}.

D. Continuous current Conduction Mode operation limits

Intending to keep the converter operation in CCM, i.e., ensure the existence of the four stages of the Boost-flyback with Series Output converter described in previous section, the following restriction must be complied. It should be highlighted that the converter can operate out of these limits, nevertheless, the CCM is no longer ensured, as well as the definition of voltage gain given in (24).

1) Magnetizing stage condition: To ensure the magnetizing stage (t_1-t_2), the following expression must be valid.

$$D_1 T_s < D T_s \tag{25}$$

Developing this expression results in,

$$D_{B1} > \frac{-\frac{L_{o2}}{2L_1} - \frac{\sqrt{k_2\left(k_2 + \left(\frac{8 I_1 L_{o2} N (1+N)}{V_i T_s}\right)\right)}}{2} + N^2}{N k_2} \tag{26}$$

where, $k_2 = 2N^2 + \frac{L_{o2}}{L_1}$.

From (24) one can find that the duty-cycle must be kept at a value slightly higher than the lower boundary given by D_{B1}.

2) Demagnetizing stage condition: Analogously, in order to ensure the demagnetizing stage (t_3-T_s), the following expression must be valid.

$$D_3 T_s < (1-D) T_s \tag{27}$$

Developing this expression yields,

$$D_{B2} < \frac{-1-\sqrt{1+\left(\frac{8 I_1 L_1 N (1-N)}{V_i T_s}\right)}}{2N} \tag{28}$$

From (28) one can find that the duty-cycle must be kept at a value slightly lower than the higher boundary given by D_{B2}.

The expressions (26) and (28) form two dotted lines that limit a region (gray) where the four operating stages exists in the converter circuit operation. They are shown in Figure 11. One can see that the CCM operation is ensured for a large amount of voltage gain and duty-cycle values.

E. Voltage and current stresses on Device

The maximum voltage stress across the switch and boost diode is given by (29). That is, the voltage stress on the switch and boost diode are equal to the boost output section voltage only.

$$V_{DS} = V_{DoB} = V_{oB} \tag{29}$$

And the maximum voltage across the flyback diode is given by (30). Note the voltage stress on the flyback diode is associated to the turns ratio of the coupled inductor.

$$V_{DoF} = V_{oF} + N V_i \tag{30}$$

With respect to the current stresses, the RMS current value in the switch is given by:

$$I_{Si(rms)} = \sqrt{\frac{1}{T_s}\int_0^{t_1} i_{Si}{}^2 dt + \frac{1}{T_s}\int_{t_1}^{t_2} i_{Si}{}^2 dt + \frac{1}{T_s}\int_{t_2}^{t_3} i_{Si}{}^2 dt + \frac{1}{T_s}\int_{t_3}^{T_s} i_{Si}{}^2 dt} \tag{31}$$

where,

$$\frac{1}{T_s}\int_0^{t_1} i_{Si}{}^2 dt = \left(\frac{k_1}{L_{o2}} + \frac{V_i}{L_1}\right)^2 \frac{t_1{}^3}{3} \tag{32}$$

$$\frac{1}{T_s}\int_{t_1}^{t_2} i_{Si}{}^2 dt = \left(\frac{V_i}{L_1}\right)^2 \frac{(t_2-t_1)^3}{3} + k_2 I_{L1(m)} (t_2-t_1)^2 \left(\frac{V_i}{L_1} + \frac{k_2 I_{L1(m)}}{(t_2-t_1)}\right) \tag{33}$$

$$\frac{1}{T_s}\int_{t_2}^{t_3} i_1{}^2 dt = 0 \tag{34}$$

$$\frac{1}{T_s}\int_{t_4}^{Ts} i_1{}^2 dt = 0 \tag{35}$$

The maximum current through the switch is:

$$I_{Si(M)} = \frac{Vi}{L_1} D + i_{L1(t1)} \tag{36}$$

The RMS current value in the flyback diode is given by:

$$I_{DoF(rms)} = \sqrt{\frac{1}{T_s}\int_0^{t_1} i_{DoF}{}^2 dt + \frac{1}{T_s}\int_{t_1}^{t_2} i_{DoF}{}^2 dt + \frac{1}{T_s}\int_{t_2}^{t_3} i_{DoF}{}^2 dt + \frac{1}{T_s}\int_{t_3}^{T_s} i_{DoF}{}^2 dt} \tag{37}$$

where,

$$\frac{1}{T_s}\int_0^{t_1} i_{DoF}{}^2 dt = \left(\frac{k_1}{L_{o2}} + \frac{V_i}{L_1}\right)^2 \frac{t_1{}^3}{3} \tag{38}$$

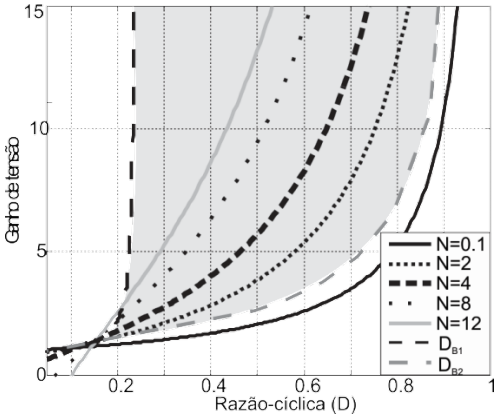


Fig. 11. Boost-Flyback with Series Output converter voltage gain in function of duty-cycle with CCM operation boundaries, D_{B1} and D_{B2}.

$$\frac{1}{T_s}\int_{t_1}^{t_2} i_{DoF}{}^2 dt = 0 \tag{39}$$

$$\frac{1}{T_s}\int_{t_2}^{t_3} i_{DoF}{}^2 dt = k_5{}^2 \frac{(t_3-t_2)^3}{3} \tag{40}$$

$$\frac{1}{T_s}\int_{t_4}^{Ts} i_{DoF}{}^2 dt = k_6 \frac{(T_S-t_3)^3}{3} + \frac{k_5 I_{L1M}}{k_3+k_4}(T_S-t_3)\left(k_6(T_S-t_3) + \frac{k_5 I_{L1M}}{k_3+k_4}\right) \tag{41}$$

The maximum current through the flyback diode is:

$$I_{DoF(M)} = \frac{N}{\frac{L_{o2}}{L_1} + N(N+1)}\left(\frac{Vi}{L_1} D + i_{L1(t1)}\right) \tag{42}$$

the RMS current value in the boost diode is given by:

$$I_{DoB(rms)} = \sqrt{\frac{1}{T_s}\int_0^{t_1} i_{DoB}{}^2 dt + \frac{1}{T_s}\int_{t_1}^{t_2} i_{DoB}{}^2 dt + \frac{1}{T_s}\int_{t_2}^{t_3} i_{DoB}{}^2 dt + \frac{1}{T_s}\int_{t_3}^{T_s} i_{DoB}{}^2 dt} \tag{43}$$

where,

$$\frac{1}{T_s}\int_0^{t_1} i_{DoB}{}^2 dt = 0 \tag{44}$$

$$\frac{1}{T_s}\int_{t_1}^{t_2} i_{DoB}{}^2 dt = 0 \tag{45}$$

$$\frac{1}{T_s}\int_{t_2}^{t_3} i_{DoB}{}^2 dt = \frac{(k_3+k_4)^2 (t_3-t_2)^3}{3} + I_{L1(M)}(t_3-t_2)\left((k_3+k_4)(t_3-t_2) + I_{L1(M)}\right) \tag{46}$$

$$\frac{1}{T_s}\int_{t_4}^{Ts} i_{DoB}{}^2 dt = 0 \tag{47}$$

where the k's coefficient are given bellow:

$$k_1 = N(N V_i + V_{oF}) \tag{48}$$

$$k_2 = 1 + \frac{L_{o2}}{L_1}\frac{V_i}{k_1} \tag{49}$$

$$k_3 = \left(\frac{L_{o2}}{L_1} + N^2\right)\frac{\left(V_i - V_{oB}\right)}{L_{o2}} \tag{50}$$

$$k_4 = N\frac{V_{oF}}{L_{o2}} \tag{51}$$

The maximum current in the boost diode is:

$$I_{oB(M)} = \frac{Vi}{L_1}D + i_{L1(t1)} \tag{52}$$

As can be seen, the current stresses on the devices are associated with the coupled inductor, turns ratio, magnetizing inductance and leakage inductance.

IV. DESIGN AND EXPERIMENTAL RESULTS

To confirm the theory presented in the previous section, an application to a PV system is taken into account to provide a straightforward design for guidelines and laboratory experimentation.

A. Definitions for the application

In order to evaluate the theoretical analysis, a PV application has been selected. The PV system is comprised by a single module (KC-200GT) whose characteristics are summarized in Table IV. When making use of a PV module model the data of the MPPT points to a temperature of 25° as shown in Table V.

B. Simplified design guidelines

The design guidelines employed in this paper consist of the following steps:

1) The converter voltage gain is defined by,

$$M = \frac{V_o}{V_{i(M)}} \therefore M = \frac{250}{26.3} \approx 9.5 \tag{53}$$

2) Assuming D = 0.5, the average magnetizing current is given by,

$$I_{L1} = \frac{I_{i(M)}\left(M - D\right)}{MD} \therefore I_{L1} \approx 13.6A \tag{54}$$

3) Hence, assuming that $\Delta I_{L1} = 10\% I_{L1(M)} = 1.36A$, the magnetizing inductance can be calculated as,

$$L_1 = \frac{V_{i(M)}DT_s}{2\Delta I_{L1}} \therefore L_1 \approx 96.6\mu H \tag{55}$$

4) Finally, when making use of expression (24) and the parameters given in Table IV and Table V, the value of the turns ratio (N) that satisfies the previous steps can be found by means of numerical simulation. Thus, $N \geq 8$. It should be noted that expression (24) does not account for the converter series resistance, which means that in practice, N should be a little higher than the calculated value. Hence, the values chosen for this application are equal to ten (N=10).

TABLE IV
PV characteristics for the KC-200GT module

Parameters		
Symbol	**Description**	**Value**
P_{MAX}	Maximum power	200 Wp
V_{MPP}	Voltage at maximum power	26.3 V
I_{MPP}	Current at maximum power	7.61 A
V_{OC}	Open circuit voltage	32.9 V
I_{SC}	Short circuit current	8.21 A

TABLE V
Maximum Power Points for a 25° C temperature

Parameters			
Irradiation	**V_{MPP}**	**I_{MPP}**	**P_{MAX}**
1000 Wp/m^2	26.30 V*	7.61 A**	200.14 W
800 Wp/m^2	25.99 V	6.17 A	160.35 W
600 Wp/m^2	25.53 V	4.62 A	117.94 W
400 Wp/m^2	24.95 V	3.07 A	76.59 W
200 Wp/m^2	24.04 V	1.53 A	36.78 W

* $V_{i(M)}$, ** $I_{i(M)}$,

The Boost-Flyback with Cascaded Output converter follows the same procedure and a similar one can be adopted to the circuit design of the Boost-Flyback with Parallel Output converter.

C. Experimental Set-up and results

Following the design guidelines shown in the preceding Section, a 50 kHz, 200 W Boost-Flyback with Series Output converter prototype has been implemented to verify the operation and the performance of the Integrated converters.

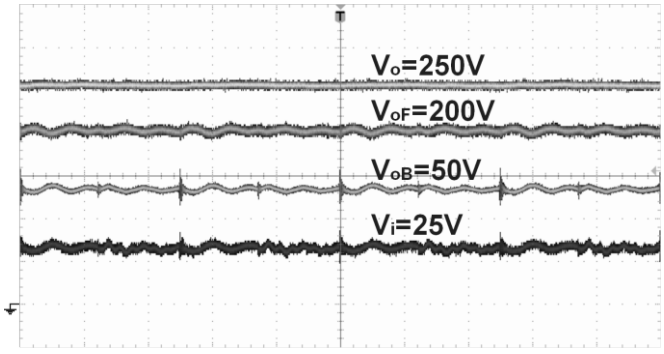
For the laboratory tests, the power circuit employs a DC voltage source and supplies resistive load. The combination of the DC voltage and load values provides similar operating points to the converter as those defined in Table V. The prototype main components are summarized in Table VI.

Figure 12(a) shows the waveforms for the output voltage of converter, the output voltage of boost and flyback section and the input voltage. As can be seen, the output voltage is the sum of the output voltage of boost and flyback section (V_o=V_{oB}+V_{oF}), which is ten times as high as the input voltage. Figure 12(b) shows the voltage waveforms across the semiconductors. The voltage across the flyback diode (V_{DF}) reaches 500V, i.e., it is twice as much as times the output voltage. Nevertheless, the boost diode voltage (V_{DB}) and the MOSFET voltage (V_S) reach only 50V, which is five times lower than the output voltage. This ensures the use of

TABLE VI
Prototype Parameters

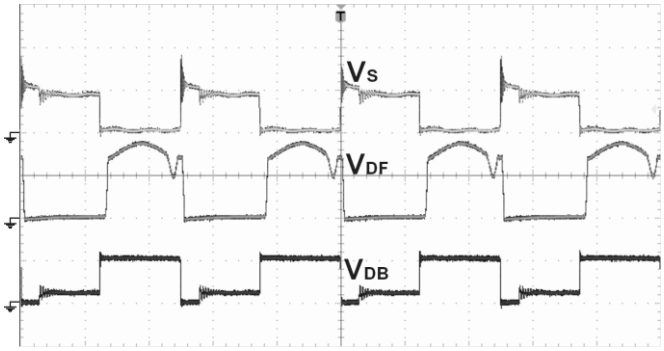
Parameters	
Symbol	**Value**
P_{iMAX}	200 W
M (V_O /V_{iM})	9.5 (250 V /26.3 V)
f	50 kHz
N	10
L_1	96.6 µH
S	IRF150N*/IRF350N
D_{BOOST}	MBR20200ct
$D_{FLYBACK}$	C4D20120

* Boost-Flyback with Series and Cascaded Output converter prototypes
** Boost-Flyback with Series and Parallel Output converter prototypes



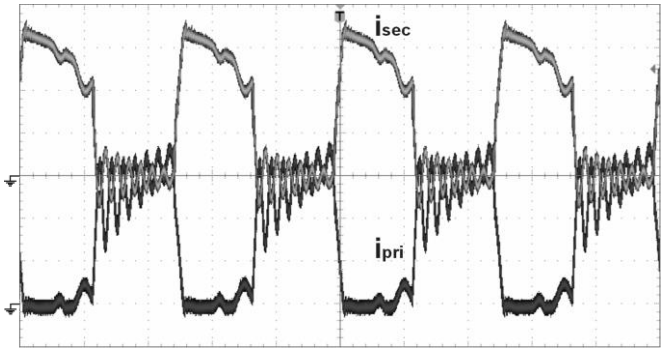
V_i: 20V/div; V_{oB}: 20V/div; V_{oF}: 50V/div; V_o: 50V/div; time 8µs/div

(a)



V_{DB}: 50V/div; V_{DF}: 250V/div; V_S: 50V/div; time 8µs/div

(b)



i_{pri}: 5A/div; i_{sec}: 0.5A/div; time 8µs/div

(c)

Fig. 12 Prototype experimental waveforms. (a) Main voltage waveforms; (b) Main semiconductor voltage waveforms; (c) Main current waveforms.

low breakdown voltage MOSFETs and, consequently low drain to source resistance devices. Figure 12(c) shows the current waveforms across the primary and secondary of coupled inductor, where it can be seen that the input current (i_{pri}) is about five times higher than the output current (i_{sec}).

Aiming to evaluate the performance of the Boost-Flyback with Series Output converter, its efficiency has been evaluated for the set of irradiation values determined by Table III and compared to the Boost-Flyback with Parallel and Cascaded Output converter prototypes.

In can be seen in Figure 13(a) that Boost-Flyback with Series Output converter prototype achieved the highest efficiency for the entire solar irradiation range, reaching a maximum value of 91.806% at 400 W/m^2. It is slightly better than the Boost-Flyback with Cascaded Output converter prototype, when both are using the same 100 breakdown voltage MOSFET (IRFP150N).

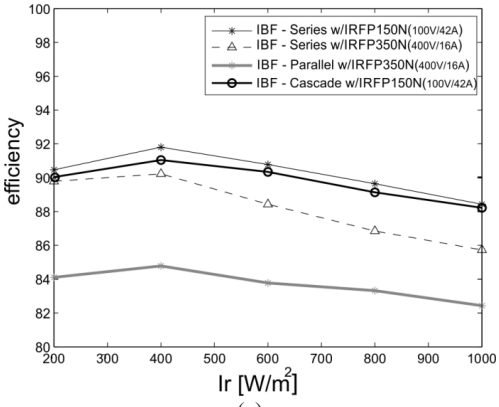
On the other hand, the Boost-Flyback with Parallel Output converter prototype presented the lowest efficiency. This difference is consequence of its higher conductions losses, since it make use of a 400 breakdown voltage MOSFET (IRFP350N).

Comparing the Boost-Flyback with Series Output converter prototype using the IRFP350N MOSFET, it can be seen that this higher on resistance device reduces efficiency, however, this prototype still overwhelm the efficiency of the Boost-Flyback with Parallel Output converter.

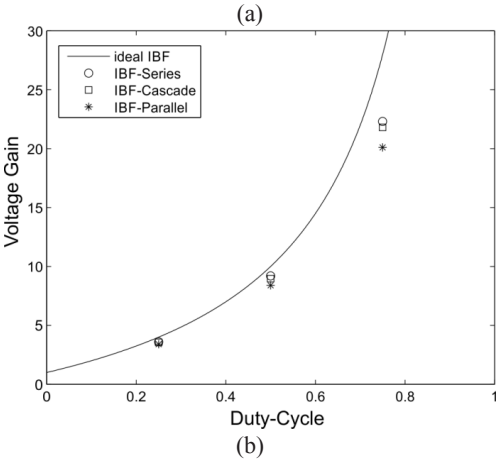
Figure 13(b) shows the static voltages gain of the Boost-Flyback with Series/Cascaded Output converters. The ideal Integrated Boost-Flyback $\left(\frac{V_o}{V_i}=\frac{1+ND}{1-D}\right)$ has been also plotted to show how much the converter actual CSR affected the results. For a duty-cycle range smaller than 0.5, the Integrated Boost-Flyback converter prototypes present similar values for the voltage gain. Nevertheless, for higher static voltage gain values, i.e., at severe duty-cycles, the Boost-Flyback with Series Output converter prototype is more suitable.

V. CONCLUSION

This paper presents a systematic methodology to generate high step-up static voltage gain converters based on the combination of two standard DC/DC converters. By means of the separation of the converter circuits into three sections,



(a)



(b)

Fig. 13. Prototype performance. (a) Efficiency curve; (b) Voltage gain comparison.

input, middle and output sections, identical or similar sections can be merged into a single integrated converter. As long as the merged input section obeys a set of rules, the Input section integration is accomplished. The remaining output sections are associated in three different combinations, giving rise to three distinct circuits. Each of them is capable of providing a higher voltage gain that corresponds to the sum of its former converters. In addition to the general rules, two intuitive flowcharts provide guidance for applying the integration concept to any standard DC/DC converter. Actually, the methodology is applied to eleven standard converters yielding seventy-two integrated topologies.

Aiming to further explore the characteristics of such converters, the Integrated boost-flyback converters have been studied and peer analyzed.

Experimental results obtained from laboratory prototypes proved the reliability of the integration methodology and also pointed out to the Boost-Flyback with Series Output converter as the strongest option for high voltage gain applications. It is a consequence of the low breakdown voltage MOSFET technologies that can be used with this prototype.

ACKNOWLEDGEMENTS

The authors would like to thank the Brazilian Research Council (CNPq) for providing financial support by means of the Project Process 481612/2012-2 and 309748/2012-7.

REFERENCES

[1] E.N. Chaves, E.A.A. Coelho, H.T.M. Carvalho, L.C.G. Freitas, J.B.V. Júnior, L.C. Freitas, "Projeto de Controlador Baseado no Modelo Interno com 1 Grau de Liberdade Utilizado em Injeção de Potência Ativa na Rede Monofásica a Partir de Geração Fotovoltaica," Eletrôn. Potên., Campo Grande, v. 20, n. 2, p. 172-184, mar./mai. 2015 (in Portuguese).

[2] J.G. de Matos, L.A. de S. Ribeiro, F.S.F. Silva, "Controle da Potência Gerada em Microrredes Autônomas e Isoladas com Fontes de Energia Renováveis e Sistema de Armazenamento com Bancos de Baterias," Eletrôn. Potên., Campo Grande, v. 19, n. 2, p. 152-162, mar./mai. 2014 (in Portuguese).

[3] R.F. Coelho, L. Schmitz, L.T. Macedo, D. C. Martins, "Estratégia para Controle do Fluxo de Potência em uma Microrrede Híbrida Destinada a Alimentação de Cargas CC Críticas," Eletrôn. Potên., Campo Grande, v. 20, n. 2, p. 205-214, mar./mai. 2015 (in Portuguese).

[4] P.A. Sobreira Jr., F.L. Tofoli, H.A.C. Braga, P.G. Barbosa, A.A. Ferreira, "Analysis Of MPPT Techniques Applied To The DCM Multiphase Boost Converter for the Mitigation of Partial Shading in PV Arrays," Eletrôn. Potên., Campo Grande, v. 18, n. 4, p. 1138-1148, set./nov. 2013.

[5] R.W. Erickson and D. Maksimović, Fundamentals of power electronics, 2nd ed., Springer, 883 p.

[6] G.M. Buiatti, J.A.M. Ramos, J.A. Martínez, A.M.R. Amaral, A.J.M. Cardoso, "Online Monitoring of Capacitors in Power Converters," Eletrôn. Potên., Campo Grande, v. 16, n. 2, p. 177-186, mar./mai. 2011.

[7] W. Li, Y. Zhao, J. Wu, X. He, "Interleaved High Step-Up Converter With Winding-Cross-Coupled Inductors and Voltage Multiplier Cells," IEEE Trans. Power Electron., vol. 27, no. 1, pp. 133-143, Jan. 2012.

[8] W. Li, X. Xiang, C. Li, W. Li, X. He, "Interleaved High Step-Up ZVT Converter With Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 300-313, Jan. 2013.

[9] D. Meneses, O. Garcia, P. Alou, J. A. Oliver, J. A. Cobos, "Grid-Connected Forward Microinverter With Primary-Parallel Secondary-Series Transformer," IEEE Trans. Power Electron., vol. 30, no. 9, pp. 4819-4830, Sept. 2015.

[10] B. Tamyurek, B. Kirimer "An Interleaved High-Power Flyback Inverter for Photovoltaic Applications," IEEE Trans. Power Electron., vol. 30, no. 6, pp. 3228- 3241, Jun. 2015.

[11] B. Axelrod, Y. Berkovich, Ad. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters," IEEE Trans. Circuits and Systems-I, Reg. Papers, vol. 55, no. 2, pp. 687-696, Mar. 2008.

[12] K.I. Hwu, Y.T. Yau, "High Step-Up Converter Based on Charge Pump and Boost Converter," IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2484-2494, May 2012.

[13] F.H. Dupont, C. Rech, R. Gules, J. R. Pinheiro, "Reduced-Order Model and Control Approach for the Boost Converter With a Voltage Multiplier Cell," IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3395-3404, May 2013.

[14] B. Wu, S. Li, K.M. Smedley, S. Singer, "A Family of Two-Switch Boosting Switched-Capacitor Converters," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5413-5424, Oct 2015.

[15] R. Guo, Z. Liang, A. Q. Huang, "A Family of Multimodes Charge Pump based DC–DC Converter With High Efficiency over Wide Input and Output Range," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4788- 4798, Nov. 2012.

[16] R.L. Palomo, J.A.M. Saldaña, E.P. Hernández, "Quadratic step-down dc–dc converters based on reduced redundant power processing approach," IET Power Electron., vol 6, no. 1, pp. 136-145, 2013.

[17] C.H.G. dos Santos, P.F.D. Garcia, S.I. Seleme Jr, A.P. Magalhães, "Cascaded Cell String Current Diverter for Improvement of Photovoltaic Solar Array Under Partial Shading Problems," Eletrôn. Potên., Campo Grande, v. 20, n. 3, p. 272-282, jun./ago. 2015.

[18] G.M.L. Chu, D.D.C. Lu, V.G. Agelidis, "Flyback-based high step-up converter with reduced power processing stages," IET Power Electron., vol. 5, no. 3, pp. 349-357, March 2012.

[19] M. Khalilzadeh, K. Abbaszadeh, "Non-isolated high step-up DC–DC converter based on coupled inductor with reduced voltage stress," IET Power Electron., vol. 8, no. 11, pp. 2184-2194, Nov. 2015.

[20] F. L. Tofoli, D. C. Pereira, W. Josias de Paula and D. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter," IET Power Electron., vol. 8, no. 10, pp. 2044-2057, 10 2015.
[21] T. J. Liang, J.H. Lee, S.M. Chen, J.F. Chen, L.S. Yang, "Novel Isolated High-Step-Up DC–DC Converter With Voltage Lift," IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1483-1491, April 2013.
[22] J.H. Lee, T.J. Liang, J.F. Chen, "Isolated Coupled-Inductor-Integrated DC–DC Converter With Non dissipative Snubber for Solar Energy Applications," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3337-3348, July 2014.
[23] S.M. Chen, M.L. Lao, Y.H. Hsieh, T. J. Liang, K. H. Chen, "A Novel Switched-Coupled-Inductor DC–DC Step-Up Converter and Its Derivatives," IEEE Trans. on Ind. Applications, vol. 51, no. 1, pp. 309-314, Jan.-Feb. 2015.
[24] Y.P. Hsieh, J.F. Chen, T.J. Liang, L.S. Yang, "Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 998-1007, Feb. 2012.
[25] S.M. Chen, T.J. Liang, L.S. Yang and J.F. Chen, "A Boost Converter With Capacitor Multiplier and Coupled Inductor for AC Module Applications," IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1503-1511, April 2013.
[26] T. Nouri, S.H. Hosseini, E. Babaei, J. Ebrahimi, "Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," in IET Power Electronics, vol. 8, no. 2, pp. 175-189, 2 2015.
[27] B.W. Williams, "Unified Synthesis of Tapped-Inductor DC-to-DC Converters," IEEE Trans. Power Electron., vol. 29, no. 10, pp. 5370-5383, Oct. 2014.
[28] X. Zhang, L. Jiang, J. Deng, S. Li, and Z. Chen, "Analysis and Design of a New Soft-Switching Boost Converter With a Coupled Inductor," IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4270- 4277, Aug. 2014.
[29] Y. Zhao, X. Xiang, C. Li, Yunjie Gu, W. Li, and X. He, "Single-Phase High Step-up Converter With Improved Multiplier Cell Suitable for Half-Bridge-Based PV Inverter System," IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2807- 2816, Jun. 2014.
[30] Q. Zhao, F. Tao and F. C. Lee, "A Front-end DC/DC Converter for Network Server Applications." IEEE Power Electronics Specialists Conference, pp. 1535-1539, 2001.
[31] K.C. Tseng, and T.J. Liang, "Novel high-efficiency step-up converter." IEE Proceedings of Electric Power Applications, vol. 151, no. 2, pp. 182-190, March 2004.
[32] S.J. Jang, T.W. Lee, K.S. Kang, S.S. Kim, C.Y. Won, "A New Active Clamp SEPIC-Flyback Converter for A Fuel Cell Generation System," IEEE Industrial Electronics Society Conference, pp. 2538-2542, 2005.
[33] T.B. Marchesan, M.D. Costa, J.M. Alonso, R.N. Prado, "Integrated Zeta – Flyback Converter To Supply Hid Lamps," Eletrônica de Potência, vol. 13, no. 4, Novembro de 2008.
[34] A.L. Kirsten, M.A.D. Costa, P.C.V. da Luz, R.N. Prado, T.B. Marchesan, T.H. de Oliveira, "Integração de Conversores PFC com a Topologia Bi-Flyback Inversora aplicado a Lâmpadas de descarga em Alta Pressão," Eletrôn. Potên., Campo Grande, v.18, n.1, p.864-872, dez.2012/fev. 2013 (in Portuguese).
[35] J. Yao, A. Abramovitz, K.M. Smedley, "Analysis and Design of Charge Pump-Assisted High Step-Up Tapped Inductor SEPIC Converter With an "Inductorless" Regenerative Snubber," IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5565-5580, Oct. 2015.
[36] K. Liu, F.C. Lee, "Topological constraints on basic PWM converters," IEEE Power Electronics Specialists Conference, pp. 164-172, vol. 1, 1988.
[37] J.R. Dreher, A.M.S.S. Andrade, L. Schuch, M.L.S Martins, "Extended methodology to synthesize high step-up integrated DC-DC converters", 15th European Conference on Power Electronics and Applications (EPE), pp.1-10, 2-6 Sept. 2013.

BIOGRAPHIES

Jacson Rodrigo Dreher was born in São Lourenço do Oeste in 12/02/1982. He obtained his Master's Degree in Electrical Engineering from UTFPR in 2012. Now he is a professor at the Federal Institute of Santa Catarina – IFSC. His research interests are photovoltaic generators, DC-DC converters and switched mode power supplies.

António Manuel Santos Spencer Andrade was born in Ribeira Grande, Cabo Verde, in 1989. He received his Bachelor of Science Degree in Automation and Control Engineering from the University of Caxias do Sul (UCS) in 2012. He received his M.S. degrees in electrical engineering from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 2015. Now he is a PhD degree student in Electrical Engineering Program at the in Federal University of Santa Maria (UFSM). His research interests are renewable energy and DC-DC converters.

Mr. Andrade is a member of the Brazilian Power Electronics Society (SOBRAEP) and the IEEE Society.

Luciano Schuch received the Ph.D. Degree in Electrical Engineering from UFSM (2007). He is currently Director of the Center of Technology (CT) and professor at the Postgraduate Program in Electrical Engineering (PPGEE) of UFSM. His research interests include the development of high performance converters, photovoltaic systems, distributed generation and uninterrupted power sources.

Mário Lúcio da Silva Martins was born in Palmeira das Missões, RS, Brazil, in 1976. He received his B.S., M.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 1999, 2002 and 2008, respectively.

From 2006 to 2012 he was with the Federal University of Technology – Parana, Pato Branco, Brazil. In 2012, he joined the Department of Electronics and Computer science of the Federal University of Santa Maria. His research interests include SMPS, UPS, PV inverters, and renewable energy.

Dr. Martins is a member of the Brazilian Power Electronics Society (SOBRAEP) and several IEEE Societies.