ANALYSIS AND DESIGN OF AN ACTIVE-CLAMPING COUPLED-INDUCTOR BOOST CONVERTER FOR HIGH-VOLTAGE-GAIN APPLICATIONS

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Abstract – **This paper proposes the analysis and design of an active-clamping coupled-inductor boost converter for high-voltage-gain applications. A buck-boost type active clamping circuit is employed in a configuration that enables the leakage energy to be recycled to the output. An accurate mathematical analysis considering the influence of the leakage and auxiliary inductances in the energy transfer process is carried out, providing the basis for the elaboration of a step-by-step design procedure. A detailed commutation analysis is also performed, describing the necessary conditions for soft-switching operation. The theoretical results are experimentally verified with a 260 W, 30 V input voltage, 400 V output voltage, 100 kHz, 94.38% peak efficiency prototype.**

Keywords – **Active Clamping, Coupled Inductor, High Step-up Ratio, High Voltage Gain.**

I. INTRODUCTION

Nowadays, renewable energy is a major research subject due to the necessity for energy sources as an alternative to the scarce resources of fossil fuels. However, many technological challenges arise in order to harness the energy in a proper way. This includes researches focusing on cost-effective and efficient electronic systems that enables the maximum utilization of the available energy.

In several cases, renewable energy sources are converted into electric energy at low voltage levels [1]. Some examples include photovoltaic (PV) systems for residential applications, fuel cells, and energy harvesting. However, whenever the system is connected to the electric grid, a dc-bus with a voltage level higher than the peak value of the grid voltage is generally required. Hence, a step-up dc-dc stage operating with a high conversion ratio is necessary.

The classical solution for voltage step-up in non-isolated applications is the conventional boost converter. However, it is known that in a practical implementation the boost converter suffers a serious efficiency impairment at high duty cycles levels, due to the parasitic resistances found in the circuit [2]. In order to overcome this issue, many researches reporting high-voltage-gain dc-dc converters are found in the literature. A major part of the reported high-voltage-gain circuits are based on the boost converter employing coupled inductor. This configuration enables the circuit to achieve high conversion ratios in a simple and effective way [3]. The application of active clamping to the coupled inductor boost converter was detailed in [4]. High-step-up converters obtained employing multiplier cells have been reported in [5]-[8], allowing the operation with increased voltage gain but with reduced duty cycle values. In [9], the integration of conventional boost converters to generate a high-voltage-gain topology requiring simple control has been proposed. Low input voltage application requiring a step-up converter often demand high input current resulting in increased stresses. In order to overcome this issue, some proposed circuits provide current distribution to alleviate the current stresses [10]-[12]. In [2] and [13], the concepts of switched capacitor and/or inductor have been used to generate topologies exhibiting high voltage gain. Soft-switching solutions have been also reported, featuring reduced switching losses thus allowing the operation at a higher switching frequency [14], [15]. The integration of the boost converter with the flyback [2], forward [16] and SEPIC [17] is also found in the literature as potential solutions for high-step-up ratio converters.

In this paper, the analysis and design of the coupled-inductor boost converter employing active clamping for leakage energy recycling and soft-switching operation are detailed. The active clamping is referred to as buck-boost given that the clamping voltage can be either lower or higher than the input voltage. An alternative buck-boost active clamping circuit applied to the coupled inductor boost converter was published in [4], along with a simplified static analysis (disregarding the influence of the leakage and external inductances on the static gain), where the leakage energy was recycled to the input. In this paper, the circuit proposed for performing the active clamping recycles the leakage energy to the output. An accurate mathematical analysis quantifying the influence of the leakage and auxiliary inductances on the energy transfer process is also detailed, in a way that a step-by-step design methodology can be elaborated for the adequate circuit design. Finally, the commutation process of the active-clamping coupled-inductor boost (ACCIB) converter is analyzed in details, describing the necessary conditions for guaranteeing soft-switching operation.

II. PRINCIPLE OF OPERATION IN STEADY STATE

In this section, the qualitative analysis of the ACCIB converter in steady state is performed, introducing the key theoretical waveforms for continuous conduction mode (CCM) operation.

The power stage of the ACCIB converter is depicted in Figure 1. The active clamping if performed by S_2 and C_c. The inductance L_c models the equivalent stray and leakage

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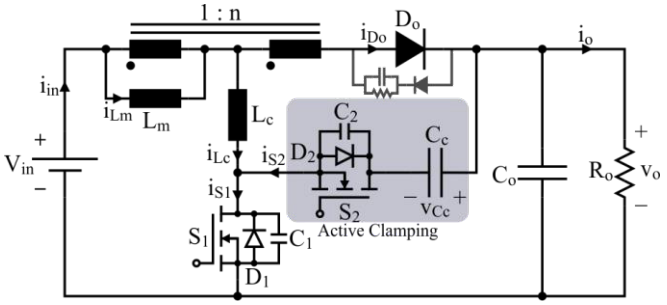

Fig. 1. Power stage of the ACCIB converter.

inductances and also the auxiliary inductor added to guarantee ZVS for a desired output power range.

A. Operating Stages Description

The operation of the ACCIB converter can be divided into seven operating stages, described as follows:

Stage 1 ($t_0 - t_1$): at $t = t_0$, D_1 becomes forward biased and the first stage starts. Switch S_1 must be turned on during this stage in order to guarantee ZVS for this element. Eventually, the current i_{Lc} reaches zero and this stage ends.

Stage 2 ($t_1 - t_2$): as i_{Lc} becomes null and has its direction reversed, it starts flowing through S_1, which was turned on during the previous stage. At $t = t_2$, i_{Lc} and i_{Lm} become equivalent, and thus diode D_o is blocked. This event characterizes the end of the second operating stage.

Stage 3 ($t_2 - t_3$): the third stage corresponds to the series connection between L_m and L_c, and energy is transferred from V_{in} to these inductances. As soon as S_1 is turned off, this stage is over.

Stage 4 ($t_3 - t_4$): the blocking of S_1 implies that i_{Lc} is redirected to C_1 and C_2, charging and discharging these capacitances, respectively. This interval corresponds to a commutation stage, which is usually brief when compared to the conventional energy transferring stages. A $t = t_4$, C_2 is completely discharged diode D_2 becomes forward biased.

Stage 5 ($t_4 - t_5$): after the commutation process is completed, D_2 provides the current path for i_{Lc}, thereby providing voltage clamping for S_1. It is noteworthy that S_2 must be turned on during this stage in order to guarantee ZVS for this switch. The fifth stage is finished when i_{Lc} becomes null.

Stage 6 ($t_5 - t_6$): at $t = t_5$, i_{Lc} reaches zero and has its direction once again reversed. Therefore, it starts flowing through S_2, which was previously turned on. Eventually, S_2 is turned off and the sixth stage ends.

Stage 7 ($t_6 - t_7$): the turn-off of S_2 redirects i_{Lc} to C_1 and C_2, discharging and charging them, respectively. Similarly to the fourth stage, a commutation process takes place during the interval $t_6 - t_7$. After C_1 is fully discharged, this stage is over and a switching period is completed.

The circuit configuration for every operating stage in steady state is shown in Figure 2.

B. Main Theoretical Waveforms

The key theoretical waveforms regarding the operation of the ACCIB converter in CCM are depicted in Figure 3.

III. MATHEMATICAL ANALYSIS

The mathematical description of the ACCIB converter CCM operation in steady state is presented in this section, the results of which are fundamental for the adequate circuit design.

Following are detailed some assumptions regarding the conditions under which the mathematical analysis is carried out:

- All converter elements are treated as ideal, except the coupled inductor (its leakage inductance influence can be considered in the L_c inductance value);
- It is assumed that the voltages on capacitors C_c and C_o are ripple free, although these ripple values can be quantified for designing purposes after the steady-state set of equations is solved. It is also assumed that $C_1 = C_2 = C_s$.

A. Definitions

In order to have a generic representation of the steady state behavior of the ACCIB converter, the definitions of the static gain (q) and inductance factor (λ) are made as follows:

$$q \triangleq \frac{V_o}{V_{in}}; \quad \lambda \triangleq \frac{L_c}{L_m}. \tag{1}$$

Every parameter related to a current value in the analysis is written in its normalized form, according to the rule

$$\overline{I}_x \triangleq \frac{2 f_s L_c I_x}{V_{in}} \tag{2}$$

where f_s is the switching frequency.

Similarly, the normalization of a given voltage parameter obeys the relation

$$\overline{V}_x \triangleq \frac{V_x}{V_{in}}. \tag{3}$$

Finally, the time intervals are expressed in the time base of one switching period T_s, as given by

$$\overline{\Delta t}_k \triangleq \frac{\Delta t_k}{T_s} = \frac{t_k - t_{k-1}}{T_s}. \tag{4}$$

B. Steady State Analysis

In steady state, the mathematical analysis of the equivalent circuit of every operating stage yields the following equations:

$$I_1 - I_2 - \frac{(V_o - V_{in})}{(1+n)L_m}\Delta t_1 = 0 \tag{5}$$

$$I_6 - \frac{(nV_{in} + V_o)}{(1+n)L_c}\Delta t_1 = 0 \tag{6}$$

$$I_2 - I_3 - \frac{(V_o - V_{in})}{(1+n)L_m}\Delta t_2 = 0 \tag{7}$$

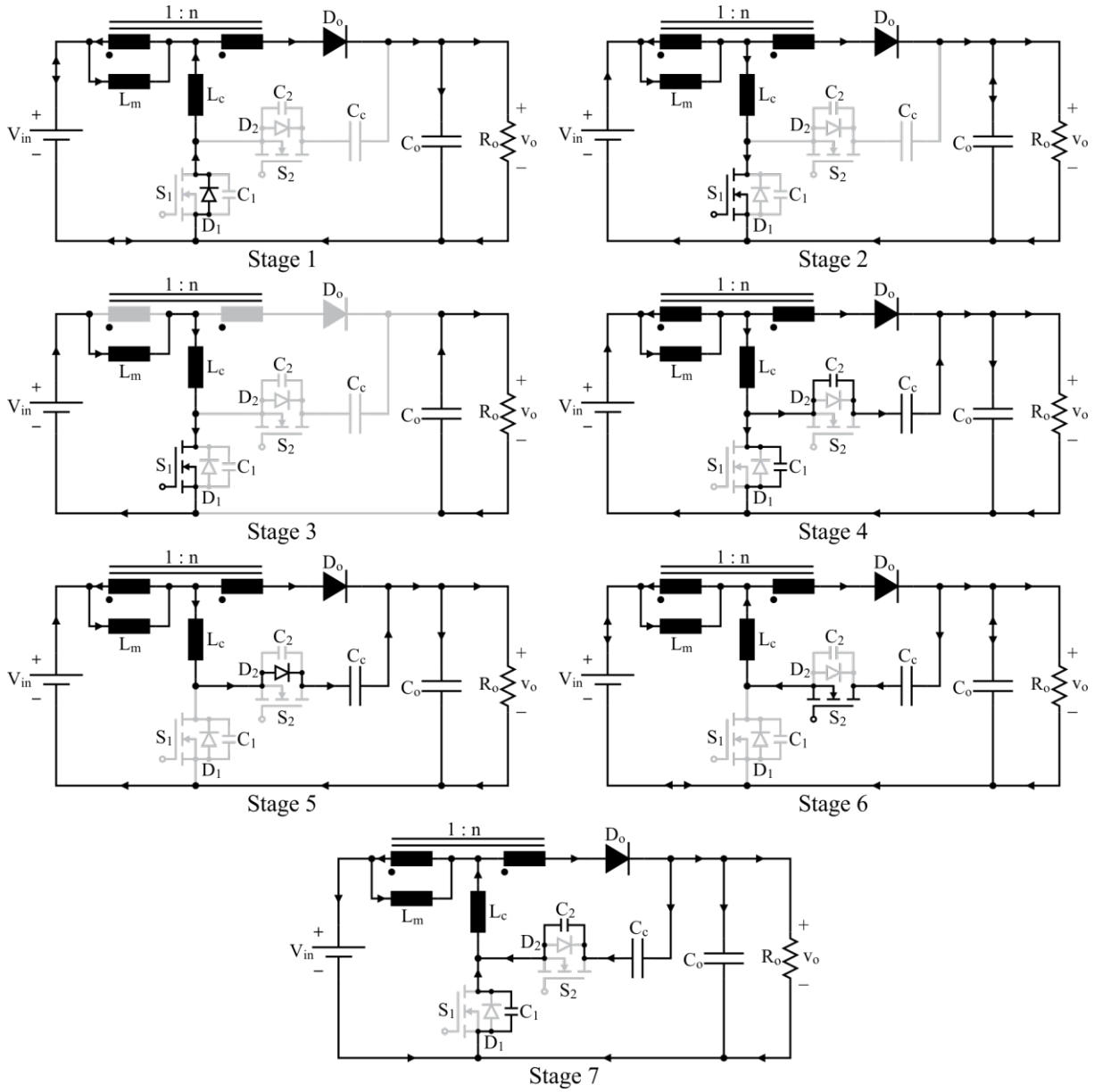

Fig. 2. Operating stages of the ACCIB converter in steady state.

$$I_3 - \frac{(nV_{in} + V_o)}{(1+n)L_c}\Delta t_2 = 0 \tag{8}$$

$$I_4 - I_3 - \frac{V_{in}}{L_c + L_m}\Delta t_3 = 0 \tag{9}$$

$$I_4 - I_5 - \frac{(V_o - V_{in})}{(1+n)L_m}\Delta t_5 = 0 \tag{10}$$

$$I_4 - \left[\frac{n(V_o - V_{in})}{(1+n)L_c} - \frac{V_{Cc}}{L_c}\right]\Delta t_5 = 0 \tag{11}$$

$$I_5 - I_1 - \frac{(V_o - V_{in})}{(1+n)L_m}\Delta t_6 = 0 \tag{12}$$

$$I_6 - \left[\frac{n(V_o - V_{in})}{(1+n)L_c} - \frac{V_{Cc}}{L_c}\right]\Delta t_6 = 0 \tag{13}$$

where n is the number of turns ratio.

As depicted in Figure 3, the duty cycle can be related to the durations of the operating stages as given by

$$\Delta t_1 + \Delta t_2 + \Delta t_3 = \frac{D}{f_s} \tag{14}$$

$$\Delta t_5 + \Delta t_6 = \frac{(1-D)}{f_s}. \tag{15}$$

Finally, the last equation is derived from the charge balance in the clamping capacitor C_c, which implies that the average value of i_{Cc} must be equal to zero in steady state. The current through C_c is equivalent to i_{Lc} during stages 4 and 5 and zero during all the other stages. Thus, based on the waveforms depicted in Figure 3, it is possible to conclude that

$$I_4 - I_6 = 0 \tag{16}$$

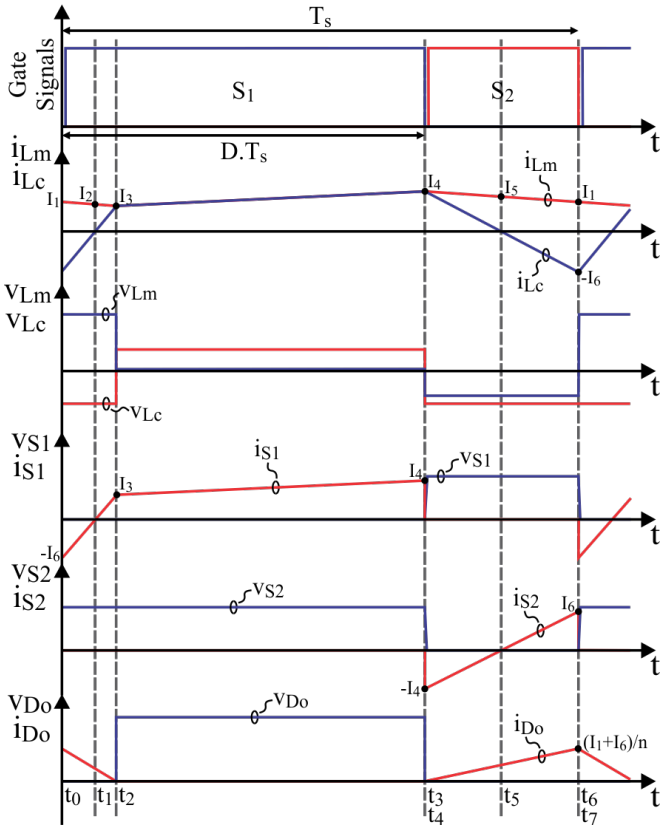

Fig. 3. Key theoretical waveforms of the ACCIB converter operation in steady state.

must hold true, so that the average value of i_{Cc} is equal to zero.

On solving the system of equations composed of (5)–(15) and using the definitions (1)–(4), one can determine the normalized values of the auxiliary parameters V_{Cc}, I_1, I_2, I_3, I_4, I_5, I_6, Δt_1, Δt_2, Δt_3, Δt_5 and Δt_6, as follows:

$$\bar{V}_{Cc} = \frac{(q - Dq - 1)}{(1 - D)} \tag{17}$$

$$\bar{I}_1 = \frac{(2\lambda - q - 2\lambda q + 1 + 2D\lambda q + Dq - 2D\lambda + nD)}{(1+n)} \tag{18}$$

$$\bar{I}_2 = \frac{\left(\lambda - q^2 - \lambda q^2 + D\lambda q^2 + Dq^2 + 2n\lambda + q - D\lambda q\right)}{(1+n)(q+n)} + \frac{\left(n + Dn^2 - 2n\lambda q - nq - nD\lambda + nD\lambda q + 2nDq\right)}{(1+n)(q+n)} \tag{19}$$

$$\bar{I}_3 = \frac{\left(\lambda - q^2 - \lambda q^2 + D\lambda q^2 + Dq^2 + 2n\lambda + q - D\lambda q\right)}{(1+n)(\lambda q + q - \lambda + n)} + \frac{\left(n + Dn^2 - 2n\lambda q - nq - nD\lambda + nD\lambda q + 2nDq\right)}{(1+n)(\lambda q + q - \lambda + n)} \tag{20}$$

$$\bar{I}_4 = \frac{(1 - q + Dq + nD)}{(1+n)} \tag{21}$$

$$\bar{I}_5 = \frac{(\lambda - q - \lambda q + 1 + D\lambda q + Dq - D\lambda + nD)}{(1+n)} \tag{22}$$

$$\bar{I}_6 = \frac{(1 + Dq + nD - q)}{(1+n)} \tag{23}$$

$$\bar{\Delta t}_1 = \frac{(1 - q + Dq + nD)}{2(q+n)} \tag{24}$$

$$\bar{\Delta t}_2 = \frac{\left(\lambda - q^2 - \lambda q^2 + D\lambda q^2 + Dq^2 + 2n\lambda + q - D\lambda q\right)}{2(1+n)(\lambda q + q - \lambda + n)} + \frac{\left(n + Dn^2 - 2n\lambda q - nq - nD\lambda + nD\lambda q + 2nDq\right)}{2(1+n)(\lambda q + q - \lambda + n)} \tag{25}$$

$$\bar{\Delta t}_3 = \frac{(q-1)(1+\lambda)}{(\lambda q + q - \lambda + n)} \tag{26}$$

$$\bar{\Delta t}_5 = \frac{(1-D)}{2} \tag{27}$$

$$\bar{\Delta t}_6 = \frac{(1-D)}{2}. \tag{28}$$

The set of equations (17)–(28) allows determining the values of voltages and currents on every element of the converter, being this a key information for the adequate converter design. Equation (17) demonstrates that the clamping voltage V_{Cc} can be lower or higher than V_{in}, thus characterizing the active clamping circuit as buck-boost.

C. Output Characteristic

From the steady state analysis results one can determine the output current average value, which is given by

$$\bar{I}_o = \frac{1}{(n - \lambda + q + \lambda q)} - \frac{(1-D)}{(1+n)} \tag{29}$$

in its normalized form. Equation (29) corresponds to the output characteristic of the ACCIB converter and provides fundamental information regarding the converter behavior when observed from its output terminals. Figure 4 depicts the curves drawn from (29) considering n =1 and λ = 0.01 for several values of duty cycle, along with the simplified analysis results (disregarding the influence of L_c). It is evident that neglecting L_c leads to a considerable inaccuracy when computing the static gain as the duty cycle is increased. The DCM region in the graph corresponds to the operation in the discontinuous conduction mode, which is not discussed in this paper. The forbidden region refers to the area where the static gain values are lower than one, which does not occur due to the boost nature of the ACCIB converter.

D. Magnetizing Current

As detailed in the operating principle of the ACCIB converter, the magnetizing inductance plays an important role on the energy transfer process. In order to ensure the adequate converter operation, the coupled inductor must be properly designed, which requires computing some key values of the magnetizing current. One of the most important is its average value, given by

$$\bar{I}_{Lm} = \frac{(n+q)(\lambda - q - D\lambda + Dn + Dq - \lambda q + D\lambda q + 1)}{(1+n)(n - \lambda + q + \lambda q)}. \tag{30}$$

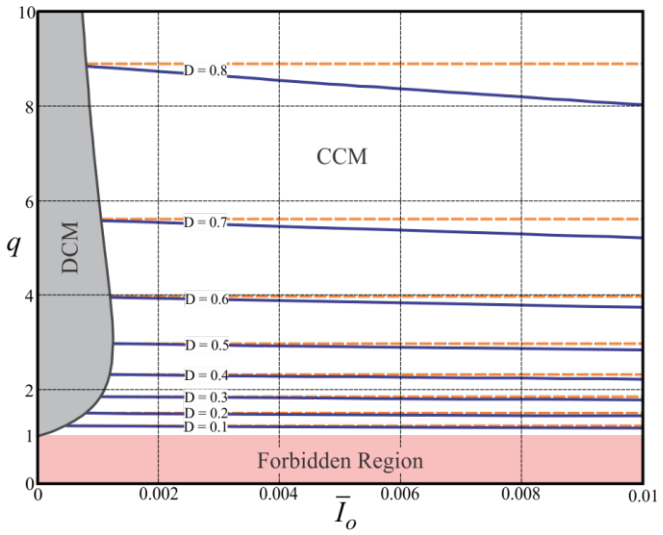

Fig. 4. Output characteristic of the ACCIB converter considering n =1 and λ = 0.01: ideal (considering L_c = 0) (dashed lines); non-ideal (continuous lines).

The coupled inductor core loss can be estimated by the magnetic flux density ripple, which can be computed from the magnetizing current ripple given by

$$\Delta I_{Lm\%} = \frac{2\lambda(q-1)(1+n)}{(n+q)(\lambda - q - D\lambda + Dn + Dq - \lambda q + D\lambda q + 1)}. \quad (31)$$

Finally, the maximum value of the magnetizing current is

$$\bar{I}_{Lm,max} = \bar{I}_4 = \frac{(1-q+Dq+nD)}{(1+n)}. \quad (32)$$

Equations (30)–(32) provide fundamental information on the magnetizing current behavior, necessary for adequately designing the coupled inductor used in the ACCIB converter.

E. Voltage Ripple on Capacitor C_c

In order to determine the value of the clamping capacitor C_c during the ACCIB converter design, the voltage ripple on this component must be computed. On observing the power stage of the converter, it can be verified that the current through this capacitor is equivalent to the current through S_2. Therefore, on analyzing the waveform of i_{S2} provided in Figure 3, one can evaluate the voltage ripple on C_c as

$$\Delta V_{Cc\%} \triangleq \frac{\Delta V_{Cc}}{V_{Cc}} = \frac{(1-D)^2(nD-q+qD+1)}{8f_s^2 L_c C_c (1+n)(q-qD-1)}. \quad (33)$$

F. Output Voltage Ripple

Since the output current of the ACCIB converter is pulsating, the capacitor C_o is placed at the output terminals to ensure that the output voltage ripple is limited to a specified value. Therefore, it is important to understand how the output voltage ripple is affected by the converter parameters and operating conditions. From the converter analysis, it is possible to demonstrate the validity of

$$\Delta V_{o\%} \triangleq \frac{\Delta V_o}{V_o} = \frac{(I_4 - I_0)^2(\Delta t_5 + \Delta t_6)}{2C_o\left[I_4 + I_6 - \frac{(I_1+I_6)}{(1+n)}\right]}. \quad (34)$$

Equation (34) could be written in terms of the converter parameters, but the result is too long and is not provided in the paper.

It is also noteworthy that the result (34) has been computed considering that the current provided to the load (R_o in this paper) is ripple free. In the case where the load also drains a pulsating current, e.g., grid-connected inverter, the resulting output voltage ripple depends on both ACCIB converter and load characteristics, so that computing this parameter may vary from application to application.

G. Commutation Analysis

In order to guarantee ZVS for both S_1 and S_2 the value of L_c must be properly chosen and a minimum dead time between the gate signals must be respected, otherwise the switching occurs with a nonzero voltage. The commutation takes place in stages 4 and 7, disregarded during the static analysis since the energy processed to the output is negligible. However, a closer look into these stages is taken in this section, aiming to describe the switching conditions of the ACCIB converter.

From the analysis of the circuit during stage 4, it is possible to demonstrate that the interval Δt_4 is given by

$$\Delta t_4 = \frac{2C_s(n+q)V_{in}}{(1+n)I_4} + \sqrt{8L_cC_s}\,tg^{-1}\left(\frac{\sqrt{K_1^2 - K_2^2} - K_1}{K_2}\right) \quad (35)$$

where:

$$K_1 = \sqrt{\frac{L_c}{2C_s}}\frac{I_4}{V_{in}}; \quad K_2 = \bar{V}_{Cc} - \frac{n(q-1)}{(1+n)}. \quad (36)$$

The result (35) is written in terms of the auxiliary parameter I_4, which can be computed using (21).

Another important result is the interval of values of L_c that ensures the complete discharge of C_2, and consequently the forward biasing of D_2. Such interval can be computed as

$$L_c > \frac{2C_s\left[\bar{V}_{Cc} - \frac{n(q-1)}{(1+n)}\right]^2 V_{in}^2}{I_4^2}. \quad (37)$$

Regarding stage 7, its duration Δt_7 is

$$\Delta t_7 = \sqrt{8L_cC_s}\,tg^{-1}\left(\frac{K_3 - \sqrt{K_3^2 - (q-\bar{V}_{Cc})K_4}}{K_4}\right) \quad (38)$$

where:

$$K_3 = \sqrt{\frac{L_c}{2C_s}}\frac{I_6}{V_{in}}; \quad K_4 = \frac{q + \bar{V}_{Cc} - (q - \bar{V}_{Cc} - 2)n}{(1+n)}. \quad (39)$$

Expression (38) is written in terms of the auxiliary parameter I_6 given in (23).

Finally, C_1 is completely discharged during stage 7 if and only if

$$L_c > \frac{2C_s\left(q-\bar{V}_{Cc}\right)\left[q+\bar{V}_{Cc}-\left(q-\bar{V}_{Cc}-2\right)n\right]V_{in}^2}{\left(1+n\right)I_6^2}. \quad (40)$$

Gathering the results of the previous analysis, a minimum value of L_c can be determined using (37) and (40) for a given range of output power. Finally, the dead time is chosen to ensure that the intervals (35) and (38) are completely elapsed prior to the turn-on event of each switch.

IV. DESIGN PROCEDURE

In this section, the several theoretical results are used to elaborate a step-by-step design methodology for the ACCIB converter.

A. Proposed Step-by-Step Design Methodology

The following steps are proposed for the ACCIB converter design:

1) Define a maximum duty cycle value in the range of 0.5 to 0.75 and estimate an equivalent stray inductance (usually units of micro-Henrys);
2) Determine the static gain with (1);
3) Calculate the maximum output current by the ratio between the maximum output power and output voltage average value;
4) Compute the normalized output current using (2);
5) The clamping voltage V_{Cc} can be calculated with (17);
6) On solving the system of equations composed of (29) and (31), it is possible to determine the values of n and λ;
7) Compute the magnetizing inductance L_m using the definition (1) and the value of λ calculated in the previous step;
8) Specify a maximum voltage ripple on capacitor C_c and calculate its capacitance using (33);
9) Determine C_o with (34) in order to meet the specified output voltage ripple;
10) Estimate the output power range where ZVS is achieved using (37) and (40), with I_4 and I_6 computed for the minimum output power. If the result is not satisfactory, update the value of the external inductance and go back to step 1. However, if the ZVS range meets the specifications, define an adequate dead time in accordance with (35) and (38).

From the converter parameters obtained in the previous steps one can evaluate the voltage and current stresses in every converter element, and thus properly choose them. Subsequently, one could perform theoretical estimations on the converter efficiency and size to verify if the design satisfies the desired specifications.

Observe that the previous steps could be used iteratively in an optimization process. In such case, based on a cost function (e.g., function of efficiency and size) the maximum duty cycle could be redefined in the optimization algorithm to determine the best converter parameter set that meets the desired specifications with a minimum cost function value. However, it is beyond the scope of this paper dealing with any optimization procedure.

B. Design of a 260 W ACCIB Converter Prototype

In order to verify the theoretical analyses detailed in the paper, a 260 W ACCIB converter prototype was designed according to the specifications provided in Table I. The main resulting parameters obtained from the steps proposed in this section are provided in Table II.

Using the results from the commutation analysis, a soft-switching range of 30–100% of output rated power is estimated. A dead time of 200 ns is chosen to ensure that the voltage transitions are completed before the turn-on signals of S_1 and S_2 are applied.

A picture of the built prototype is shown in Figure 5.

V. EXPERIMENTAL RESULTS

The theoretical analysis has been validated in laboratory by testing the 260 W ACCIB converter prototype and the

TABLE I
Design Specifications of the 260 W ACCIB Converter Prototype

Parameter	Value
Output Power (P_o)	260 W
Input Voltage (V_{in})	30 V
Output Voltage (V_o)	400 V
Switching Frequency (f_s)	100 kHz
Magnetizing Current Ripple ($\Delta I_{Lm\%}$)	< 35%
Clamping Voltage Ripple ($\Delta V_{Cc\%}$)	< 5%
Output Voltage Ripple ($\Delta V_{o\%}$)	< 1%

TABLE II
Main Parameters of the 260 W ACCIB Converter Prototype

Parameter	Value
L_m	46.9 µH
L_c	2.5 µH
D	0.75
n	4.963
q	13.33
V_{Cc}	280 V
C_o	2.35 µF
C_c	1 µF
S_1 and S_2	IRFP4668PBF
D_o	C4D05120A

Fig. 5. Picture of the 260 W prototype built for the experimental tests.

main results are presented in this section.

Output voltage and output current waveforms, taken at nominal operating conditions, are shown in Figure 6. The average values of 399.9 V and 658 mA have been measured, thus demonstrating the operation at approximately 260 W. Figure 7 depicts the input voltage and current waveforms, where their respective average values are 30.31 V and 9.69 A.

As discussed in the paper, one important feature of the ACCIB converter is its capability of ZVS operation. In order to verify the occurrence of ZVS the drain-to-source and gate-to-source measured waveforms for S_1 and S_2 are depicted in Figures 8 and 9, respectively. For a better visualization of the switching characteristics, details on the turn-on process of S_1 and S_2 are also provided. Soft switching is guaranteed for both S_1 and S_2 within the range of 30–100% of output rated power, thus in accordance with the design procedure carried out.

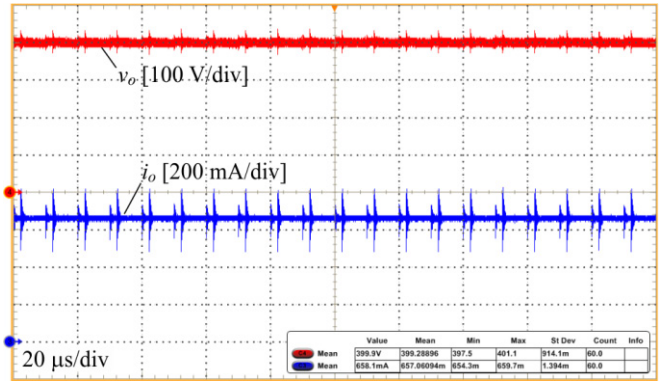

Fig. 6. Output voltage v_o [100 V/div] and output current i_o [200 mA/div].

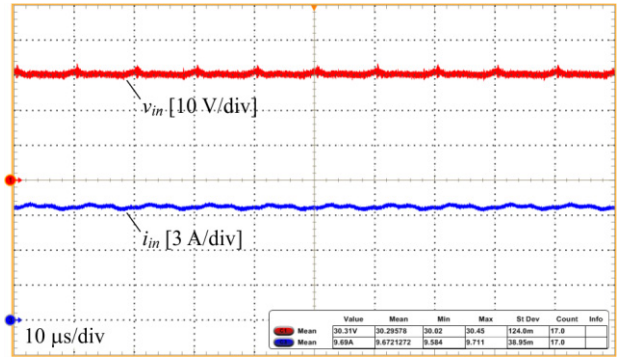

Fig. 7. Input voltage v_{in} [10 V/div] and input current i_{in} [3 A/div].

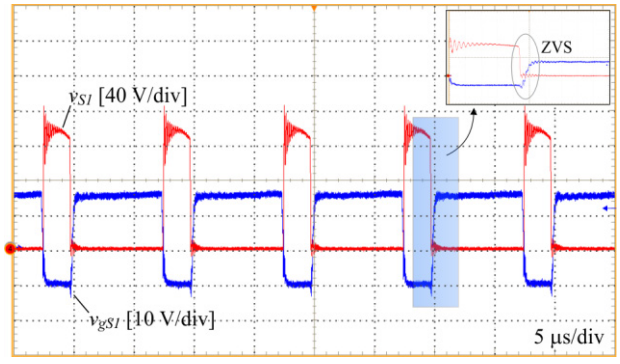

Fig. 8. Drain-to-source voltage v_{S1} [40 V/div] and gate voltage v_{gS1} [10 V/div] on switch S_1.

In addition to providing ZVS capability to the coupled inductor boost converter, the active clamping also enables recovering most of the energy stored in the leakage inductance of the coupled inductor. In this paper, the active clamping has been realized aiming to divert the leakage energy to the output filter of the converter. Figure 10 depicts the voltage waveform on the clamping capacitor C_c, where an average value of 272.9 V was measured, which is in a good agreement with the theoretical prediction of 280 V.

Since diode D_o is in series with one winding of the coupled inductor, ringing due to resonance between its junction capacitance with the winding leakage inductance is expected in a practical implementation. It is noteworthy that such resonance has not been considered in the theoretical analysis as it has a negligible influence on the energy transfer process of the ACCIB converter. In order to keep the reverse voltage of D_o limited into its safe operating region, an auxiliary RCD (resistor-capacitor-diode) dissipative clamping circuit has been included in the prototype, as depicted in Figure 1. The dissipative clamping circuit was realized with a resistance of 380 kΩ, capacitance of 5.6 nF and the diode MUR1100 (values set empirically). The waveform of the reverse voltage on D_o is provided in Figure 11, where it can be observed a clamping level of 812.8 V.

Finally, several efficiency measurements are provided in Figure 12 and the loss distribution in the 260 W ACCIB converter prototype is shown in Figure 13. A maximum efficiency of 94.38% is observed at 50% of the rated output power. At nominal conditions, the measured efficiency is 93.40%.

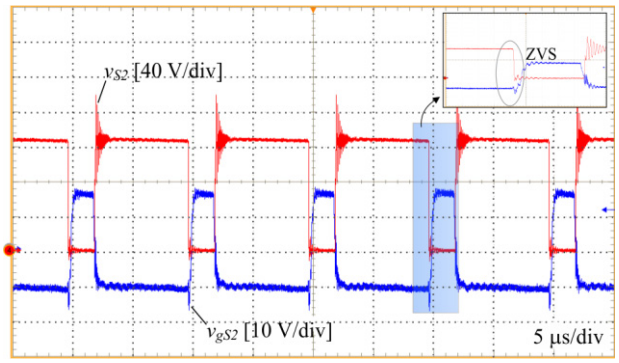

Fig. 9. Drain-to-source voltage v_{S2} [40 V/div] and gate voltage v_{gS2} [10 V/div] on switch S_2.

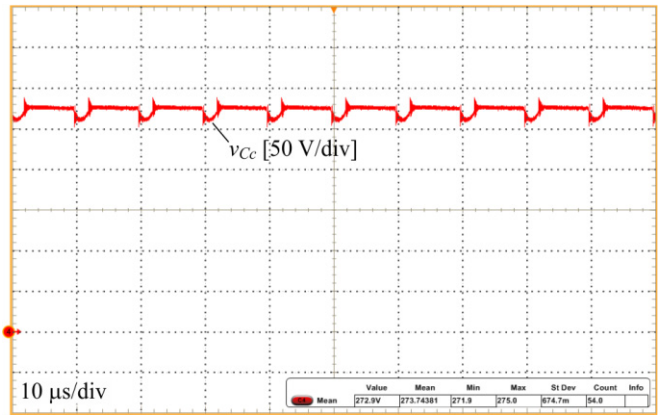

Fig. 10. Clamping voltage v_{Cc} [50 V/div].

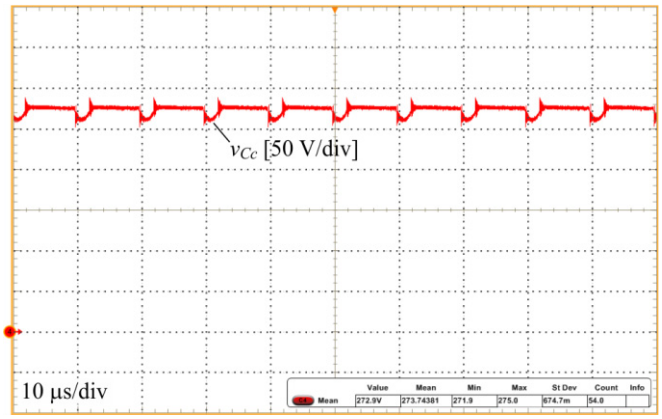

Fig. 10. Clamping voltage v_{Cc} [50 V/div].

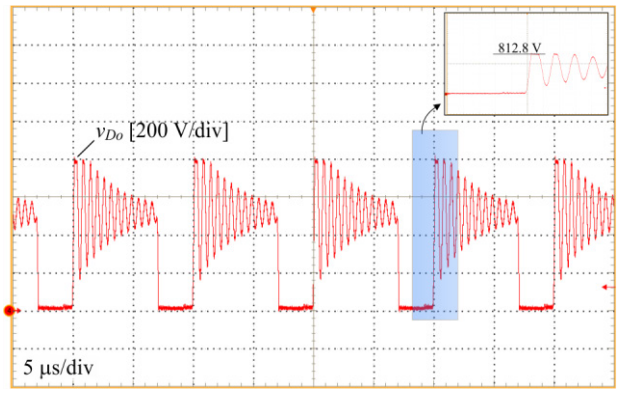

Fig. 11. Reverse voltage on diode D_o v_{Do} [200 V/div].

VI. CONCLUSIONS

In this paper, the mathematical analysis and design of an active-clamping coupled-inductor boost converter were detailed. In the proposed analysis, the influence of the leakage and external inductances on the energy transfer process was taken into consideration, and thus an accurate description of the converter operation was achieved.

The employment of the coupled-inductor allowed the circuit to operate with a high voltage gain while maintaining the duty cycle at low levels. In order to prevent voltage spikes to occur on the boost switch (and consequently additional losses), an extra switch and capacitor were added to the circuit in order to implement the active clamping. This way, zero-voltage-switching was achieved on both converter's switches, thus contributing to improving the circuit efficiency.

A comparison between the proposed ACCIB converter and the solution reported in [4] demonstrates that both circuits exhibit a similar ideal static gain and equivalent number of components (disregarding the passive clamping for D_o). However, in this paper the active clamping is set to recycle the energy stores in the leakage and external inductances to the output stage. Moreover, in [4] only a simplified static analysis is reported, while this paper provides an accurate model predicting the non ideal static gain and also the switching conditions of the ACCIB converter.

Experimental results validated the theoretical analysis carried out and demonstrated the feasibility of the converter. Efficiency measurements with a voltage step-up ratio of

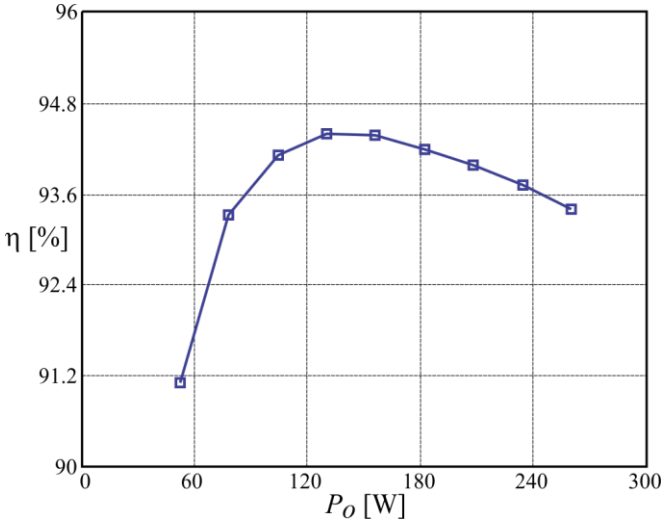

Fig. 12. Measured efficiency for several output power conditions.

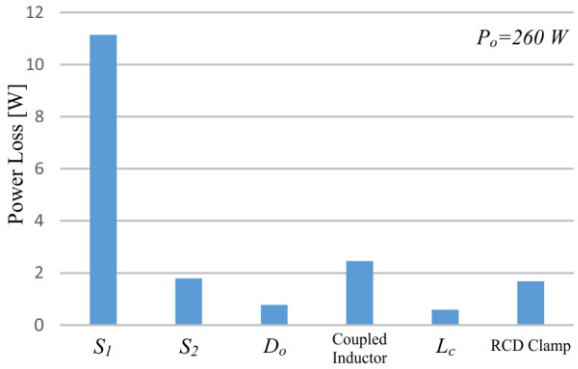

Fig. 13. Loss distribution in the 260 W ACCIB converter prototype at P_o = 260 W.

13.33 indicated a maximum efficiency of 94.38% at 50% of the rated output power. At nominal conditions, the circuit exhibited an efficiency of 93.40%. These results are considered adequate for a converter operating with a voltage gain of 13.33, switching frequency of 100 kHz and a design carried out without any optimization procedure. Therefore, the ACCIB converter demonstrated an interesting potential for high-voltage-gain applications requiring good efficiency levels and a relatively simple circuit.

REFERENCES

[1] B. Gu, J. Dominic, J. S. Lai, Z. Zhao, C. Liu, "High Boost Ratio Hybrid Transformer DC–DC Converter for Photovoltaic Module Applications", *IEEE Transactions on Power Electronics*, vol. 28, nº 4, pp. 2048-2058, April 2013.

[2] K. C. Tseng, T. J. Liang, "Novel high-efficiency step-up converter," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 182-190, Mar. 2004.

[3] H. Liu, H. Hu, H. Wu, Y. Xing, I. Batarseh, "Overview of High-Step-Up Coupled-Inductor Boost Converters", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, nº 2, pp. 689-704, June 2016.

[4] T. F. Wu, Y. S. Lai, J. C. Hung, Y. M. Chen, "An improved boost converter with coupled inductors and

buck-boost type of active clamp," *in Fortieth IAS Annual Meeting*, vol. 1, pp. 639-644, 2005.
[5] K. C. Tseng, C. C. Huang, W. Y. Shih, "A High Step-Up Converter With a Voltage Multiplier Module for a Photovoltaic System", *IEEE Transactions on Power Electronics*, vol. 28, nº 6, pp. 3047-3057, June 2013.
[6] B. Axelrod, Y. Beck, Y. Berkovich, "High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: steady state and dynamics", *IET Power Electronics*, vol. 8, nº 8, pp. 1420-1428, Aug. 2015.
[7] X. Hu, C. Gong, "A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques", *IEEE Transactions on Power Electronics*, vol. 29, nº 2, pp. 789-800, Feb. 2014.
[8] A. M. S. S. Andrade, E. Mattos, H. L. Hey, L. Schuch, M. L. S. Martins, "Conversor Boost-Flyback com Células Multiplicadoras de Tensão para Aplicação em Fontes Alternativas", *Eletrônica de Potência*, vol. 22, nº 2, pp. 122-130, abr./jun. 2017.
[9] R. G. d. A. Cacau, T. B. Lazzarin, M. C. T. Villanueva, I. Barbi, "A high step-up non-isolated DC-DC converter based on the integration of conventional boost converters", *in 2016 IEEE 25th International Symposium on Industrial Electronics (ISIE)*, pp. 408-420, 2016.
[10] S. L. Brockveld, G. Waltrich, "Conversor CC-CC de Alto Ganho com Divisão de Esforços de Corrente no Estágio De Estrada", *Eletrônica de Potência*, vol. 22, nº 4, pp. 380-388, out./dez. 2017.
[11] V. F. Gruner, L. Schmitz, D. C. Martins, R. F. Coelho, "Conversor CC-CC de Alto Ganho com Compartilhamento da Corrente de Entrada, Modulação Phase-Shift e Compactação do Filtro De Saída", *Eletrônica de Potência*, vol. 23, nº 2, pp. 141-150, abr./jun. 2018.
[12] K. C. Tseng, C. A. Cheng, C. T. Chen, "High Step-Up Interleaved Boost Converter for Distributed Generation Using Renewable and Alternative Power Sources", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, nº 2, pp. 713-722, June 2017.
[13] M. A. Salvador, T. P. Horn, T. B. Lazzarin, R. F. Coelho, "Conversor CC-CC de Alto Ganho Obtido pela Combinação entre Redes de Indutor e de Capacitor Chaveados", *Eletrônica de Potência*, vol. 23, nº 2, pp. 161-170, abr./jun. 2018.
[14] X. Zhang, L. Jiang, J. Deng, S. Li, Z. Chen, "Analysis and Design of a New Soft-Switching Boost Converter With a Coupled Inductor", *IEEE Transactions on Power Electronics*, vol. 29, nº 8, pp. 4270-4277, Aug. 2014.
[15] S. Sathyan, H. M. Suryawanshi, B. Singh, C. Chakraborty, V. Verma, M. S. Ballal, "ZVS–ZCS High Voltage Gain Integrated Boost Converter for DC Microgrid", *IEEE Transactions on Industrial Electronics*, vol. 63, nº 11, pp. 6898-6908, Nov. 2016.
[16] J. C. Giacomini, P. F. S. Costa, A. M. S. S. Andrade, L. Schuch, M. L. S. Martins, "Desenvolvimento de um Conversor CC-CC Boost-Forward Integrado para Aplicações com Elevado Ganho de Tensão", *Eletrônica de Potência*, vol. 22, nº 2, pp. 206-214, abr./jun. 2017.
[17] S. W. Lee, H. L. Do, "Zero-Ripple Input-Current High-Step-Up Boost–SEPIC DC–DC Converter With Reduced Switch-Voltage Stress", *IEEE Transactions on Power Electronics*, vol. 32, nº 8, pp. 6170-6177, Aug. 2017.

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