TRANSFORMERLESS STEP-UP INVERTER BASED ON SWITCHED-CAPACITOR CONVERTER TECHNOLOGY

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Abstract – **In this paper the integration between a voltage source inverter (VSI) and a switched capacitor converter (SCC) is proposed to generate a sinusoidal waveform with a double peak voltage value at the converter output terminal, without the use of a transformer or a dc-dc boost converter. The novel structure (VSI-SCC) is designed as a transformerless step-up inverter with linear gain. VSI and SCC models are individually characterized to integrate both structures in only one model. To validate the theoretical analysis a prototype was designed for a power of 1 kW, considering a dc input voltage of 200 V and an ac output voltage of 220 V (rms). In this prototype the VSI converter supplies 110 V (rms) to the SCC converter, and this converter step-up it to 220 V (rms). Furthermore, open and closed-loop control were also tested in the prototype reaching a maximum efficiency of 90%.**

Keywords – **Linear Gain, Step-up Inverter, Switched-Capacitor, Transformerless.**

I. INTRODUCTION

In recent years voltage source inverters (VSIs) have been used in a wide range of applications associated with, for instance, renewable energy sources, distributed generation systems, uninterruptible power supply (UPS), electric and hybrid vehicles and smart-grids [1]–[4]. In the majority of cases VSI topologies are employed as step-down inverters (half-bridge, full-bridge, etc.), mainly due to their simple control system and linear gain characteristics.

On the other hand, step-up inverters [5]–[12] present non-linear gain characteristic, such as Z-source [8]–[11] and SEPIC [12] inverters. These structures increase the control system complexity and make it difficult to obtain a sinusoidal waveform at the converter output. Other way to obtain a step-up structure is using a two-stage boost-buck inverter, which employs a dc-dc converter to increase the dc voltage and a conventional inverter to supply the ac voltage. This solution introduces higher voltage stress on the semiconductors.

The simplest solution to boost the VSI output voltage is the use of a low-frequency transformer, which is the technique most commonly employed in industry, due to its simplicity and robustness. However, low-frequency transformers require large cores, resulting in heavy and bulky magnetic components.

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Recently, switched-capacitor dc-dc converters have been used to multiply or divide voltage. The integration between switched-capacitor (SC) principles and traditional converters has been a good option to increase the rated conversion of conventional structures, as verified in [13]–[16] for dc-dc converter, [17] for rectifier and [18] for inverters. Some disadvantages of SC circuits, as parasitic elements, hard switching and peak of current, limited their power. However, recent research has been developed, as in [19]–[22], to increase the power range of SC application.

In this context, in this paper, the integration between a VSI and a switched-capacitor converter (SCC) topology is proposed, in order to obtain a step-up voltage source inverter with linear gain characteristics without using low-frequency transformers or dc-dc boost stages. The novel structure is named as VSI-SCC.

II. PROPOSED INTEGRATION BETWEEN INVERTER AND SWITCHED-CAPACITOR

The proposed converter is shown in Figure 1(a). VSI-SCC topology can work in buck or boost mode and it allows a bidirectional power flow. Furthermore, the proposed converter also presents split-phase characteristics at the output stage (voltages under C_2 and C_3), which can expand the range of potential applications for the proposed converter. The main aim behind this topology is to boost the VSI output voltage using an ac-ac SCC [23], [24] topology instead of a transformer. The only magnetic device of the proposed topology is the inductor on the filter stage. The capacitor C_1, at the filter stage, is the integrating element, being part of both converters (VSI and SCC). In [18] are shown preliminary results of the proposed structure. This study presents more complete experimental results, besides a n cells SCC analysis and a comparison between this structure and other boost inverters. In [25] is shown a VSI+SCC step down structure and in [26] and [27] a dc-dc SCC is employed at the VSI input.

A. Voltage Source Inverter

The inverter implemented in the proposed converter is a full-bridge inverter with an output filter and a three-level PWM modulation. The peak voltage value of this converter is defined by:

$$V_{ip} = ME \tag{1}$$

where:

M - Index modulation;
E - Input voltage.

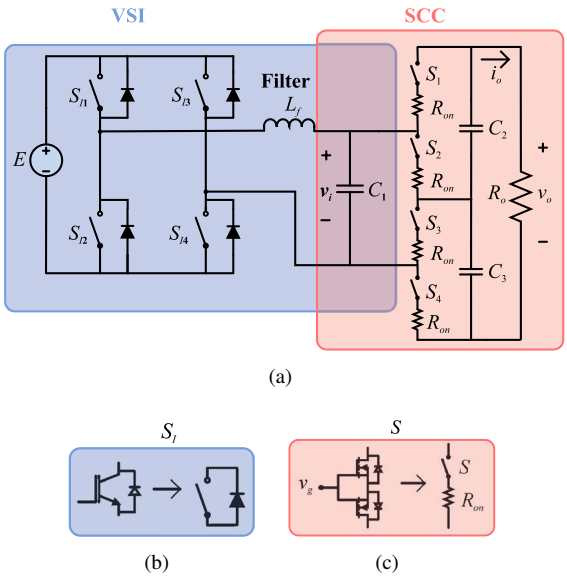


Fig. 1. Proposed topology and switch models: (a) Proposed topology; (b) VSI switch model; (c) SCC four-quadrant switch model.

B. Passive Filter (LC)

A conventional second-order passive filter LC is employed between the VSI and the SCC. The inductor L_f in Figure 1(a) is designed considering the current ripple in accordance with:

$$\Delta_{I_L} = \frac{EV_{ip}sin(\omega t)}{2EL_f f_s} \tag{2}$$

where f_s is the switching frequency.

The filter capacitor is defined by the SCC equivalent capacitance and will be described in a later section.

C. Switched-Capacitor Converter

The SCC shown on the right side of Figure 1(a) is a step-up ac-ac converter. This converter naturally equalizes the capacitor voltages of C_2 and C_3 if these capacitances and switching frequencies are properly designed, as demonstrated in [23]. The resistance, R_{on}, in Figure 1(a) represents the equivalent series resistance of the four-quadrant switch, obtained from the manufacturer datasheet.

The SCC topology can operate in buck or boost mode and, since a higher output voltage is desired in this study, the boost mode was used. For the boost mode there are two different operational stages. The first is when the switches S_1 and S_3 are turned on, as shown in Figure 2(a). In this operational stage the C_1 voltage is equalized with the C_2 voltage. In the second stage, shown in Figure 2(b), the switches S_1 and S_3 are blocked and S_2 and S_4 are turned on and therefore the C_1 voltage is equalized with the C_3 voltage. The gate signals of the SCC are shown in Figure 2(c). Usually, a dead-time is imposed in the switching between the S_1-S_3 and S_2-S_4 to avoid a short circuit.

The duty cycle must be close to 0.5 to equalize both the C_2 and C_3 voltage values with the lowest impedance. Thus, it is assumed that this topology has a fixed duty cycle and it works in open-loop.

The presented analysis in this section was carried out considering the positive semi-cycle of the sinusoidal waveform, however, for the negative part it works in a dual way. In Figure 3 the voltage and the current waveforms for the capacitors and the switches of the SCC topology for both positive and negative sinusoidal semi-cycle parts are shown. The attributed current flow for Figure 3 is shown in Figure 2(a) and 2(b).

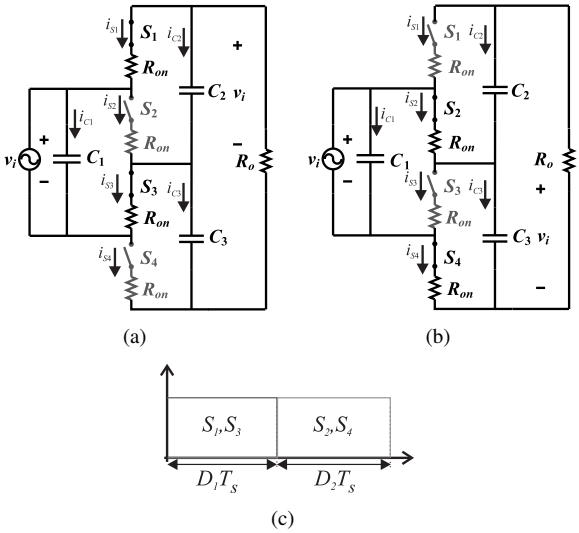


Fig. 2. Operational stages of the SCC topology: (a) First operational stage; (b) Second operational stage; (c) SCC gate signals.

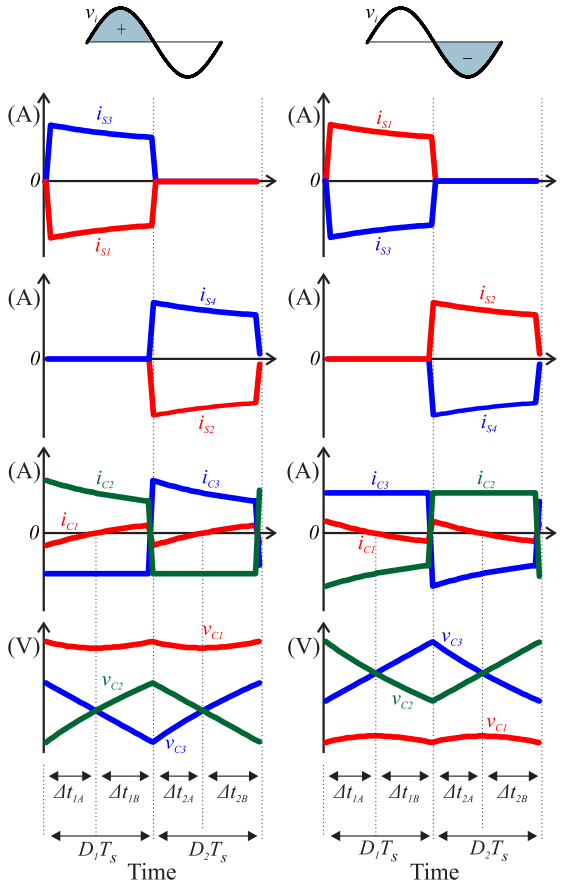


Fig. 3. Voltage and current waveforms for the switches and the capacitors of the SCC topology considering positive and negative sinusoidal semi-cycles.

In accordance with [28] and [29], SCC topologies can operate in three different ways, based on the capacitor current (i_c). That ways depending on the switched capacitor, R_{on} and the operating frequency. These operational modes are the complete charge (CC), the partial charge (PC) and the no charge (NC) mode. The waveforms for the operational charging modes are shown in Figure 4. In the CC mode the current on the switched capacitor C_1 reaches zero, but the currents in modes PC and NC do not. Also, in the CC mode the current reaches high values and, consequently, higher losses occur. Therefore, this mode is not a good choice for the converter proposed in this paper. On the other hand, the NC mode requires high capacitance and switching frequency values, leading to high costs and technological limitations. Thus, the mode which provides the best results is the PC mode and for this reason it was used in this study.

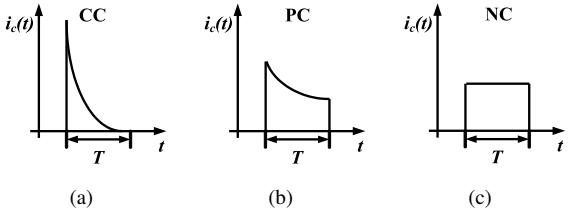


Fig. 4. SSC operational charging modes: (a) Complete charge (CC); (b) Partial charge (PC); (c) No charge (NC).

Considering a low frequency analysis, v_o in Figure 1(a) can be obtained by summing the voltage across the capacitors C_2 and C_3, as described by:

$$v_o = v_{C_2} + v_{C_3} = v_i + v_i = 2v_i \tag{3}$$

where:

v_i - VSI output voltage;

v_o - SCC output voltage.

Thus, from (3) it is possible to determine the static gain, which is the ratio between the output and input voltages given by:

$$G = \frac{v_o}{v_i} = \frac{2v_i}{v_i} = 2. \tag{4}$$

As previously described, the gain for the structure proposed in Figure 1(a) is two. However, a higher gain can be obtained if more cells are added in series, as demonstrated in [23] and [28].

The equivalent circuit seen by the low voltage side is shown in Figure 5(a). In this figure it was considered that:

$$C_2 = C_3 = C_x. \tag{5}$$

The duty cycle was equal to 0.5 to balance the capacitor voltages. R_{eq} is the equivalent resistance seen from the low voltage side. The conduction losses of the switched capacitor cell can be designed by a resistance, as discussed in [23], [28] and [29]. This resistance is called of series resistance (R_s), and is given by:

$$R_s = \frac{2R_{on}}{f_s\tau}\frac{(1-e^{-1/f_s\tau})}{(1-2e^{-D/f_s\tau}+e^{-1/f_s\tau})}. \tag{6}$$

The constant time, τ, is obtained by:

$$\tau = 2R_{on}C_1. \tag{7}$$

As seen in (6), the value of R_s changes for different switching frequencies and τ values. Thus, in order to understand the behavior of R_s, (6) was plotted in Figure 5(b) for different f_s and τ values. From this figure it is possible to conclude that, for lower frequencies and τ values, the series resistance has a higher value and, consequently, the conduction losses are higher. The minimum value for R_s is equal to $2R_{on}$, in the NC operational mode.

From Figure 5(b) it is also possible to determine the limits for the operational modes [28]. Thus, in order to design a converter to operate in the PC mode, the designer should respect the limits shown in Figure 5(b) [23]. The first limit is given by:

$$5\tau > T_s/2. \tag{8}$$

Therefore substituting (7) into (8) the following relation is obtained:

$$2R_{on}f_sC_1 > 0.1. \tag{9}$$

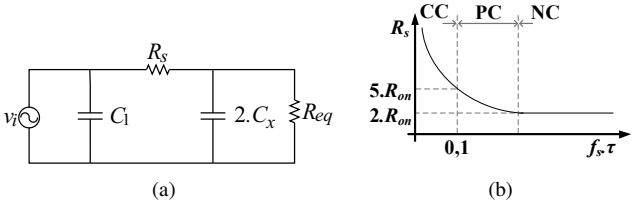


Fig. 5. SCC parameters: (a) Equivalent circuit; (b) Series resistance (R_s) for different frequency and constant time τ values.

D. Integration Seen from the VSI Side

From the VSI side the SCC topology is seen as an equivalent capacitor, which is part of the passive output filter. This equivalent capacitor can be found disregarding the R_{on} resistors in Figure 5(a).

Considering the parameters shown in (5) the equivalent capacitance seen from the low voltage side is given by

$$C_{eq} = C_1 // \frac{4C_x}{2} = C_1 // 2C_x. \tag{10}$$

E. Integration Seen from the SCC Side

From the SCC side the VSI is represented by an alternating voltage source added to a high-frequency component generated by the PWM modulation. This high-frequency component will circulate through the SCC components, causing losses. Figure 6 shows the circuit seen from the SCC side for the two operational stages.

F. Static Gain

The static gain for the complete circuit, i.e., after the integration between VSI and SCC, is obtained multiplying the index modulation (M) by the static gain provided by (4). Thus, the static gain for the proposed converter is:

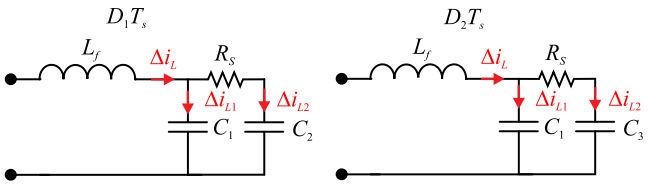


Fig. 6. Circuit seen from the SCC side for the two operational stages.

$$G_t = 2M. \tag{11}$$

Therefore, the peak voltage value of the proposed converter output voltage is given by:

$$V_{op} = 2ME. \tag{12}$$

G. Dynamic Analysis in Open-Loop

Numerical simulations were carried out with open-loop to validate the equivalent capacitance mentioned in subsection D. In the simulation two circuits were observed, one considering the circuit from Figure 1(a) and the other considering C_{eq} obtained in subsection D. The results obtained from the simulation for these two circuits are reported in Figure 7. Based on the similarities in the step responses for the two circuits, it is verified that the equivalent capacitance properly represents the equivalent circuit and can be used in the following analyses.

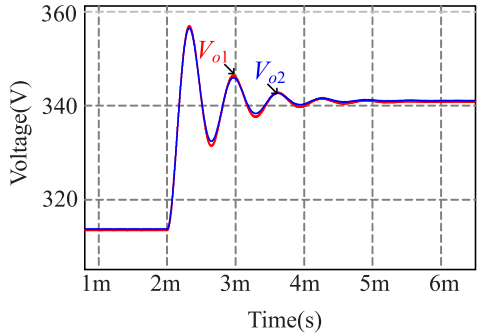


Fig. 7. Step response for comparison between the circuits shown in Figure 1(a) (V_{o1}) and using C_{eq} (V_{o2}).

H. Dynamic Analysis in Closed-Loop

The closed-loop control implemented for the output voltage is shown in Figure 8. The feedback control in this topology can be carried out in two different parts of the circuit, i.e., in the VSI output or in the SCC output port. In both cases, the converter model is found with the small-signal model, based on [30], [31], wherein the control variable is the duty cycle. If the feedback control is carried out at the VSI output, the converter model $G_1(s)$ in Figure 8 is given by:

$$G_1(s) = \frac{\hat{v}_i}{\hat{d}} = \frac{E}{s^2 L_f C_{eq} + s\frac{L_f}{R_{eq}} + 1}. \tag{13}$$

On the other hand, if the feedback control is carried out at the SCC output, the converter model is given by:

$$G_2(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{2E}{s^2 L_f C_{eq} + s\frac{L_f}{R_{eq}} + 1}. \tag{14}$$

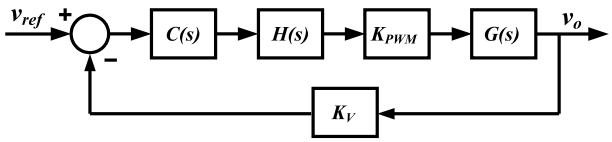


Fig. 8. Closed-loop control diagram.

The frequency response of the open-loop transfer function of the proposed converter ($K_{PWM}.K_v.G_1(s)$) in the no-load case is plotted in the Bode diagram shown in Figure 9. The curve in this figure has multiple zero crossings (around 0 dB), which might hinder the converter control. Therefore, to avoid multiple zero crossings, a band-rejection filter was designed and tuned to around the LC filter resonant frequency. The band-rejection filter transfer function is represented by $H(s)$ in Figure 8 and is given by:

$$H(s) = \frac{s^2 + (2\pi f_f)^2}{s^2 + 2\pi f_a + (2\pi f_f)^2}. \tag{15}$$

where:

f_f - Center frequency of the band-rejection filter;

f_a - Bandwidth of the band-rejection filter.

The controller transfer function is represented by $C(s)$ in Figure 8. To control the proposed converter a PI controller was implemented.

In Figure 8, the symbols K_v and K_{PWM} represent the gain given by the voltage sensor and PWM modulation, respectively.

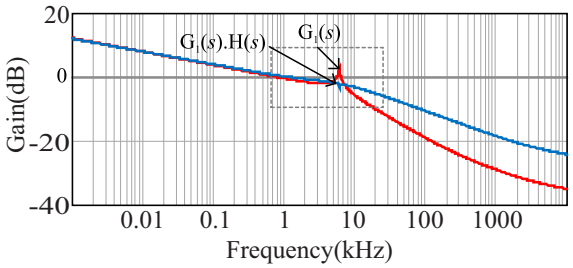


Fig. 9. Frequency response of the open-loop transfer function for the no-load case without and with the band-rejection filter.

III. GENERALIZATION TO *n* CELLS

Up to this point, the analysis was carried out with only one SC cell, composed of two bidirectional switches and two capacitors. If desired, the gain can be increased by cascading more SC cells, as shown in Figure 10. Thus, it is possible to increase the VSI gain by integrating an SCC with n SC cells at the VSI output, as can be seen in Figure 10(d).

The static gain for an n-cells SCC is defined by:

$$G_n = n + 1. \tag{16}$$

The number of bidirectional switches for n SCC cells is described by:

$$N_{bid\_sw} = 2(n+1). \tag{17}$$

The total number of capacitors for the SCC topology is given by:

$$N_{cap} = n+1. \tag{18}$$

A structure with n SCC cells considering all of the capacitors with the same capacitance values is shown in Figure 10(c). If even and the odd switches of the SCC cells are synchronized, i.e., they commutate at the same time, the voltage balance in all capacitors is guaranteed.

The equivalent capacitance seen by the low voltage side can be found in a way similar to that described in section II-D. Therefore, the equivalent capacitance is given by:

$$C_{eq} = C(2n+1). \tag{19}$$

Each SCC cell can provide an additional gain in the output voltage. Thus, the output peak voltage for the complete structure can be defined by:

$$V_{op} = (n+1)ME. \tag{20}$$

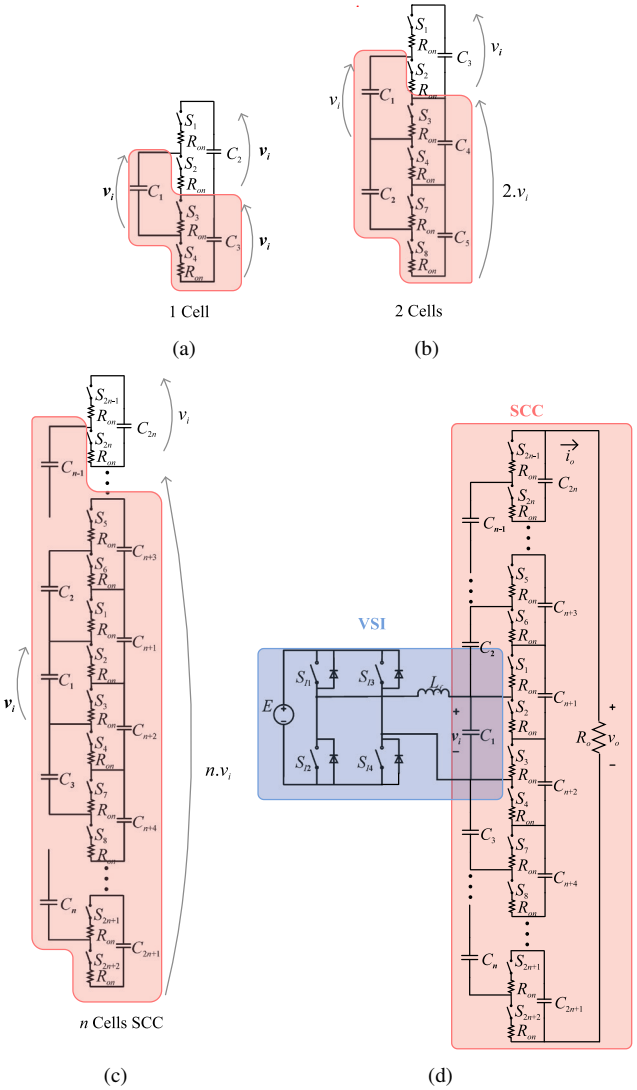


Fig. 10. Generalization for n cells: (a) One-cell SCC; (b) Two-cells SCC; (c) n-cells SCC; (d) Generic structure of the VSI-SCC with n SCC cells.

Finally, the transfer function of the proposed topology for the structure shown in Figure 10(c) is given by:

$$G_3(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{(n+1)E}{s^2 L_f C_{eq} + s\frac{L_f}{R_{eq}} + 1}. \tag{21}$$

Similarly, the equivalent circuit for a structure with n SCC cells is shown in Figure 11.

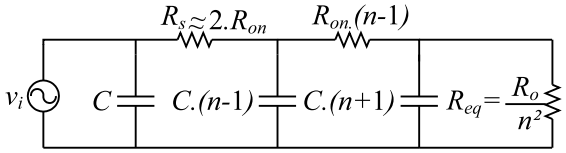


Fig. 11. Equivalent circuit for a structure with n SCC cells.

IV. PROTOTYPE AND EXPERIMENTAL RESULTS

The theoretical concepts developed in this paper was verified in a 1 kVA prototype. They were built separately as two cells and subsequently connected to each other. The specifications for the two prototypes are shown in Table I, and the controller specifications are shown in Table II. The SCC topology was built using two series-connected MOSFETs with a common source. The capacitors are subject to high frequency and high value of currents and besides that to a high voltage stress. Therefore, an AC voltage is applied in these capacitors. Thus, is common to use polypropylene film capacitors. The main components used to build the SCC prototype are shown in Table III. The VSI was build with a integrated IGBT module. The main components of the VSI are shown in Table IV. The schematic and gate driver circuitry for the VSI+SCC structure are shown in Figures 12 (a), 12 (b) and 12 (c).

The capacitors, switches and switching frequency from SCC stage are defined to operate in PC mode, as was presented in in Figure 3. Hence, the current across the SCC switches at the worst case (at peak of v_i voltage) was verified by simulation and the result is seen in Figure 13. The currents obtained are similar to PC theoretical curve shown in Figure 4, which corroborates the proposed design.

TABLE I
VSI and SCC Specifications

VSI		SCC	
S	1000 VA	S	1000 VA
E	200-300 V	V_{irms}	110 V
V_{irms}	110 V	V_{orms}	220 V
f_o	60 Hz	f_o	60 Hz
f_s	20 kHz	f_s	100 kHz
Δ_{ILmax}	20%	C_1, C_2, C_3	20 μF
L_f	700 μH		
C_{eq}	60 μF		

Figure 14(a) shows the voltage across the SCC switches, where the maximum value reached is close to the VSI output peak voltage. Figure 14(b) shows the output voltage (v_o), the input voltage at SCC (v_i), the control (reference) voltage (v_c) and dc input voltage (E) at the VSI input terminal. In this figure it is clearly shown that v_o is twice v_i, and therefore the VSI-SCC topology properly inverts and steps up the input voltage. This test was carried for the no-load case to test the

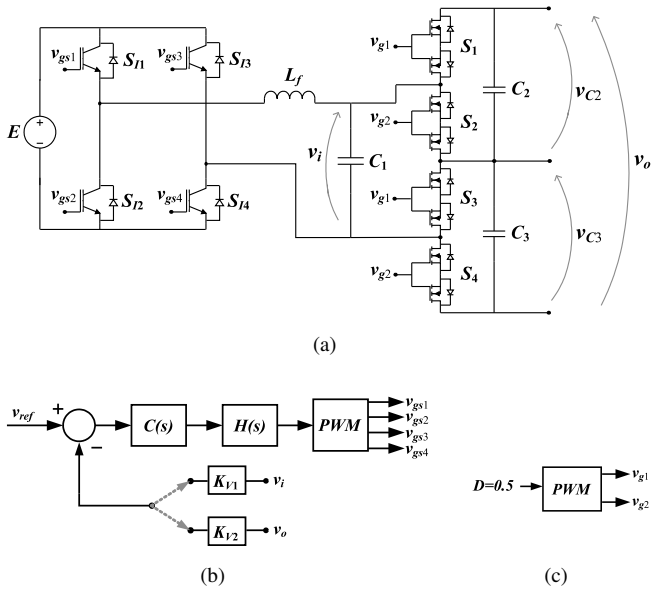


Fig. 12. (a) Schematic; (b) Gate driver circuitry for VSI stage; (c) Gate driver circuitry for SCC stage.

TABLE II
Control Specifications

Phase margin of the system	90°
Zero dB crossing over	600 Hz
PI zero (ωz)	533 rad/s
PI gain	0.82
Center frequency of the band-rejection filter	796 Hz
Bandwidth of the band-rejection filter	486 Hz
LC filter resonant frequency	776 Hz

TABLE III
SCC Main Components

Description	Values
MOSFET	FQA62N25C (R_{on}=60mΩ)
Polypropylene Capacitors (two in parallel)	932C4W10J-F (10μF/400V/ESR=1.8mΩ)
MOSFET Driver	UCC27424
Pulse Width Modulator	UC3525

TABLE IV
VSI Main Components

Description	Values
IGBT MODULE (Integral gate driver)	FNA41060 (660V-10A)
Control	Operational Amplifiers
Voltage transducer	LV 25-P
Inductor	700μF-60Hz

system stability.

The experimental results shown in Figure 14(c) and Figure 14(d) verified the converter controllability for a load step of 50% to 100% (see i_o current). Two tests were carried out, one with a feedback control at the input terminal of the SCC topology and the other one at the output of the proposed topology. In both cases, the control was stable and controlled the system correctly. Furthermore, it had a fast dynamic response.

Voltage regulation at the converter output voltage was also

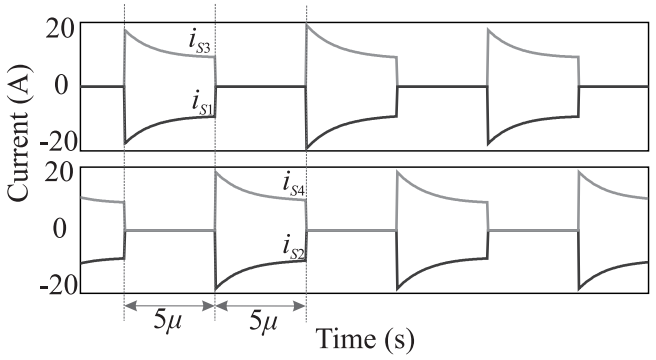


Fig. 13. Current across the SCC switches.

carried out for both control methods and the results are shown in Figure 15. From this figure, it is possible to conclude that on using feedback control at the output voltage (v_o) the system obtains a better regulation voltage. This can be explained by the different approaches to the losses in the two control methods. When the feedback control is placed at v_i, the control does not consider the losses in the SCC structure. On the order hand, if the feedback control is carried out at the output voltage, the control will regulate the voltage considering the losses in both converters.

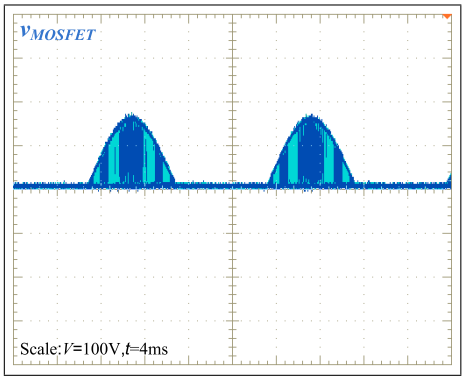
The experimental results obtained with a RL load are reported in Figure 16(a) and Figure 16(b), with a feedback control at the input (v_i) and the output (v_o) terminals of the SCC topology. The system shows stability using both methods, however, once again the regulation voltage provided better results when the feedback control was placed at the output voltage (v_o).

The split-phase characteristic was also tested. To carry out these tests, a resistive-inductive load (55 Ω + 45 mH) was placed at output v_{C2} and resistive loads (60 Ω and 120 Ω respectively) were added at outputs v_{C3} and v_o (see Figure 12(a)). Even with different loads at each output the voltages remained regulated. The results are shown in Figure 16(c) and Figure 16(d).

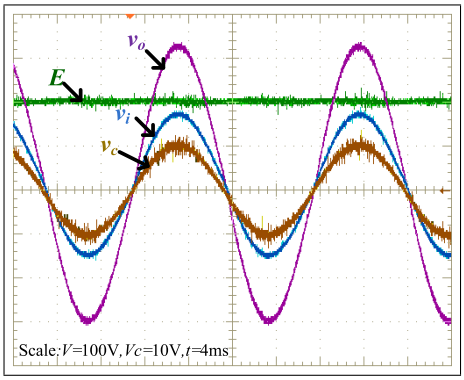
Results for the SCC converter operating with 1 kW are given in [18] and [23], and the efficiency reached 96%. Furthermore, during the test it was observed that the VSI converter reached an efficiency of 95%. Therefore, the complete structure has an efficiency of approximately 91%. The efficiency curves of the VSI, the SCC, and the VSI+SCC are shown in Figure 17.

V. COMPARISON BETWEEN THE PROPOSED CONVERTER WITH CONVENTIONAL SOLUTIONS

This paper proposes an integration between VSI and SCC topologies, which provides a higher voltage at the output compared with the input. For this reason, the proposed structure is compared with conventional step-up inverter solutions, as Z-Source Inverter (ZSI) [10], [32]–[35], Differential Boost Inverter (DBI) [5], [36], conventional two-stage Boost-Buck inverter (dc-dc Boost converter + classical VSI, named as TS-BBI) and classical Buck VSI + autotransformer (named as VSI+AT). This comparison is shown in Tables V and VI, considering a LC filter at the output,



(a)



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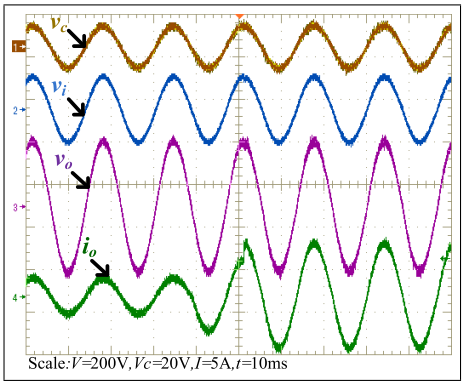
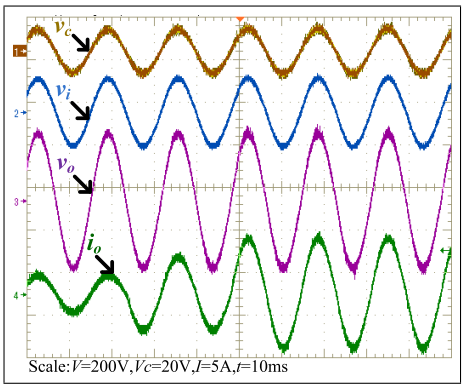


(c)



(d)

Fig. 14. Experimental results: (a) SCC switch voltage; (b) Output voltage (v_o), voltage at the SCC input terminals (v_i), control voltage (v_c) and dc input voltage (E) at the VSI input terminal for no-load case; (c) Load step response with feedback control at v_i ; (d) Load step response with feedback control at v_o .

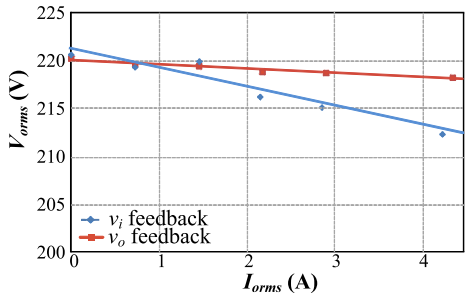


Fig. 15. Regulation voltage considering feedback control at the input v_i and the output v_o terminals of the SCC topology.

needed to ensure a sinusoidal output voltage in each topology.

TABLE V
Quantitative Comparison Between the Proposed Converter and Other Solutions

Number of elements	ZSI[1]	DBI[2]	TS-BBI[3]	VSI+AT[6]	VSI+SCC[4]
Inductors[5]	3	2	2	1	1
Capacitors[5]	3	3	2	1	3
Autotransformer[6]	-	-	-	1	-
Diodes	5	4	5	4	12
Active switches	4	4	5	4	12
Driver circuits	4	4	5	4	12

[1]Based on [10], [32]–[35].[2]Based on [5], [36].[3]Based on [34], [35].[4]Consider $n = 1$.[5]Consider the LC output filter.[6] Low frequency.

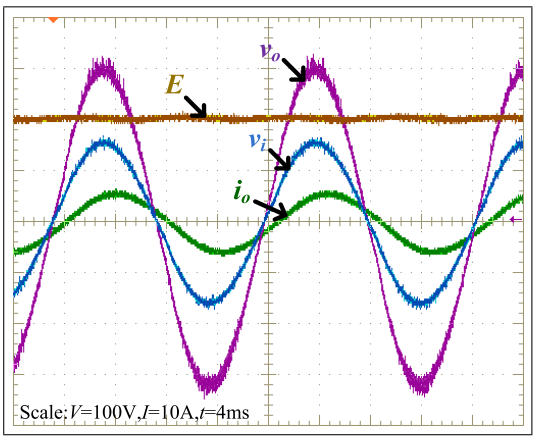
TABLE VI
Qualitative Comparison Between the Proposed Converter and Other Solutions

Characteristics	ZSI[1]	DBI[2]	TS-BBI[3,4]	VSI+AT[4,5]	VSI+SCC[4,5]
Boost factor	$\frac{1}{1-2\cdot d}$	$\frac{1}{1-d}$	$\frac{1}{1-d_{boost}}$	a	n
Static Gain	$\frac{1}{1-2\cdot d}$	$\frac{2\cdot d-1}{d\cdot(1-d)}$	$\frac{d_{buck}}{1-d_{boost}}$	$d_{buck}\cdot a$	$d_{buck}\cdot n$
Voltage stress factor[6]	$\frac{1}{1-d}$	$\frac{1}{1-d}$	$\frac{1}{1-d_{boost}}$	E	E
Gain Characteristic	Non Linear	Non Linear	Non Linear	Linear	Linear
Complexity of controller	High	High	Medium	Low	Low

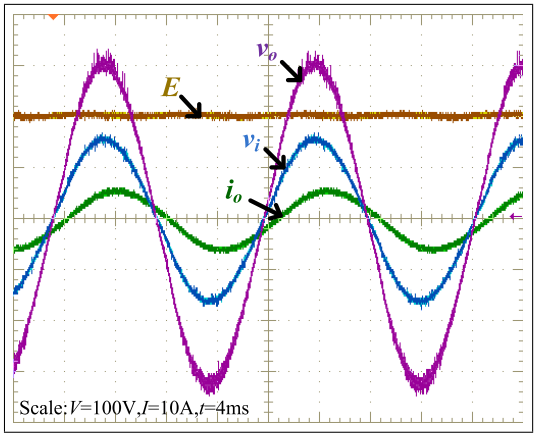
[1]Based on [10], [32]–[35].[2]Based on [5], [36].[3]Based on [34], [35].[4]Two-stage topologies can be presented by two duty cycles, one for Boost stage (d_{Boost}) and another for Buck stage (d_{Buck}).[5]Variable a is the autotransformer ratio and n is the number of SC cells.[6]In the worst case, the ZSI has other voltage stresses on Z-capacitor, which can be seen in references [32], [34], [35].

The quantitative analysis presented in Table V compares the VSI+SCC and other conventional solutions. The proposed converter employs a fewer number of magnetic components, however, it has higher number of switches, being a typical characteristic of switching capacitor converters.

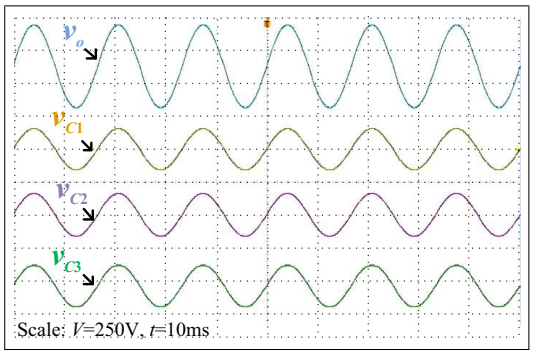
A qualitative analysis is also presented in Table VI. The proposed converter has a linear boost factor, i.e., a linear static gain, which is similar to the VSI+AT solution. The others step-up structures have a non-linear boost factor (as shown in Table VI) and, consequently, a non-linear static gain. A linear boost factor characteristic facilitates the proposed converter control system, however, it should built with more SC cells to obtain higher gains.



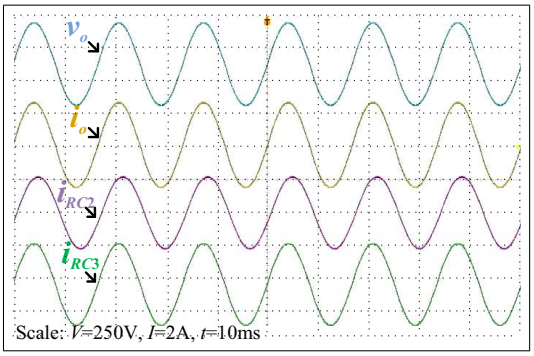
(a)



(b)



(c)



(d)

Fig. 16. Experimental results: (a) Under RL load, with feedback control at v_i ; (b) Under RL load, with feedback control at v_o ; (c) For the split-phase outputs: voltage waveforms; (d) For the split-phase outputs: current waveforms.

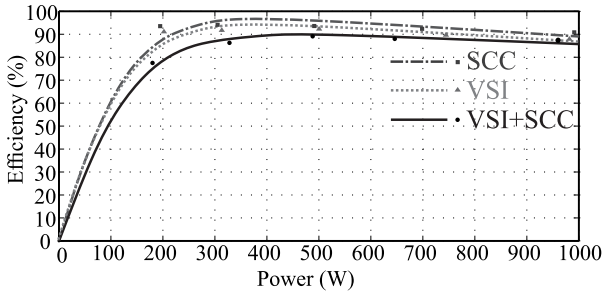


Fig. 17. Efficiency curves of the complete and individual structures.

Another important characteristic that should be analyzed is the voltage stress across the switches. The semiconductors of VSI+SCC and VSI+AT topologies have a maximum voltage equal to the input voltage, which is independent of the SC cells number. On the other hand, the maximum voltage across the semiconductors of Z-Source and Boost topologies are dependent of the operational point.

Therefore, because both SCC and autotransformer have linear boost factor characteristic, one can conclude that the proposed converter has some similarities with the VSI+AT solution, and, thus, the last topology is used to carry out a qualitative and a quantitative analysis. For this reason, a comparison between the SCC prototype and a commercial autotransformer was carried out and the results are shown in Table VII. The SCC has a lower power density than the autotransformer; however, it has much higher specific power. Therefore, if the two converters (VSI-SCC) are placed on the same board and the magnetic components are optimized, it is expected that the final volume of the proposed converter could achieve a higher power density value.

TABLE VII
Comparison Between the SCC and an Autotransformer

	Autotransformer	SCC
Volume (cm^3)	1109.5	1449
Mass (kg)	2.7	0.7
Aparent Power (VA)	1010	1000
Power Density (VA/cm^3)	0.91	0.69
Specific Power (VA/kg)	374.1	1428.6

VI. CONCLUSIONS

The goal of the study reported herein was to investigate the possibility for integration between the VSI and the SCC converters. It results in a transformerless step-up inverter where the static gain can be increased using more switched-capacitor cells in series. Furthermore, the proposed converter also presents split-phase characteristics at the output stage, which can expand the range of potential applications for the proposed converter. The proposed structure (VSI-SCC) is designed as a transformerless step-up inverter.

Static and dynamic characteristics were analyzed for both the VSI and SCC topologies individually and then the two converters were attached to each other to validate the proposed converter. To create the VSI and the SCC models, equivalents circuits were proposed and tested using numerical simulations and satisfactory results were obtained. The analysis was expanded to n SCC cells.

Once the models for the two converters had been obtained,

controllers were designed considering feedback control at two locations: at the SCC input terminal (v_i) and at the SCC output terminal (v_o). Therefore, to determine the best feedback control technique the converter regulation voltage at the output terminal was measured and the feedback control placed at v_o presented better results.

The theoretical concepts presented in this paper were validated through experimental results for both resistive and inductive loads, in both cases showing promising results in applications which require step-up inverters and split-phase outputs. The fact that the converter proposed in this paper does not use low-frequency, bulky and heavy transformers makes it competitive in terms of volume, weight and efficiency when compared to conventional structures.

The proposed converter has higher specific power and lower power density when compared with commercial autotransformers.

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