STUDY OF HIGH STEP-UP GAIN DC-DC CONVERTERS BASED ON STACKING OF NON-ISOLATED TOPOLOGIES

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***Abstract* – This paper approaches the study of stacked DC-DC converters with high step-up gain, using low-voltage devices. The proposed topologies are generated from the stacking of conventional buck-boost structures and they are suitable in applications that a high conversion ratio is required. The stacked converters can also be employed as DC bus to provide one or several output voltage levels with self-balancing, and thus different loads can be connected to one or more capacitors of the stack. A generalized theoretical analysis of the proposed topologies approaching static gain, voltage and current stresses on the main components and power flow analysis is described in this paper. A 1-kW prototype with 100 V input voltage and 400 V output voltage was designed, built and tested. The experimental results corroborate the generalized theoretical analysis and they demonstrate the feasibility of the proposed converters.**

Keywords **– High Step-Up Conversion Ratio, Integration of Commutation Cells, Non-Isolated Applications, Stacked DC-DC Converters.**

I. INTRODUCTION

Nowadays, high-voltage gain and high performance DC-DC converters have been widely used in power conversion stage of DC systems. High step-up converters are commonly required in many applications, such as the front-end stage for clean energy source, electric vehicles, DC back-up energy system for a UPS, fuel cell powered systems, telecommunications power systems and the high-intensity discharge lamp ballast used in automotive headlamps [1–5].

Theoretically, the conventional boost converter could be an adequate solution in such applications. However, in practice, the static gain is limited due to losses associated with the inductor, filter capacitor and power semiconductors. With a high value of duty cycle, the efficiency decreases considerably, the electromagnetic interference (EMI) problem is severe and voltage stress on the semiconductors increases significantly when the boost converter works with higher gains [6]. Therefore, several high voltage gain converters have been described in the technical literature in order to overcome the aforementioned limitations [7–32]. Some topologies employing a modified cascaded boost in order to achieve high voltage gain were proposed, such as a single-switch quadratic boost converter and a two-switch three-level boost converter [7]. The main drawbacks of this alternative are increased complexity and cost, and low efficiency due to losses in the successive power processing stages.

High voltage gain can also be achieved through the coupled inductors used as a transformer in non-isolated DC-DC converters, which reduces the switch voltage stress [8–13]. In [14–17], a family of interleaved high step-up boost converters with winding-cross-coupled inductors is proposed, which the switch voltage stress is reduced and the input and output current ripples are minimized because the extreme duty cycles are avoided. In [18], a coupled inductor boost integrated flyback converter, with high voltage gain and ripple-free input current, is proposed. By incorporating a coupled inductor into the boost cell, high voltage gain is achieved by adjusting the turns ratio of the coupled inductor.

Other alternatives for high voltage gain are the topologies based on switched capacitors (SC) [19–21], which are more suitable for low power applications. The main disadvantages of the switched capacitor technique are poor output voltage regulation and the high current peaks through the semiconductors due to the charge-discharge of the switched capacitors during the switching transients. In [22], a method combining an SC converter and the switching-mode DC-DC converter is proposed, integrating the advantages of the high voltage gain of a SC converter and excellent output regulation of a switching-mode DC-DC converter.

The concept of three-state switching cell (3SSC) was introduced in [23] as an alternative for high current applications due to the distribution of losses among the power semiconductors. In recent years, several DC-DC converters topologies, with high voltage gain, employing this concept have been proposed in the literature [24, 25]. Auxiliary windings can be added to the autotransformer of the 3SSC providing high voltage step-up [26, 27]. The static gain can be adjusted by the turns ratio between the autotransformer winding and auxiliary windings, without increasing the voltage stress for the active switches.

Voltage multiplier cells (VMCs) can also be added to the boost converters based on 3SSC in order to provide high voltage gain. A family of DC-DC converters based on 3SSC and VMC for high power and high current applications was proposed in [28], where the topologies presented reduced blocking voltages across the controlled switches compared to similar circuits. A disadvantage of this proposal is the need for a high component count to obtain high voltage gain.

Within this context, this paper presents the study of non-isolated stacked DC-DC converters with high step-up voltage gain. The proposed topologies are obtained from stacking

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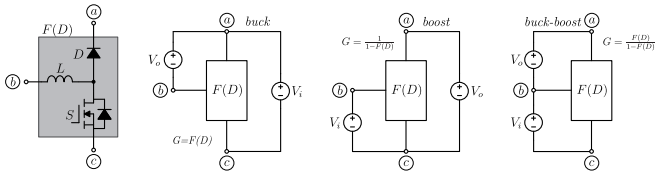
buck-boost structures and the main features of the converters are possibility of modularity and natural voltage balance across the capacitors, which provides reduced blocking voltages across the semiconductors when operating with optimal duty-cycle. Therefore, the proposed topologies can be used as DC bus where one or several output voltage levels are required with self-balancing, for example, systems with multilevel inverters.

II. COMMUTATION CELL CONCEPT

The classical converters buck, boost and buck-boost can be described through the commutation cell concept. On analyzing these three converters, common factors can be observed: all have an inductor, a diode and an active switch. These three components form the central nucleus of basic converters and they are known in the literature as commutation cell, as shown in Figure 1.a. The three converters have the same commutation cell, and the only difference between them is the way in which the input and output voltage sources can be connected to the commutation cell. Thus, given a generic commutation cell, there are only three possibilities of connecting voltage sources transferring energy from one to another, as shown in Figure 1.b to 1.d.



(a) (b) (c) (d)

Fig. 1. Classical converters applied to a generic commutation cell: (a) Commutation cell of the classical converters; (b) Buck structure; (c) Boost structure; (d) Buck-boost structure.

Conceptually, a commutation cell is associated with a mathematical function $F(D)$ which is related to the duty cycle D, generating a maximum of three topologies with characteristic buck, boost or buck-boost. Thus, if the mathematical function $F(D)$ of the commutation cell is known, it is possible to calculate the static gain of the topologies without the need for any theoretical analysis [33, 34].

III. GENERATION OF THE PROPOSED TOPOLOGIES

The proposed non-isolated high step-up DC-DC converters are generated based on the commutation cell concept. In this paper, six commutation cells are applied to the buck-boost structure shown in Figure 1.d. Figures 2.a, 2.c, 3.a, 3.c, 4.a and 4.c show the six commutation cells (basic, Cúk, SEPIC 1, zeta 1, SEPIC 2 and zeta 2, respectively) applied to the buck-boost structure (Figure 1.d). These topologies contain one commutation cell, resulting in an alternative to the conventional boost converter. In order to obtain high voltage gain, the proposed converters are generated through the stacking of buck-boost structures with their respective commutation cells. The number of stacked cells can be increased depending on the input voltage and on the required output voltage and, thus, high voltage gains can be obtained. Figures 2.b, 2.d, 3.b, 3.d, 4.b and 4.d show the proposed topologies for a generic number of cells. The main features of the proposed converters are as follows: possibility of modularity and natural voltage balance across the capacitors, providing low voltage stresses on the power semiconductors when operating with the optimal duty-cycle, regardless of the number of stacked cells.

The proposed topologies have unidirectional power flow and they work as step-up converters. However, these topologies can be changed into bidirectional structures by replacing the diodes with active switches. Therefore, the proposed topologies can be applied as high step-down or high step-up DC-DC converters. In this paper, the theoretical analysis, design example and experimental results are reported only for the step-up operation.

IV. GENERALIZED THEORETICAL ANALYSIS OF THE PROPOSED TOPOLOGIES

In this section, a theoretical analysis of the topologies for a generic number of stacked cells is performed. In order to facilitate the analysis, the proposed topologies shown in Figures 2, 3 and 4 are divided into three groups of two converters: (i) basic and Cúk cells (Figure 2); (ii) SEPIC 1 and zeta 1 cells (Figure 3) and (iii) SEPIC 2 and zeta 2 cells (Figure 4). The converters of each group have as a common characteristic the same static gain. Table I shows the mathematical functions $F(D)$ associated with the commutation cells of each group, the operation range of the duty cycle and the static gain for one commutation cell.

The static gain of the topologies shown in Table I can be generalized for a number m of stacked commutation cells. Equations (1), (2) and (3) show the generic static gain as a function of the duty-cycle D and of the number of cells m for the topologies of group 1, 2 and 3, respectively. Figure 5 shows the static gain of the proposed topologies for different numbers of stacked cells. It should be noticed that, for a fixed value of duty-cycle, a high step-up gain will be obtained when the number of stacked cells is increased.

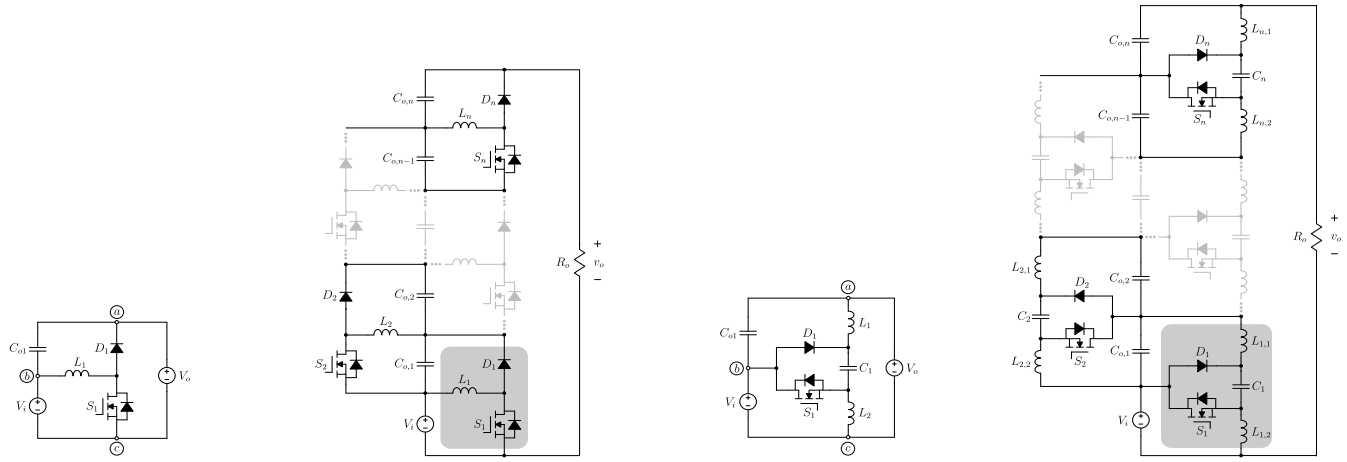
TABLE I
Comparison Among Topologies From Groups 1, 2 and 3

Characteristic	Groups		
	1	2	3
$F(D)$	D	$\frac{2D-1}{D}$	$\frac{D}{1-D}$
Duty cycle range	$0 < D < 1$	$0,5 < D < 1$	$0 < D < 0,5$
Static gain for one commut. cell	$G_{v1} = 1 + \frac{D}{1-D}$	$G_{v2} = 1 + \frac{2D-1}{1-D}$	$G_{v3} = 1 + \frac{D}{1-2D}$

$$G_{vm1}(D,m) = \frac{V_o}{V_i} = \sum_{k=0}^{m}\left(\frac{D}{1-D}\right)^k \quad (1)$$

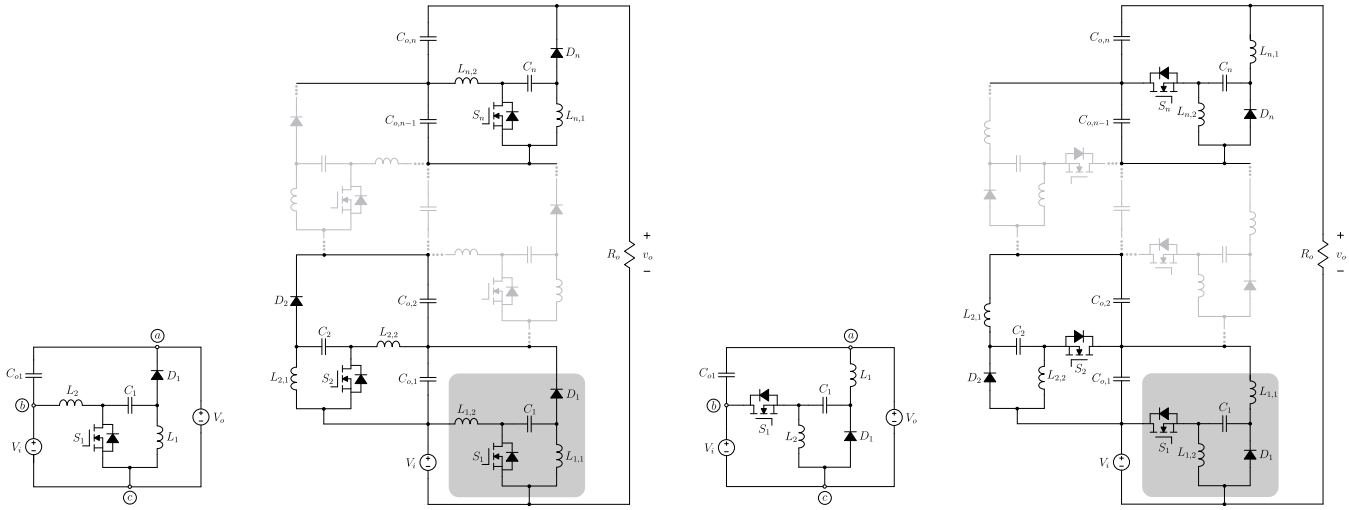
$$G_{vm2}(D,m) = \frac{V_o}{V_i} = \sum_{k=0}^{m}\left(\frac{2D-1}{1-D}\right)^k \quad (2)$$

$$G_{vm3}(D,m) = \frac{V_o}{V_i} = \sum_{k=0}^{m}\left(\frac{D}{1-2D}\right)^k. \quad (3)$$



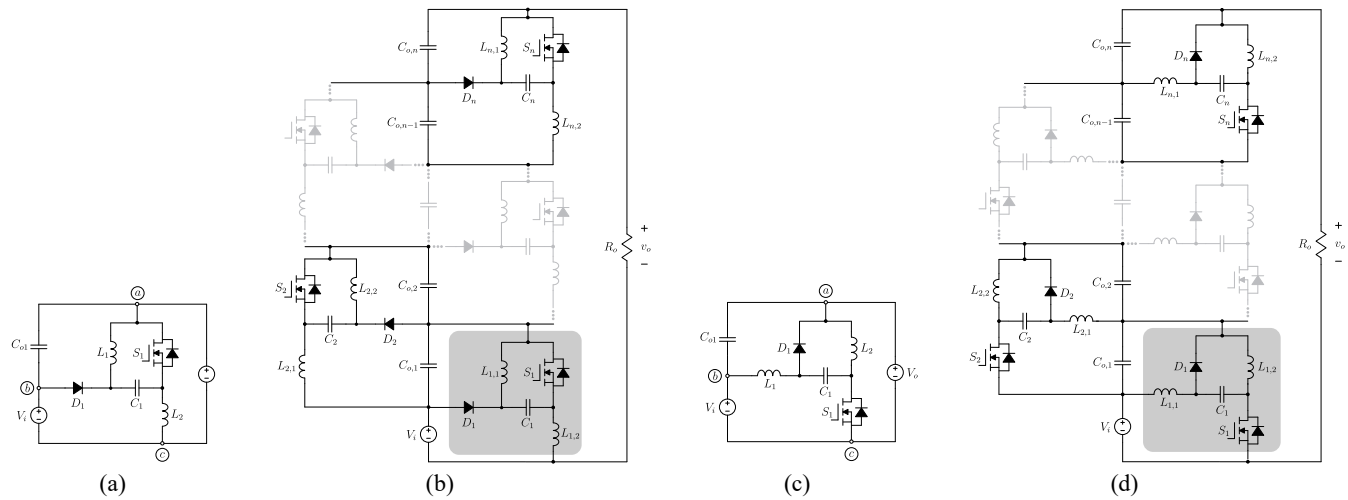
(a) (b) (c) (d)

Fig. 2. Proposed converters of group 1: (a) Basic commutation cell applied to the buck-boost structure; (b) Generalized version for a number *n* of stacked basic cells; (c) Cúk commutation cell applied to the buck-boost structure; (d) Generalized version for a number *n* of stacked Cúk cells.



(a) (b) (c) (d)

Fig. 3. Proposed converters of group 2: (a) SEPIC 1 commutation cell applied to the buck-boost structure; (b) Generalized version for a number *n* of stacked SEPIC 1 cells; (c) Zeta 1 commutation cell applied to the buck-boost structure; (d) Generalized version for a number *n* of stacked zeta 1 cells.



(a) (b) (c) (d)

Fig. 4. Proposed converters of group 3: (a) SEPIC 2 commutation cell applied to the buck-boost structure; (b) Generalized version for a number *n* of stacked SEPIC 2 cells; (c) Zeta 2 commutation cell applied to the buck-boost structure; (d) Generalized version for a number *n* of stacked zeta 2 cells.

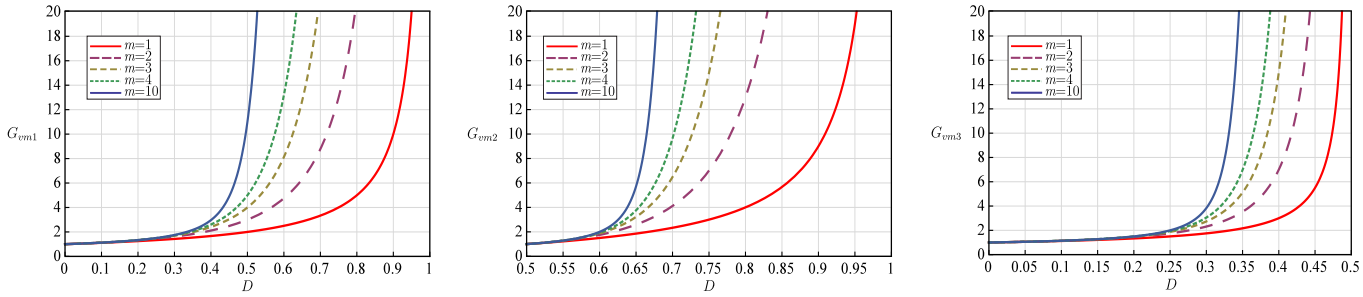


Fig. 5. Static gain as a function of the duty-cycle for different numbers of stacked cells: (a) Topologies of group 1; (b) Topologies of group 2; (c) Topologies of group 3.

The voltage across the stacked capacitors is also described as a function of the duty-cycle D, input voltage V_i and number of cells m, as defined in (4), (5) and (6). The variable n establishes the position of each capacitor in the stack, which can vary between 1 and m. The average voltage over the stacked capacitors versus duty-cycle considering $m = 4$ is shown in Figure 6, where it can be observed that there is an optimal duty-cycle value for each converters group which equally balances the voltage across the stacked capacitors and, consequently, reduces the voltage and current stresses on the power semiconductors. The generic expressions for the voltage and current stresses on the main components of the proposed converters parametrized as functions of the input and output variables are defined in Table II.

$$V_{Co,n1}(D,n) = V_i \cdot \left(\frac{D}{1-D}\right)^n \tag{4}$$

$$V_{Co,n2}(D,n) = V_i \cdot \left(\frac{2D-1}{1-D}\right)^n \tag{5}$$

$$V_{Co,n3}(D,n) = V_i \cdot \left(\frac{D}{1-2D}\right)^n. \tag{6}$$

The maximum voltage across the switches/diodes parametrized as a function of the output voltage V_o considering $m = 4$ is illustrated in Figure 7, where an optimal duty-cycle value for each converters group can also be observed. The rms current value for the switches and the average current value for the diodes versus duty-cycle parametrized as a function of the input current I_i can be seen in Figures 8 and 9, respectively.

V. ANALYTICAL DESCRIPTION

The proposed topologies in this paper present as feature a modular structure based on stacking of DC-DC converters. The converters work as balancing voltage modules and they are connected on two adjacent capacitors in the stack structure. Therefore, a converter with m capacitors contains m balancing modules (M_1 to M_n) and m output voltage levels. The load can be connected to one or more capacitors of the stack, as shown in Figure 10.a. The m output voltage levels will be multiple of the input voltage, when the converters operate with optimal duty-cycle. Hence, another potential application of these topologies is to use them as DC bus, in which several output voltage levels are required with self-balancing (for example, systems with multilevel inverters). It should be noticed here that the proposed topologies can be driven either using just one PWM modulator with one single controller, or each module uses its own modulator and controller. In that second option, an independent control of the m output voltage levels are achieved.

A. Current Distribution and Power Flow Analysis

The current distribution in the generalized structure operating with optimal duty-cycle is shown in Figure 10.b. It should be noticed that the current distribution in the voltage modules M_1 to M_n is unbalanced. This is a natural feature from the stacking of buck-boost structures, in which the current stresses are larger in modules closer to the low-voltage side (input voltage for step-up configuration).

The system efficiency may be estimated using the power flow analysis in the proposed converters. The power is transferred to the load through the m voltage modules (M_1 to M_n). On considering that the converters operate with optimal duty-cycle and the voltages across the stacked capacitors are balanced, the largest amount of power is processed by the module closer to the input voltage source, hence this module presents the highest current stress. The rated power of each module (considering m modules in stacked connection) is given by (7). The rated power of the voltage module closer to the input voltage source and closer to the load is given by (8) and (9), respectively.

$$P_{M_n} = \frac{(m+1-n)\cdot P_o}{m+1} \tag{7}$$

$$P_{M_{n=1}} = \frac{m \cdot P_o}{m+1} \tag{8}$$

$$P_{M_{n=m}} = \frac{P_o}{m+1}. \tag{9}$$

The variable n establishes the position of the voltage module in the stack. The efficiency definition proposed herein supposes each voltage module has a η_n conversion efficiency. Thus, system efficiency is given as

$$\eta_T = \frac{P_o}{P_o + \sum_{k=1}^{m} \Delta P_{M_k}}, \tag{10}$$

where ΔP_{Mn} represents the losses associated with the respective voltage module M_n and is given by

TABLE II
Comparison Of The Current And Voltage Stresses For The Topologies Of Groups 1, 2 and 3

Characteristic	Group 1		Group 2		Group 3	
	Basic cell	Cúk	SEPIC 1	Zeta 1	SEPIC 2	Zeta 2
Voltage stress on the switch/diode (V_{Sn}/V_o)	$\frac{D^{n-1}}{(1-D)^n\cdot\sum_{k=0}^{m}\left(\frac{D}{1-D}\right)^k}$		$\frac{(2D-1)^{n-1}}{(1-D)^n\cdot\sum_{k=0}^{m}\left(\frac{2D-1}{1-D}\right)^k}$		$\frac{D^{n-1}}{(1-2D)^n\cdot\sum_{k=0}^{m}\left(\frac{D}{1-2D}\right)^k}$	
Voltage stress on the switch/diode (V_{Sn}/V_i)	$\frac{D^{n-1}}{(1-D)^n}$		$\frac{(2D-1)^{n-1}}{(1-D)^n}$		$\frac{D^{n-1}}{(1-2D)^n}$	
Average current through switch ($I_{Sn,avg}/I_o$)	$\frac{D}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$		$\frac{2D-1}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\frac{D}{1-2D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Average current through diode ($I_{Dn,avg}/I_o$)	$\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$		$\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Rms current through switch ($I_{Sn,rms}/I_o$)	$\frac{\sqrt{D}}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$		$\frac{\sqrt{D}}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\frac{\sqrt{D}}{1-2D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Rms current through diode ($I_{Dn,rms}/I_o$)	$\frac{\sqrt{1-D}}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$		$\frac{\sqrt{1-D}}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\frac{\sqrt{1-D}}{1-2D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Average current through inductor $L_{n,1}$ ($I_{Ln1,avg}/I_o$)	$\frac{1}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$	$\frac{D}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$	$\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Average current through inductor $L_{n,2}$ ($I_{Ln2,avg}/I_o$)	—	$\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k$	$\frac{D}{1-D}\cdot\sum_{k=0}^{m-n}\left(\frac{2D-1}{1-D}\right)^k$		$\frac{D}{1-2D}\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-2D}\right)^k$	
Average voltage over the capacitor C_n (V_{Cn}/V_i)	—	$\frac{D^{n-1}}{(1-D)^n}$	$\left(\frac{2D-1}{1-D}\right)^{n-1}$	$\frac{D\cdot(2D-1)^{n-1}}{(1-D)^n}$	$\frac{D^{n-1}\cdot(1-D)}{(1-2D)^n}$	$\left(\frac{D}{1-2D}\right)^n$

$$\Delta P_{M_n}=\frac{P_{M_n}\cdot(1-\eta_n)}{\eta_n}. \tag{11}$$

The generalized system efficiency for the topology with m modules can be calculated substituting (7) and (11) into (10):

$$\eta_T=\frac{1}{1+\frac{1}{m+1}\cdot\left[n\cdot\frac{(1-\eta_1)}{\eta_1}+(n-1)\cdot\frac{(1-\eta_2)}{\eta_2}+\ldots+2\cdot\frac{(1-\eta_{n-1})}{\eta_{n-1}}+\frac{(1-\eta_n)}{\eta_n}\right]},\ \text{for } m\geq 2. \tag{12}$$

B. Inductors' Current Ripple

The inductances from all modules are chosen to ensure the continuous conduction mode (CCM) for a range of output power. The boundary between the continuous and discontinuous conduction mode (DCM) happens when the current ripple in any inductor (L_n) is equal to $2I_{Ln,avg}$. The procedure for calculation of the inductances is performed based on the converter shown in Figure 2.b with m stacked commutation cells. However, it can be applied to all proposed topologies. The minimum inductance that ensures the operation of the converter in CCM is given by

$$L_n=\frac{V_{Co,n-1}\cdot D}{2\cdot I_{Ln,avg\_\min}\cdot f_s}, \tag{13}$$

where $V_{Co,n-1}$ is the average voltage over the capacitor n-1 of the stack and $n\in\{1,2,...,m\}$.

Equation (13) can be described as a function of the input voltage V_i and minimum output power P_{o_min}, as shown in (14). It can be observed that the inductance values are larger for the inductors closer to the load (step-up side). However, the volume of the magnetics closer to the load tends to decrease, since the current stresses are lower and the volume is proportional to the product $L_n.I_{Ln,avg}^2$.

The switching frequency and the minimum output power should be chosen with quite criterion, since the appropriate choice of these parameters can reduce the weight and volume of the inductors.

$$L_n=\frac{V_i^2\cdot D^n\cdot(1-D)^{2-n}\cdot\sum_{k=0}^{m}\left(\frac{D}{1-D}\right)^k}{2\cdot P_{o\_\min}\cdot f_s\cdot\sum_{k=0}^{m-n}\left(\frac{D}{1-D}\right)^k}. \tag{14}$$

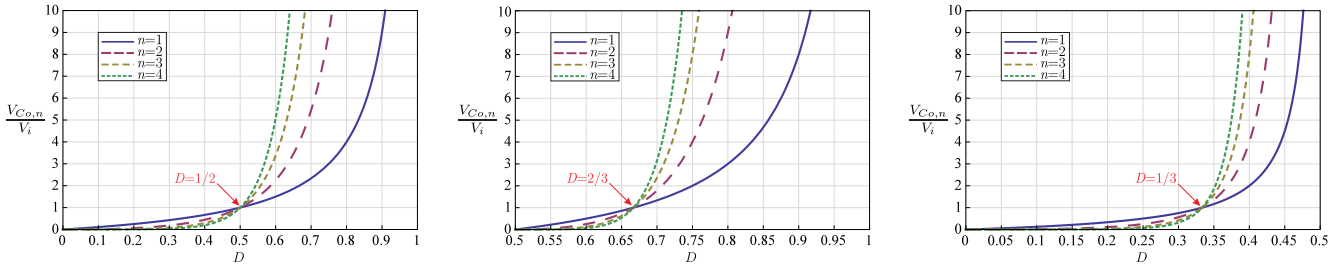
For the converter operating with optimal duty-cycle (D = 0.5), equation (14) is reduced to

$$L_n=\frac{V_i^2\cdot(m+1)}{8\cdot P_{o\_\min}\cdot f_s\cdot(m-n+1)}. \tag{15}$$

C. Capacitors' Voltage Ripple

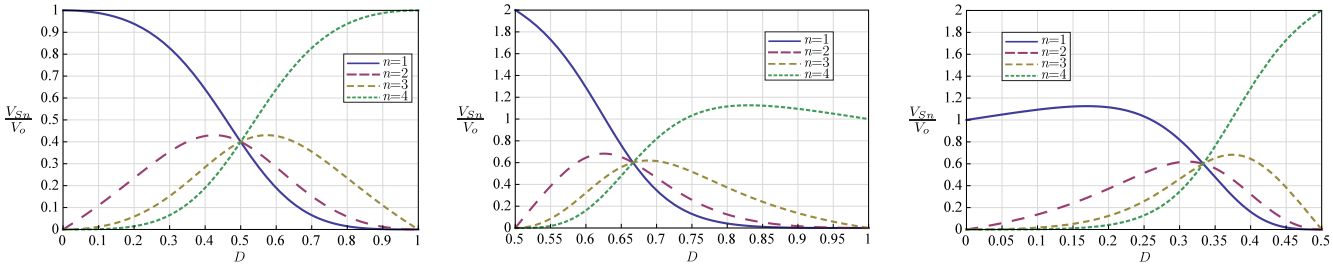
The capacitors can be defined in two ways: the same value of capacitances or the same ripple voltage for all capacitors in the stack. If modularity is desired, the first option is the most recommended.

In addition, equal capacitances ensure the voltage balance during the startup. Since the current stresses on the capacitors are unbalanced as well, the capacitor closer to the input voltage source always has the higher voltage ripple. Therefore, for the first option of capacitors choice, all capacitances are defined from the capacitance $C_{o,1}$. On analyzing



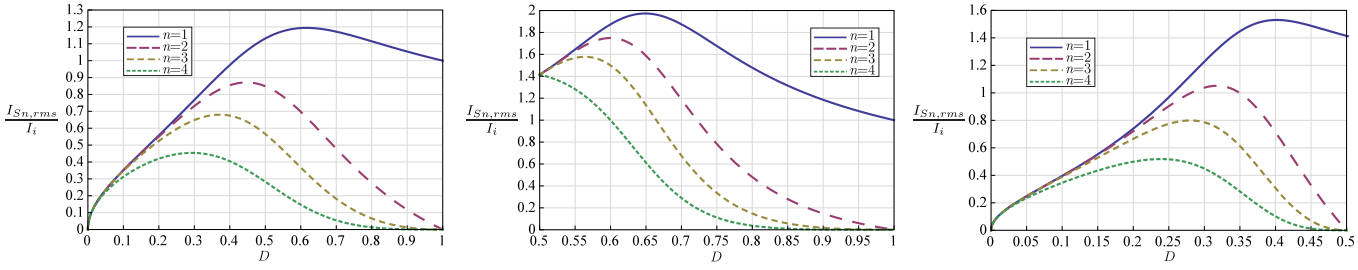
(a) (b) (c)

Fig. 6. Voltage across the stacked capacitors parametrized as a function of the input voltage V_i considering m = 4: (a) Topologies of group 1; (b) Topologies of group 2; (c) Topologies of group 3.



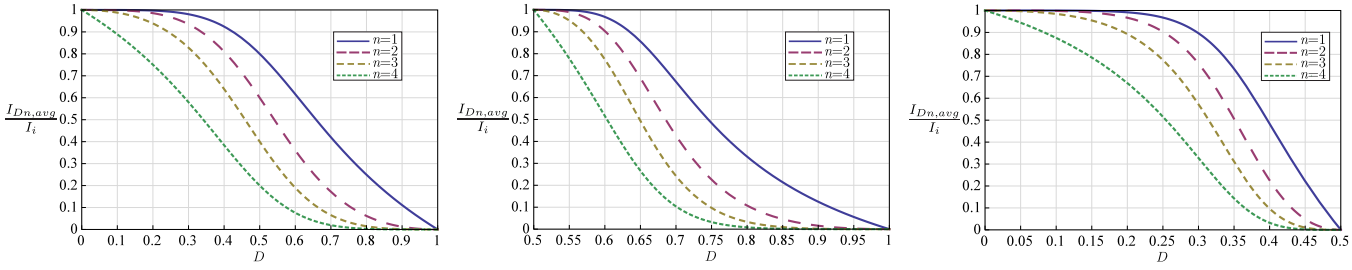
(a) (b) (c)

Fig. 7. Maximum voltage across the switches and diodes parametrized as a function of the output voltage V_o considering m = 4: (a) Topologies of group 1; (b) Topologies of group 2; (c) Topologies of group 3.



(a) (b) (c)

Fig. 8. Rms current in the switches parametrized as a function of the input current I_i considering m = 4: (a) Topologies of group 1; (b) Topologies of group 2; (c) Topologies of group 3.



(a) (b) (c)

Fig. 9. Average current in the diodes parametrized as a function of the input current I_i considering m = 4: (a) Topologies of group 1; (b) Topologies of group 2; (c) Topologies of group 3.

the time interval 0 – DT_s, the equation that defines any capacitance in the stack is given by

$$C_{o,n} = \frac{I_{Co,n} \cdot D}{\Delta V_{Co,n} \cdot f_s}, \tag{16}$$

where $I_{Co,n}$ represents the current through the capacitor $C_{o,n}$ during the time interval 0 – DT_s and it is defined as

$$I_{Co,n} = I_o \cdot \left[1 + \frac{1}{1-D} \cdot \sum_{k=0}^{m-(n+1)} \left(\frac{D}{1-D}\right)^k\right], \text{ with n} \in \{1,2,...,\text{m-1}\}. \tag{17}$$

When the converter operates with optimal duty-cycle (D = 0.5), equation (17) will be reduced to

$$C_{o,n} = \frac{I_o \cdot \left(m - n + \frac{1}{2}\right)}{\Delta V_{Co,n} \cdot f_s}, \text{with n} \in \{1,2,...,\text{m}\}. \tag{18}$$

The rms value of the current in all capacitors for the converter operating with optimal duty-cycle is defined by

$$I_{Con,rms} = 2I_o \cdot \left(m - n + \frac{1}{2}\right), \text{with n} \in \{1,2,...,\text{m}\}. \tag{19}$$

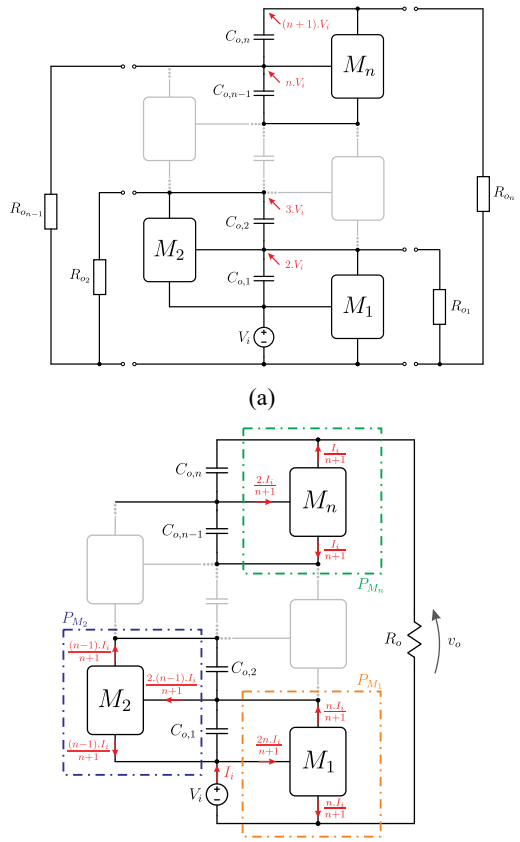


Fig. 10. Steady state analysis of the generalized equivalent circuit of the proposed converters: (a) Possibility of load connection; (b) Current distribution.

VI. SIMPLIFIED DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

In order to verify the generalized theoretical analysis developed in the previous section, a design example was performed and a 1-kW prototype was built and tested. A study case with three stacked basic commutation cells (m = 3) was chosen for experimental verification. The power circuit is shown in Figure 11 and it is similar that proposed in Figure 2.b. The operation point set in the prototype was the optimal duty-cycle (D = 0.5), which ensures a balance voltage across the stacked capacitors and reduces the voltage

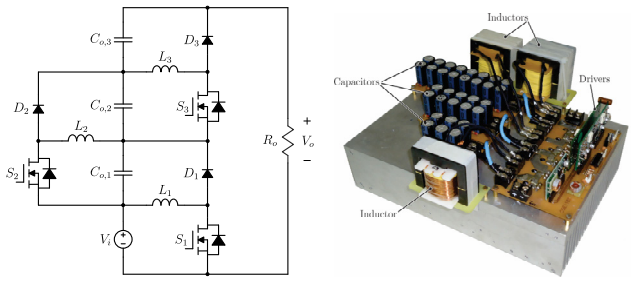


Fig. 11. DC-DC converter based on the stacking three conventional buck-boost converters and implemented 1 kW stacked DC-DC converter hardware prototype.

and current stresses on the power semiconductors. Therefore, the generic expressions described in Table II are simplified and the results are written in Table III. These expressions are used to calculate the voltage and current stresses on the power semiconductors, capacitors and inductors for the prototype. The converter specifications are described in Table IV. All of the selected components used in the prototype are shown in Table IV. Figure 11 shows the 1-kW hardware prototype.

A. Experimental Results

The experimental results present herein are relevant voltage and current waveforms for steady state operation of the converter, which verify the proposed structure and analysis. The results are shown in Figures 12–13 and they were obtained by the converter operating at rated power. Figure 12.a shows the output voltage and the voltages across the capacitors $C_{o,1}$, $C_{o,2}$ and $C_{o,3}$. It is observed in Figure 12.a the natural voltage balance in the stacked capacitors, when the converter operates with duty-cycle equal to 0.5. Figure 12.b shows the current waveforms through the inductors L_1, L_2 and L_3. The average values obtained were: $I_{L1,avg}$ = 15 A, $I_{L2,avg}$ = 10 A and $I_{L3,avg}$ = 5 A, which match with theoretical analysis. Therefore, it is possible to confirm the unbalanced current distribution in the converter, where the current stresses are higher in the inductors closer to the input voltage source, as mentioned in previous sections. The input i_i and output i_o current are shown in Figure 12.c. As a natural consequence of the stacking of buck-boost structures, the input current is pulsating. This problem can be avoided if a LC filter is added in series with the power supply.

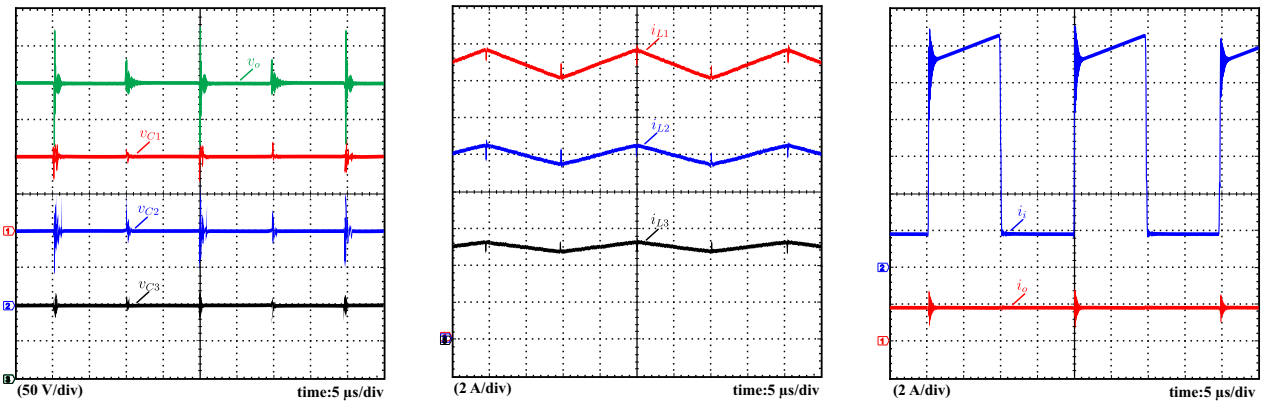
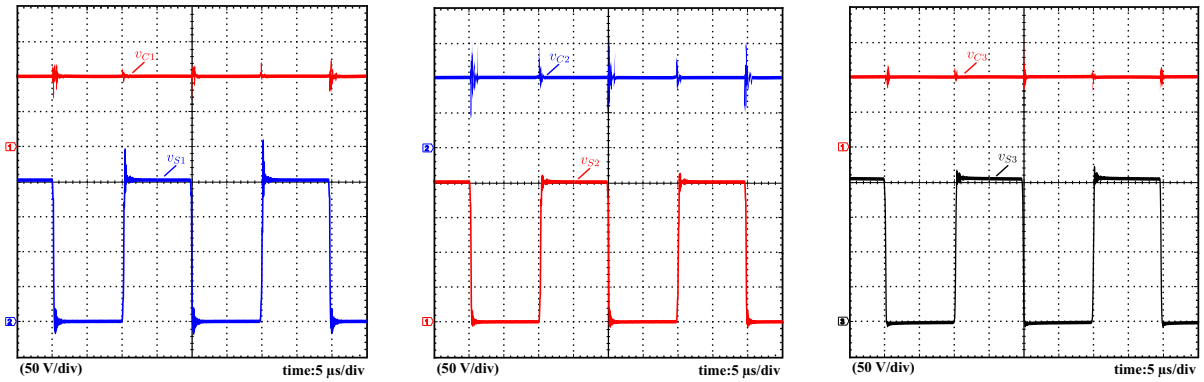


Fig. 12. Experimental results: (a) Output voltage v_o and capacitor voltages $v_{Co,n}$; (b) Inductor currents i_{Ln}; (c) Input and output current.



(a) (b) (c)

Fig. 13. Experimental results: (a) Capacitor voltage v_{C1} and switch voltage v_{S1}; (b) Capacitor voltage v_{C2} and switch voltage v_{S2}; (c) Capacitor voltage v_{C3} and switch voltage v_{S3}.

TABLE III
Simplified Expressions Used To Calculate Voltage And Current Stresses On The Components Considering *m* = 3

Characteristic	Voltage and current stresses on the components considering generic duty-cycle and $m = 3$.			Generalized expressions considering $D = 0.5$
Static Gain	____	____	____	$G_v = \frac{V_o}{V_i} = m+1$
Voltage in each stacked capacitor	$V_{Co,1} = V_i \cdot \frac{D}{1-D}$	$V_{Co,2} = V_i \cdot \left(\frac{D}{1-D}\right)^2$	$V_{Co,3} = V_i \cdot \left(\frac{D}{1-D}\right)^3$	$V_{Co,n} = V_i = \frac{V_o}{m+1}$
Voltage stress in each switch/diode	$V_{S1} = V_i \cdot \frac{1}{1-D}$	$V_{S2} = V_i \cdot \frac{D}{(1-D)^2}$	$V_{S3} = V_i \cdot \frac{D^2}{(1-D)^3}$	$V_{Sn} = 2 \cdot V_i = \frac{2 \cdot V_o}{m+1}$
Rms current through each switch	$I_{S1,\text{rms}} = I_o \cdot \frac{\sqrt{D} \cdot (1-D+D^2)}{(1-D)^3}$	$I_{S2,\text{rms}} = I_o \cdot \frac{\sqrt{D}}{(1-D)^2}$	$I_{S3,\text{rms}} = I_o \cdot \frac{\sqrt{D}}{1-D}$	$I_{Sn,\text{rms}} = \sqrt{2} \cdot I_o \cdot (m-n+1)$
Average current through each diode	$I_{D1,avg} = I_o \cdot \frac{1-D+D^2}{(1-D)^2}$	$I_{D2,avg} = I_o \cdot \frac{1}{1-D}$	$I_{D3,avg} = I_o$	$I_{Dn,avg} = I_o \cdot (m-n+1)$
Average current through each inductor	$I_{L1,avg} = I_o \cdot \frac{1-D+D^2}{(1-D)^3}$	$I_{L2,avg} = I_o \cdot \frac{1}{(1-D)^2}$	$I_{L3,avg} = I_o \cdot \frac{1}{1-D}$	$I_{Ln,avg} = 2 \cdot I_o \cdot (m-n+1)$
Current ripple in each inductor	____	____	____	$\Delta I_{Ln} = \frac{V_i}{2 \cdot L_n \cdot f_s}$

The waveforms in Figures 13.a, 13.b and 13.c show the voltages across the stacked capacitors $C_{o,n}$ and the switches S_n. All capacitor voltages are balanced and equal to the input voltage. It should be noticed that the voltage across the power semiconductors (v_{Sn} and v_{Dn}) is clamped with a maximum value given by the sum of the voltages from the capacitors $C_{o,n}$ and $C_{o,n-1}$, since the converter operates with a duty-cycle of 50%.

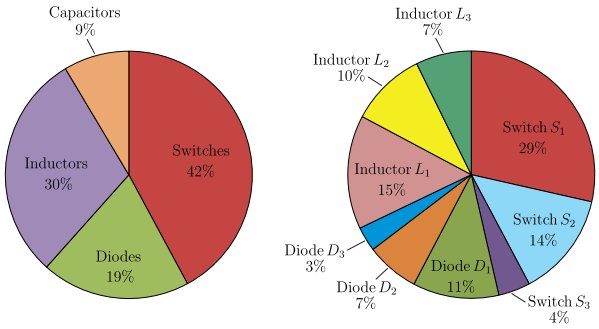
B. Power Loss Analysis and Efficiency

In order to verify the losses distribution in the designed converter, a power loss analysis in all components was performed. In this analysis, the switching and conduction losses of the switches, the conduction losses of the diodes, the core and winding losses of the inductors and the conduction losses of the capacitors were estimated based on manufacturers' datasheets. Figure 14.a shows the theoretical loss distribution at rated power. In this condition, it can be observed that the losses in the switches are more significant, representing 42% of the total power losses. The theoretical total losses were 77.62 W, resulting in a theoretical efficiency of 92.8%. The distribution of losses per component is seen in Figure 14.b. As expected, the losses are higher in the components closer to the input voltage source, components S_1, L_1 and D_1.

Lastly, Figure 15 shows the experimental efficiency curve for the converter as a function of the output power. The measurements were obtained using the digital wattmeter Yokogawa WT500. The converter reaches the maximum efficiency of 93.65% close to 440 W. The measured efficiency of the converter operating under nominal conditions i.e., 1 kW output power, was 91.8%. The experimental verification corroborated with the theoretical analysis presented. The moderate efficiency can be justified due to the fact that the experimental verification was intended only to validate the theoretical analysis presented. The efficiency can be improved if the main focus is the optimization of the converter. This could be obtained using new semiconductors and improving the inductors design.

TABLE IV
Converter Specifications

Specification	Value
Output Power (P_o)	1 kW
Output Voltage (V_o)	400 V
Input Voltage (V_i)	100 V
Switching frequency (f_s)	50 kHz
Diodes D_1, D_2 and D_3	STTH3003CW
Switches S_1, S_2 and S_3	IRFP264
Capacitors $C_{o,1}$, $C_{o,2}$ and $C_{o,3}$	[25, 50, 75] µF
Inductors L_1, L_2 and L_3	[0.667, 1.0, 2.0] mH



(a) (b)

Fig. 14. Theoretical loss distribution for the converter operating at rated power.

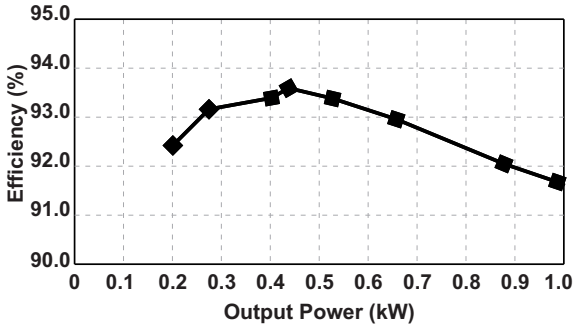


Fig. 15. Efficiency curve as a function of the output power.

VII. PERFORMANCE COMPARISON

This section presents a performance comparison between the proposed generalized topology shown in Figure 2.b and other generalized structures of non-isolated high step-up DC-DC converters proposed in the literature. Voltage gain, voltage stress across the switches and diodes, total device number and possibility of bidirectional power flow are compared and shown in Table V. To present an appropriate comparison, as example, the voltage gain and duty-cycle are set to 14 and 0.5, respectively, for all of analyzed topologies. Consequently, the value of m (variable that defines the number of stages) is different for each topology.

The voltage stress on the switches and diodes of the proposed converter is relatively lower when compared with the converters proposed in [31]-[32]. The voltage stress on the diodes of the converter in [31] is twice as large as that of the power semiconductors of the proposed topologies in this paper. In comparison with the converter in [32], the voltage stress on the switches and diodes is three times higher than in the proposed converter shown in Figure 2.b. The voltage stresses on the power semiconductors in the other analyzed converters shown in Table V are similar to the proposed topologies in this paper. In addition, in the proposed structures in [29]-[32], some capacitors are subjected to high voltage levels and, therefore, it is necessary the use of higher voltage rated capacitors. In the converter shown in Figure 2.b, all the capacitors are under low voltage stresses, which is equal to output voltage divided by the number of cells. If the proposed converters in this paper operate with optimal duty-cycle, the voltage stresses on the power semiconductors and capacitors will decrease when number of cells m increases.

As main drawback, the proposed converters employ a larger total device number compared to others converters (when operating with optimal duty-cycle value). However, for a low number of stacked cells m, high voltage gain can also be obtained if the proposed converters operate with duty-cycle greater than their respective optimal values. For to achieve voltage gain of 14 with duty-cycle 0.5, the number of stacked cells needed for the proposed converter shown in Figure 2.b is equal to 13. The number of cells m decreases from 13 to 6 if the duty-cycle D increases from 0.5 to 0.55. Thus, to achieve the same voltage gain, the total number devices of the proposed converters may be reduced by the increasing the duty-cycle, which makes the converters more competitive in terms of cost and volume. Furthermore, with a lower total number devices, the conduction losses are reduced and, consequently, the efficiency is improved. On the other hand, the voltage stresses on the switches will be unbalanced and, consequently, the use of higher voltage rated MOSFET can be needed. Other possible use of these topologies is in applications that need several output voltage levels, in which the load can be connected to one or more capacitors of the stack. Furthermore, the proposed converters can be used in applications that require bidirectional power flow. Among the competitors, only the proposed converter in [21] has these features.

VIII. CONCLUSIONS

In this paper, a study of stacked DC-DC converters with high step-up gain was presented. The proposed converters are obtained from the stacking conventional buck-boost structures. The main features of the proposed converters are as follow: possibility of modularity, simple control implementation, possibility of bidirectional power flow and natural voltage balance across the stacked capacitors, which provides low voltage stresses on the power semiconductors when the converters operate with the optimal duty-cycle value. Thus, lower voltage rated MOSFET with low $R_{DS\text{-}ON}$ may be used, which reduces the conduction losses and, consequently, improves the overall efficiency. In addition, the proposed converters have potential to be used as DC bus to provide one or several output voltage levels with self-balancing, in which the load may be connected to one or more capacitors of the stack.

As a contribution of this paper, a theoretical analysis of the proposed converters for a generic number of stacked cells was presented. The theoretical analysis approached: static gain, voltage and current stresses on the active and passive

TABLE V
Comparison Between Proposed Generalized Topology Shown In Figure 2.b And Other Generalized Structures Of Non-isolated High Step-up DC-DC Converters Proposed In The Literature

Characteristic	Proposed topology (Fig. 2*b*)	Proposed topology in [29]	Proposed topology in [30]	Proposed topology in [31]	Proposed topology in [32]	Proposed topology in [21]
Static Gain (M_V)	$\sum_{k=0}^{m}\left(\frac{D}{1-D}\right)^{k}$	$\frac{m+1}{1-D}$	$\begin{cases}\frac{(m+1)-D}{1-D}, & m \text{ even}\\ \frac{m+D}{1-D}, & m \text{ odd}\end{cases}$	$\frac{2\cdot m}{1-D}$	$\frac{D\cdot(2+n)+m\cdot(1+n)+n}{1-D}$	$\frac{m}{1-D}$
Voltage stress on the switches	$\frac{2\cdot V_o}{m+1}$	$\frac{V_o}{m+1}$	$\frac{V_o}{m+D}$	$\frac{V_o}{2\cdot m}$	$\frac{V_o\cdot(1+M_V)}{M_V\cdot(m+D+1)}$	$\frac{V_o}{m}$
Voltage stress on the diodes	$\frac{2\cdot V_o}{m+1}$	$\frac{V_o}{m+1}$	$\frac{V_o}{m+D}$	$\frac{V_o}{m}$	$\frac{V_o\cdot(1+M_V)}{M_V\cdot(m+D+1)}$	$\frac{V_o}{m}$
Total device number	$4\cdot m$	$4\cdot m+4$	$4\cdot m+4$	$4\cdot m+5$	$4\cdot m+18$	$6\cdot m+2$
Several output voltage levels	*Yes*	*No*	*No*	*No*	*No*	*Yes*
Possibility of bidirectional power flow	*Yes*	*No*	*No*	*No*	*No*	*Yes*

components, power flow analysis, inductors' current ripple analysis and capacitors' voltage ripple analysis. Furthermore, a brief theoretical analysis considering the operation of the converters with the optimal duty-cycle value was described.

In order to verify the theoretical analysis developed in this paper, a 1 kW prototype was designed and built, and experimental results were obtained. The results have demonstrated the performance and feasibility of the proposed step-up stacked DC-DC converters.

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