A FRONT-END BRIDGELESS POWER FACTOR CORRECTOR FOR ELECTRIC VEHICLE BATTERY CHARGERS

Jefferson Carlos Fischer[1], Juliana Andressa da Silva[2], Yales Rômulo de Novaes[1], Sérgio Vidal Garcia Oliveira[1,2]

[1]Universidade do Estado de Santa Catarina, Joinville - SC, Brazil
[2]Universidade Regional de Blumenau, Blumenau - SC, Brazil
e-mail: fischer.jcf@gmail.com, julianaa.eng@gmail.com, yales.novaes@udesc.br, sergio_vidal@ieee.org

***Abstract* – In this paper, a bridgeless power factor corrector converter is suggested for electric vehicle battery chargers. The converter is applicable as a front-end stage for residential charging, i.e. automotive level 1. It is presented a steady state operation analysis for the proposed converter. It operates in current continuous conduction mode controlled by a voltage outer loop and a current inner loop control strategy. Experimental results were performed for a 1 kW prototype, considering 220 V grid voltage, 400 V dc output voltage, 70 kHz switching frequency, and the control system implemented by the UCC28070. The experimental results are satisfactory, which demonstrate a peak efficiency of 98.4% at half load, and features high efficiency from light load to full load. Additionally, the input current THD is less than 5% from half to full load and the power factor is higher than 0.99 from half to full load.**

***Keywords* – AC-DC Converter, Battery Chargers, Bridgeless Boost Converter, Electric Vehicle, Power Factor Corrector.**

NOMENCLATURE

L	Boost inductance.
V_{in}	Grid voltage.
ΔI_L	Inductor ripple current.
f_s	Switching frequency.
P_{out}	Output power.
f_{line}	Line frequency.
V_{out}	Output voltage.
ΔV	Output ripple voltage.
D	Duty cycle.
K_{VFF}	Feed-forward voltage factor.
$L_{1,2}$	Inductors $L_{1,2}$.
$D_{1,2}$	SiC Schottky diodes $D_{1,2}$.
$D_{a,b}$	Ultrafast diodes $D_{a,b}$.
$Q_{1,2}$	Switches $Q_{1,2}$.
$D_{q1,2}$	Intrinsic body diodes of $Q_{1,2}$.
C_o	Output filter capacitor.
$V_{g1,2}$	Gating signals for $Q_{1,2}$.
$I_{L1,2}$	Current on inductors $L_{1,2}$.
$I_{D1,2}$	Current on diodes $D_{1,2}$.
$I_{Da,b}$	Current on diodes $D_{a,b}$.
$I_{Dq1,2}$	Currents on intrinsic body diodes of $Q_{1,2}$.
$I_{Q1,2}$	Currents on switches $Q_{1,2}$.
V_{ret}	Grid rectified voltage.
V_{ref}	Reference's voltage.
I_{ref}	Reference's current.
$C_{i(s)}$	Current compensator.
$C_{v(s)}$	Voltage compensator.
K_{pwm}	PWM modulator gain.
$G_{i(s)}$	Input current to control transfer function.
$G_{v(s)}$	Output voltage to input current transfer function.
H_i	Current sensor.
H_v	Voltage sensor.

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I. INTRODUCTION

There is growing interest in electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) technologies because of their reduced fuel usage and greenhouse emissions [1], [2]. The technological and financial viability that EVs and PHEVs have been receiving are contributing each year more to the popularization of these means of transportation, in order to make vehicles more efficient [3]. Currently, in order to increase the commercialization of these types of vehicles, it is focus of study mainly the technology of energy accumulators, e.g. batteries, and the features of battery chargers. The battery chargers applied to these vehicles are very important for the development of EVs and PHEVs. The charging time and the life of the battery are related to the characteristics of these devices. A battery charger must be efficient and reliable, with high power density, low cost, and reduced weight and volume [1].

A variety of architectures and topologies has been proposed for the battery chargers applied to electric vehicles. However, due the high ripple of low frequency on the output current, the single stage composed exclusively only by an AC-DC converter is only suitable for lead-acid batteries [4]. On the other hand, a double stage composed by AC-DC and DC-DC converters allows the rejection of the low frequency ripple. Therefore, the approach of double stage like AC-DC converters combined with DC-DC converters is preferable for battery chargers of electric vehicles, where the power levels are relatively high and the lithium-ion batteries require low ripple of voltage, which are used as main system of energy storage [5].

The battery chargers are categorized fundamentally into 3 types: on-board, off-board, or recharging stations. In addition, a relevant factor to consider the type of charger is

its power level. Embedded chargers limit high powers due to weight, volume, and cost issues [6], [7]. The types of chargers mentioned may have an unidirectional or bidirectional power flow. In the case of unidirectional chargers, the power flow is in the direction from the power supply to the energy accumulators. These tend to reduce the battery degradation [8], [9]. Considering bidirectional chargers, the power flow can be either from the power supply to the batteries, or vice versa.

The power levels of the chargers reflect in power, charging time, charger location, cost and effect on the grid. Table I presents the charging power levels. Level 1 is the starting point in the development and dissemination of EVs and PHEVs technology. This is the slowest method for charging the accumulators. In relation to level 1, the rated powers in level 2 are greater and the charging times consequently are reduced. Level 3 is used for fast charges, for commercial use similar to a conventional fuel station. This level covers the largest powers of the chargers. Level 3 chargers are also called recharging stations. The main drawback is the installation cost of these recharging stations.

TABLE I
Charging Power Levels (Based on [1])

Power level	Charger location	Typical use	Rated power
Level 1 120 V ac (US) 230 V ac (EU)	On-board 1-phase	Charging at home or office	Up to 3 kW
Level 2 240 V ac (US) 400 V ac (EU)	On-board 1- or 3-phase	Charging at private or public outlets	Up to 20 kW
Level 3 208-600 V ac or dc	Off-board 3- phase	Commercial, similar to a conventional fuel station	Up to 100 kW

According to the Electric Power Research Institute (EPRI), many EV owners expect to charge their vehicles at home overnight. For this reason, power levels 1 and 2 will be the primary options [10]. In this context, the present paper has proposed to present a level 1 bridgeless boost power factor corrector AC-DC converter applied in electric vehicle battery chargers. In order to meet the power level 1, the power flow is unidirectional and the converter has 1 kW of power. This choice was made fundamentally based on topology comparison as shown in Table II.

The converter proposed in this paper refers to phase shifted semi-bridgeless PFC boost converter from Table II. In comparison with a conventional PFC boost converter, the proposed converter features reduced EMI, lower value of input ripple, a reduced magnetic size, and allows greater efficiencies. Therefore, the main focus was selecting a converter that would allow a higher efficiency. Additionally to the power factor corrector (PFC) topologies shown in Table II, some other PFC topologies derived from conventional boost converter have also been studied [11]-[13]. Based on the proposed converter design, the experimental results of the built prototype are collected and evaluated.

II. PROPOSED BOOST TOPOLOGY

A. Bridgeless Boost PFC AC-DC Converter

The proposed boost topology refers to the bridgeless boost PFC AC-DC converter, as shown in Figure 1, an already existing topology as presented in [14], [15]. Comparing with conventional boost topology, the main difference is that the proposed topology eliminates the traditional rectifier bridge, and uses switches Q_1 and Q_2 to replace the two rectifier diodes of the rectifier leg. There are two additional diodes D_a and D_b to connect the ground to the input, which makes the input line voltage referenced to ground.

TABLE II
Topology Comparison as Presented in [15]

Topology	Conventional PFC boost Converter	Phase shifted semi-bridgeless PFC boost	Interleaved PFC boost converter	Bridgeless interleaved PFC boost	Bridgeless interleaved resonant PFC converter
Power Rating	< 1 kW	< 3.5 kW	< 3.5 kW	> 5 kW	> 5 kW
EMI/ Noise	Poor	Fair	Fair	Best	Best
Capacitor Ripple	High	Medium	Low	Low	Low
Input Ripple	High	Medium	Low	Low	Low
Magnetic Size	Large	Medium	Small	Small	Small
Driver	2 LS	2 LS	2 LS	2 LS	2 LS+2HS
Efficiency	Poor	Best	Fair	Best	Fair
Cost	Low	Medium	Medium	High	Highest

The advantage of using D_a and D_b diodes is that the return current for the power supply passing through these components produces lower losses in D_a and D_b diodes if compared to the return current for the power supply passing exclusively through Q_1/D_{q1} and L_1 or Q_2/D_{q2} and L_2, where the conduction losses are greater in these components. Therefore, this arrangement allows an increase of efficiency for converter. Additionally, the signals from the switches are 180° out of phase.

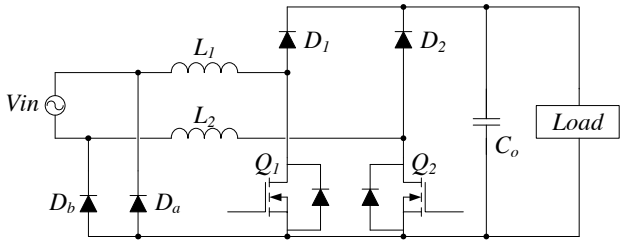

Fig. 1. Bridgeless boost PFC AC-DC converter.

B. Proposed Boost Topology Operation Analysis

In relation to the circuit operation, to analyze the operation steps of converter shown in Figure 1, the input voltage cycle is shared into positive and negative half-cycles. The detailed operation of the circuit depends on the duty

cycle D. The analysis of the positive half-cycle is realized for $D > 0.5$ and $D < 0.5$ [16]. It is assumed that all devices from circuit are ideal.

1) Positive half-cycle operation and analysis for D > 0.5: The detailed operation of the proposed converter depends on duty cycle. During each half-cycle, the duty cycle of the converter is greater than 0.5 (when the input voltage is less than half the output voltage) or less than 0.5 (when the input voltage is greater than half the output voltage). Waveforms of proposed converter during operation in the positive half-cycle with the duty cycle $D > 0.5$ are shown in Figure 2.

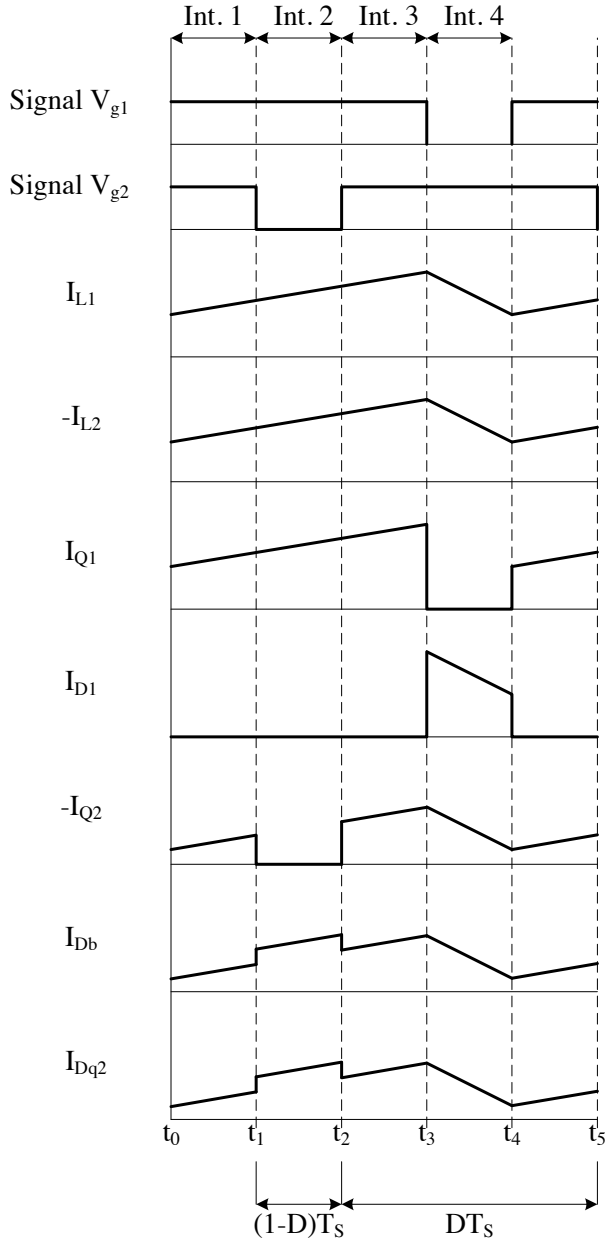

Fig. 2. Waveforms of proposed converter for $D > 0.5$.

In order to simplify the analysis, it's assumed that the current is divided equally in the diodes D_1 and D_2, in the intrinsic diodes D_{q1} and D_{q2} of the MOSFETs Q_1 e Q_2, and properly in the MOSFETs. The intervals of operation are also shown. During the positive half-cycle, the circuit's operation can be divided into four operation intervals:

Interval 1 (t_0 - t_1): at t_0, the switches Q_1 and Q_2 are in conduction. During this time, the currents in the inductances L_1 and L_2 increase linearly and as a consequence energy is stored in these inductors. The energy stored in the capacitor C_o is transferred to the load. The return current is then divided among the components D_b, D_{q2} and Q_2.

Interval 2 (t_1 - t_2): at t_1, only switch Q_1 is in conduction mode. During this time, the currents in the inductances L_1 and L_2 continue to increase linearly and energy is stored in these inductors. The energy stored in the capacitor C_o is transferred to the load. The return current is then divided between the components D_b and D_{q2}.

Interval 3 (t_2 - t_3): at t_2, switches Q_1 and Q_2 are in conduction again, and instant 1 is repeated. During this time, the currents in the inductances L_1 and L_2 increase linearly and as a consequence energy is stored in these inductors. The energy stored in the capacitor C_o is transferred to the load. The return current is again divided among the components D_b, D_{q2} and Q_2.

Interval 4 (t_3 - t_4): at t_3, only switch Q_2 is in conduction mode. During this time, the energy stored in the inductors L_1 and L_2 is released to the output through the components L_1, D_1, partially Q_2, D_{q2}, L_2 and D_b.

2) Positive half-cycle operation and analysis for D < 0.5: The waveforms of the proposed converter for $D < 0.5$ are shown in Figure 3. The intervals of operation are also shown.

Interval 1 (t_0 - t_1): at t_0, the switches Q_1 and Q_2 are not in conduction mode. During this time, the energy stored in the inductors L_1 and L_2 is released to the output through the components L_1, D_1, partially D_{q2}, L_2 and D_b.

Interval 2 (t_1 - t_2): at t_1, only switch Q_1 is in conduction mode. During this time, the current in the inductors L_1 and L_2 continues to increase linearly and energy is stored in these inductors. The energy stored in the capacitor C_o is transferred to the load. The return current is then divided only between components D_b and D_{q2}.

Interval 3 (t_2 - t_3): at t_2, the switches Q_1 and Q_2 are not in conduction again. During this time, the current in the inductors L_1 and L_2 decreases linearly, and the energy in these inductors is released. The energy stored in L_1 and L_2 is released to the output through the components L_1, D_1, partially D_{q2}, L_2 and D_b.

Interval 4 (t_3 - t_4): at t_3, only switch Q_2 is in conduction mode. During this interval, the energy stored in the inductors L_1 and L_2 is released to the output through the components L_1, D_1, partially Q_2, D_{q2}, L_2 and D_b.

The operation of the converter during the negative half-cycle of the input voltage is similar to the operation during the positive half-cycle of the input voltage.

III. CONTROL STRATEGY

For the bridgeless boost PFC AC-DC converter it is proposed the application of the control technique with instantaneous average values. The control circuit must act in order to maintain the operation of the system according to the specific features desired. The current loop is responsible for maintaining the input current with the same shape and in phase with the sinusoidal input voltage. The current loop is designed following the application review from Texas Instruments [17]. The designed controllers are of PI (proportional-integral) with filter type. On the other hand, the voltage loop is responsible for maintaining the output voltage within the pre-set limits, thus allowing the converter to respond for any load variations at the output. The voltage loop is also designed following the application review from Texas Instruments [17]. The designed controllers are of PI (proportional-integral) with filter type.

The proposed converter makes the use of the dedicated IC UCC28070 [18]. Figure 4 shows the internal control structure of IC UCC28070 connected to converter, while in Figure 5 is shown in detail the closed loop control in block diagram. The UCC28070, interleaved PFC controller in continuous conduction mode (CCM), is an advanced power factor correction device that integrates two pulse width modulators (PWMs) operating 180° out of phase. Interleaved PWM operation generates reduction in the ripple of the input current.

In the following is thoroughly explained each of the elements that compose the control circuit shown in Figure 4.

1) Transformer: used to obtain a sample of the input voltage waveform from the grid. Model: Hayonik 1 A, input 0 V-127 V-220 V, output 24 V+24 V.

2) Hall sensor: is a Hall effect current sensor, positioned in series with the inductors L_1 and L_2. Model: LEM LTSR 15-NP.

3) Resistive divider: its function is to collect the sample of the output voltage from the power circuit. The sample of the output voltage must be set according to the value of the voltage reference of voltage compensator.

4) Voltage rectifier: connected to the secondary of transformer in order to set the grid sample signal.

5) Subtractor amplifiers: circuit responsible for eliminating the intrinsic 2.5 V offset from the current Hall sensor.

6) Feed-forward voltage (K_{VFF} block): a unique circuit algorithm detects the transition of the peak of input voltage through seven thresholds and generates an equivalent V_{FF} level centered within the 8-Q_{VFF} ranges. A great benefit of the Q_{VFF} architecture is that the fixed K_{VFF} factors eliminate any contribution to distortion of the multiplier output, unlike an externally filtered input voltage signal which unavoidably contains 2nd-harmonic distortion components.

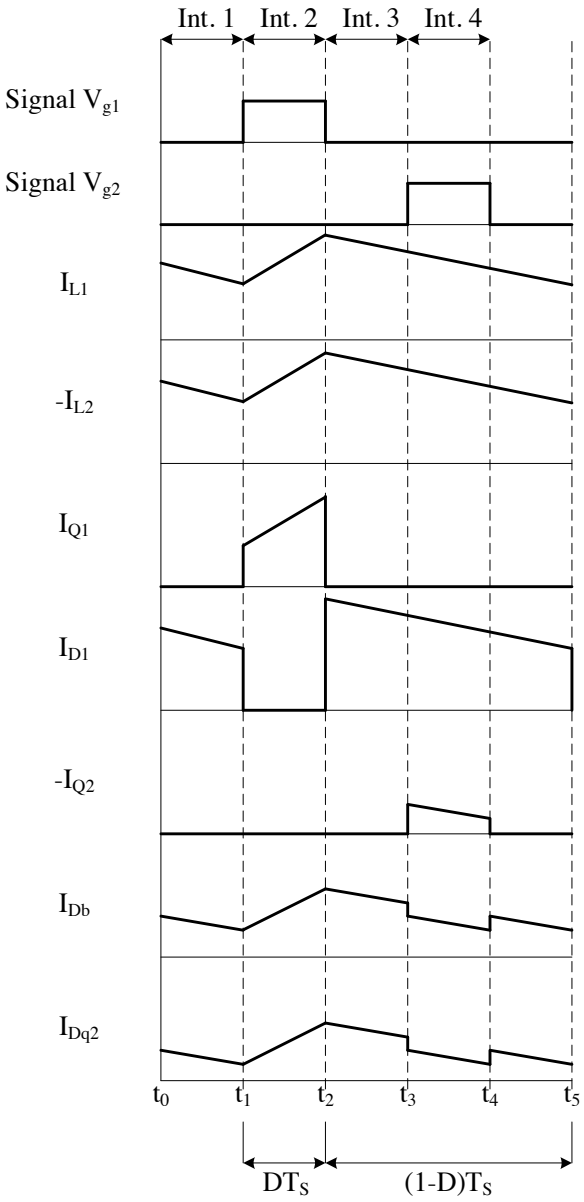

Fig. 3. Waveforms of proposed converter for D < 0.5.

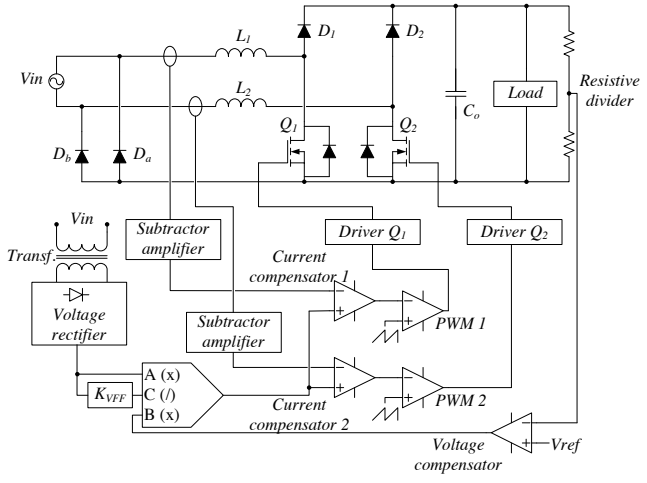

Fig. 4. Internal control structure of UCC28070 connected to the proposed converter.

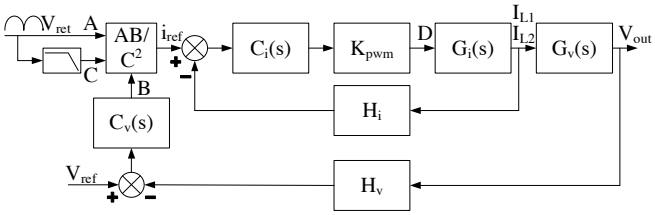

Fig. 5. Closed loop control in block diagram.

7) Multiplier: this block generates a reference signal from the algebraic operations provided by the input signals A, B and C, as shown in the multiplier block of Figure 4.

8) Voltage compensator: this block monitors the output voltage of the converter and acts on the voltage loop dynamics.

9) Current compensators: the current compensators monitor the currents through the inductors and act on the current loop dynamics.

10) PWM modulators: these are comparators of two input signals, the first being a sawtooth signal with set frequency, adjusted for the design. The second signal is the control signal from the current compensator. The result is the PWM signals applied to the drivers that will trigger the switches Q_1 e Q_2.

11) Drivers: they have the function of accurately reproducing the waveform of the PWM signal, adjusting the voltage and current values to the necessity of the switches Q_1 and Q_2. Model: UCC27324.

IV. EXPERIMENTAL RESULTS

A prototype for proposed converter was built, as shown in Figure 6. The specifications for the built prototype and equipments used for experimental results are presented on Table III, as well as devices used in prototype are specified on Table IV.

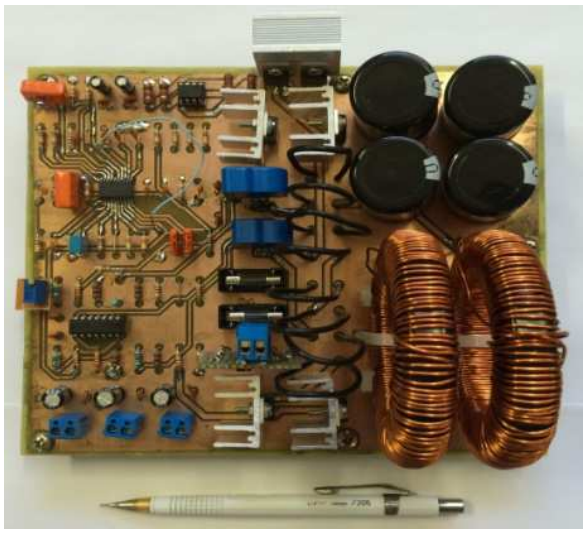

Fig. 6. Experimental prototype of proposed converter.

In relation to inductors design described on Table IV, although L_1 and L_2 inductances are the same value, it was not considered as a design of coupled inductors due the greater flexibility that uncoupled inductors provide to the designer. Choosing to use two separate uncoupled inductors typically offers a much broader selection of components. Additionally, the capacitors from Table IV are of electrolytic type, being the choice made due to availability of some units in the laboratory.

The estimated loss distribution for the semiconductors is provided in Figure 7 considering 220 V grid voltage, 400 V dc output voltage and 70 kHz switching frequency. The MOSFETs are under more stress, followed by losses on inductors and ultrafast diodes. For 1 kW output power, and 25.5 W total losses, the converter efficiency is nearby 98%.

For estimated loss distribution in semiconductors, Figure. 7, and for efficiency tests, Figure 14, the Politerm auxiliary power supply model POL-16E is included on measurements.

The Politerm power supply was used to supply IC UCC28070 and IC UCC27324. Experimental waveforms from proposed converter are provided in Figures 8 to 13.

TABLE III
Parameters Used for the Prototype

Parameter	Value	Equipment
Rated input voltage	V_{in}: 220 V	-Politerm power supply, model POL-16E
Rated output voltage	V_{out}: 400 V	
Rated output power	P_{out}: 1 kW	-Tektronix oscilloscope, model MDO4054B-3
Switching frequency	f_s: 70 kHz	
Line frequency	f_{line}: 60 Hz	-Tektronix power analyzer, model PA4000
Output ripple voltage	ΔV: 5%	
Inductor ripple current	ΔI_L: 20%	-JNG voltage regulator, model TDGC2-5kVA

TABLE IV
Devices Used in Prototype

Device	Manufacturer	Part number	Quantity
Inductors L_1, L_2 (L=1,045mH)	Core: Magmattec	Core: MMTS60T7713	2
Sic Schottky diodes D_1, D_2	Infineon	IDH04S60C	2
MOSFETs Q_1, Q_2	Infineon	IPP60R099CP	2
Ultrafast diodes D_a, D_b	Fairchild	MUR860	2
Capacitors (C_o=220μF)	EPCOS	B43504-S5227-M1	4

The input voltage, input current, output voltage and output current in the load are given in Figure 8. The input current is in phase with the input voltage and has a sinusoidal shape. In addition, there is a low frequency ripple in the output voltage. Furthermore, the ripple in the output voltage is also reflected in the output current. The input voltage, output voltage and the currents in the inductors L_1 and L_2 are given in Figure 9. As can be seen, the currents in the inductors are 180° out of phase. Due to the existence of MOSFETs as

switches, the return currents for the power supply are made partially through the intrinsic diodes of the MOSFETs and the inductors L_1 and L_2.

Figure 10 presents the command pulse of switch Q_1, current in switch Q_1 and current in inductor L_1 for duty cycle D less than 0.5. Figure 11 presents the command pulse of switch Q_1, current in switch Q_1 and current in inductor L_1 for duty cycle D greater than 0.5. The shapes of these waveforms correspond to theoretical waveforms.

Figures 12 and 13 present a 50% load step, changing the output current from 1.17 A to 2.34 A. Thus, it is noted that the overshoot in the waveform of the output voltage is around 15 V, and its value is reestablished to 400 V in a period close to 300 ms. It is important to note that the output voltage waveform in Figure 13 is set in the ac coupling mode.

The experimental efficiency for the prototype built is presented in Figure 14, considering 220 V grid voltage, 400 V dc output voltage and 70 kHz switching frequency. It can be highlighted that the converter has an efficiency range practically constant over the entire analyzed power.

The efficiency measurements values in Figure 14 are slightly higher than Figure 7, efficiency nearby 98%, because the values in Figure 7 correspond to calculated values. In other words, for the measured values in Figure 14 must be considered the calibration and tolerance of used equipment.

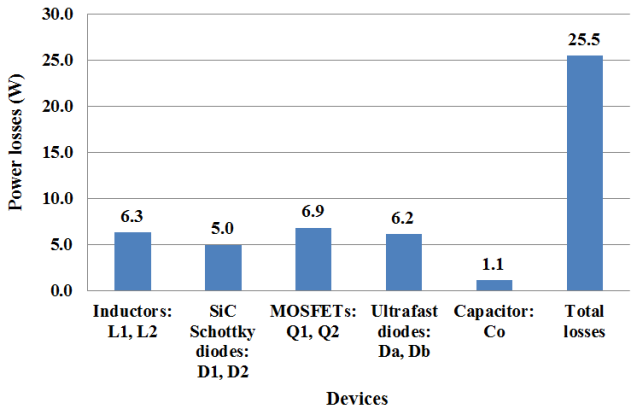

Fig. 7. Estimated loss distribution for the semiconductors considering V_{in} = 220 V, V_{out} = 400 V and f_s = 70 kHz.

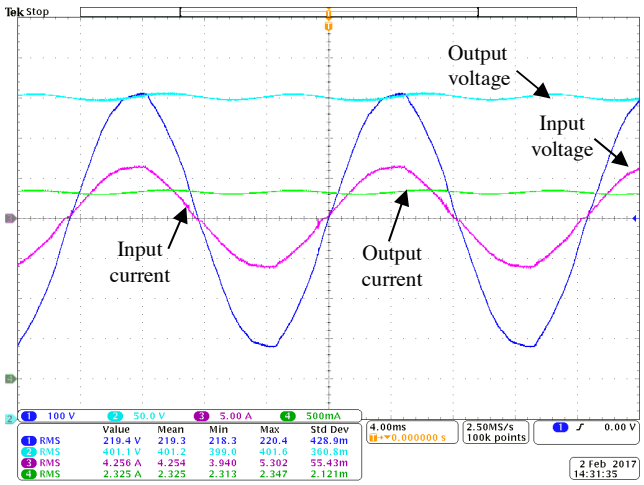

Fig. 8. Input voltage, input current, output voltage and output current.

Figure 15 illustrates the measured power factor as a function of output power. The shape of the curve presented was already expected, featuring a higher value of power factor near the nominal output power. Therefore, the maximum measured power factor value is 0.996. Figure 16 presents the total harmonic distortion of the input current as a function of output power.

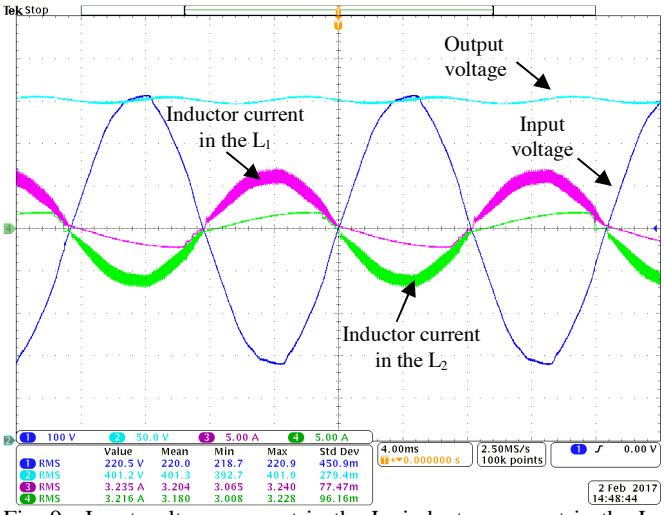

Fig. 9. Input voltage, current in the L_1 inductor, current in the L_2 inductor and output voltage.

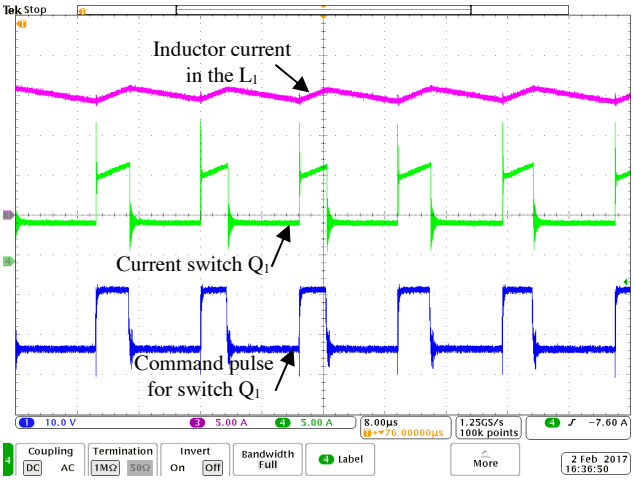

Fig. 10. Command pulse for switch Q_1, current in switch Q_1 and current in inductor L_1 for D < 0.5.

Figure 17 illustrates the harmonic spectrum of input current amplitude for converter operating in rated load and considering 220 V grid voltage, 400 V dc output voltage and 70 kHz switching frequency. This is compared to the limits for equipments classified as class D in the standard IEC 61000-3-2. The proposed converter meets the class D standard limits for all harmonics.

In this case, as the output power approaches the design nominal value, THD decreases, as expected. Therefore, the lowest value found for THD is 3.57%.

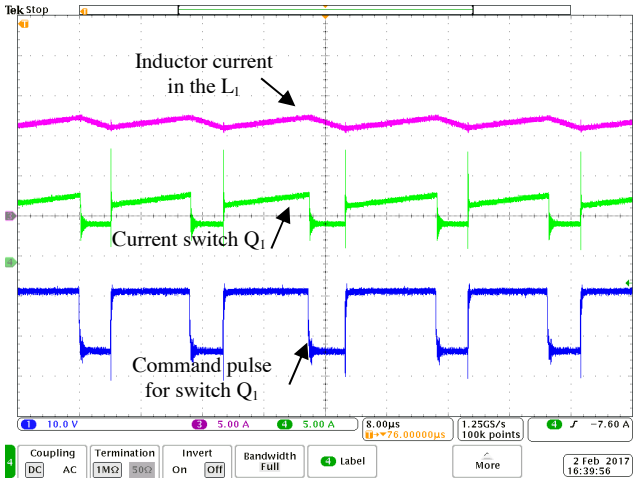

Fig. 11. Command pulse for switch Q_1, current in switch Q_1 and current in inductor L_1 for $D > 0.5$.

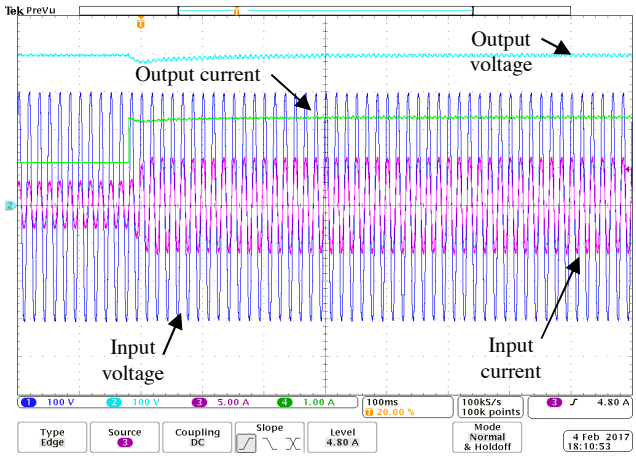

Fig. 12. Load step 50%: input voltage, input current, output voltage and output current.

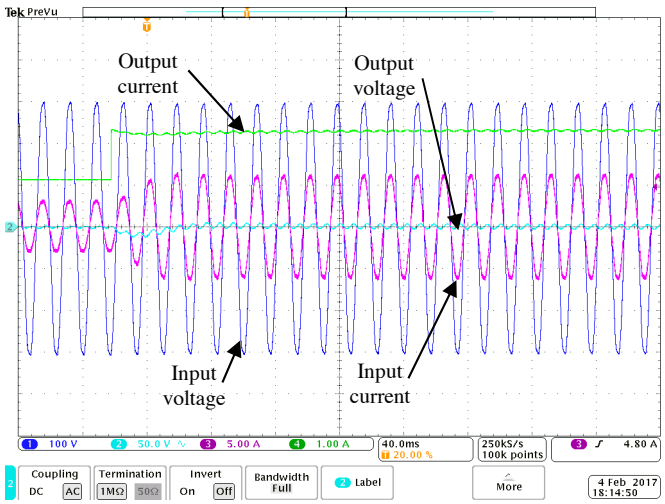

Fig. 13. Load step 50% with output voltage in ac coupling: input voltage, input current, output voltage and output current.

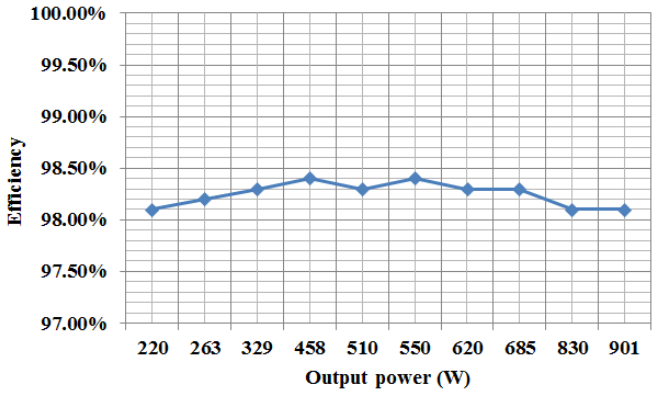

Fig. 14. Efficiency as a function of output power for V_{in} = 220 V, V_{out} = 400 V and f_s = 70 kHz.

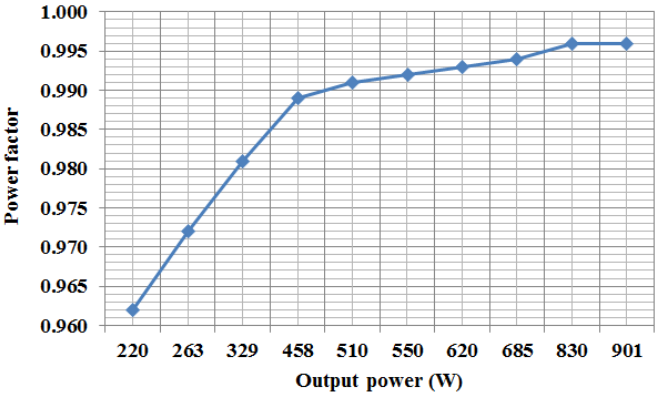

Fig. 15. Power factor as a function of output power for V_{in} = 220 V, V_{out} = 400 V and f_s = 70 kHz.

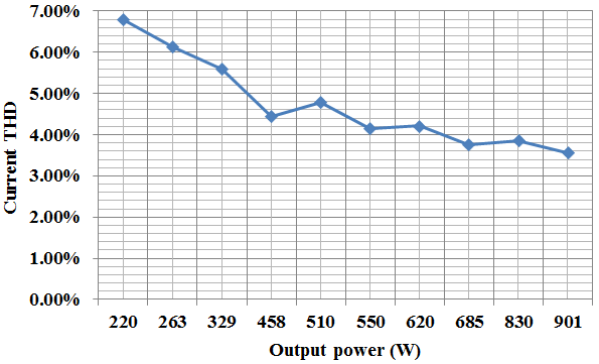

Fig. 16. Current THD as a function of the output power for V_{in} = 220 V, V_{out} = 400 V and f_s = 70 kHz.

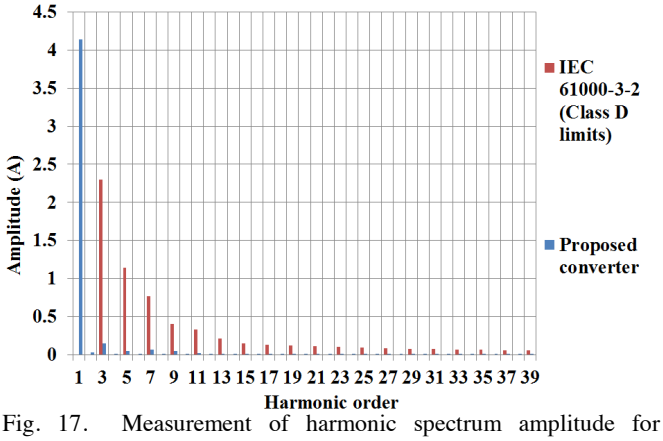

Fig. 17. Measurement of harmonic spectrum amplitude for proposed converter compared to IEC 61000-3-2 standard.

V. CONCLUSIONS

A bridgeless boost power factor corrector AC-DC converter has been proposed as a front end converter in a double stage level 1 for electric vehicle battery chargers. A circuit operation analysis and control strategy for proposed topology has been presented. A prototype was built in order to confirm the theoretical results. The converter presents a peak efficiency of 98.4% at half load, and features high efficiency from light load to full load, being this essential to reduce the charging time, size and cost of the charger, and cost of electricity. Experimental results show that input current THD is less than 5% from half to full load and the power factor is higher than 0.99 from half to full load. Additionally, the converter is properly suited for automotive level 1 residential charging applications.

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BIOGRAPHIES

Jefferson Carlos Fischer, was born in 20/06/1988 in Jaraguá do Sul/SC is an electrical engineer (2012) with the Centro Universitário Católica de Santa Catarina and master (2017) with Universidade do Estado de Santa Catarina (UDESC). His areas of interest are in power electronics and comprehends: ac-dc converters, converters applied to electric vehicles and hybrid electric vehicles. Eng. Fischer is member of the Brazilian Society of Power Electronics (SOBRAEP).

Sérgio Vidal Garcia Oliveira, was born in 17/04/1974 in Lages/SC is an electrical engineer (1999) with the Universidade Regional de Blumenau (FURB), master (2001) and doctor (2006) in Electrical Engineering with the Universidade Federal de Santa Catarina (UFSC). Sérgio is a full-time professor at Universidade do Estado de Santa Catarina (UDESC) and in part-time at FURB. His areas of interest are in, electric drives, distributed generation systems, quality and energy efficiency. Dr. Oliveira is member of SOBRAEP, SBA, PELS and IES.

Juliana Andressa da Silva, was born in 21/12/1989 in Foz do Iguaçu/PR is a telecommunications engineer (2014) and master's degree student (2017-2018) with the Universidade Regional de Blumenau (FURB). Her areas of interest are in power electronics and comprehends: ac-dc converters, electromagnetic losses and energy efficiency.

Yales Rômulo de Novaes, was born in 1974 in Indaial/SC, is an electrical engineer (1999) with the Universidade Regional de Blumenau (FURB), master (2000) and doctor (2006) in Electrical Engineering with the Universidade Federal de Santa Catarina (UFSC). From 2006 to 2008 was a post-doctoral fellow at the Industrial Electronics Laboratory at EPFL, Lausanne, Switzerland. From 2008 to 2010 worked as scientist with the Power Electronics Systems group at ABB Corporate Research Center, Daetwill, Switzerland. Currently he is an associate professor at Universidade do Estado de Santa Catarina (UDESC).