A Full-Bridge Partial-Power Processing Converter for Three-Stage Small Wind Turbine Systems

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***Abstract* – In order to process the energy generated by small wind turbines (SWT) in grid-connected systems, three-stage configurations (rectifier, dc-dc converter, and inverter) have been suitable due to low cost of three-phase diode rectifiers, facility to perform the maximum power point tracking in dc-dc converters, and power decoupling between the grid and wind generator. As drawback, the three-stage solutions can present higher losses in relation to two-stage systems due to the additional converter. To reach a better efficiency, partial-power converters (PPC) can be used, in which only a part of the power generated by the SWT is processed by the converter. In this method, topology, power/voltage levels, and the operating range characteristics can impact the power handled by the converter. Since the experimental analysis of PPC applied to SWT systems remains to be investigated in the literature, this paper analyzes the Full-Bridge with Zero-Voltage Switching operating as PPC in SWT systems connected to the single-phase grid. In order to evaluate the performance of the proposed structure, experimental results are verified for a 1.5 kW SWT, in which the Full-Bridge PPC processes only 70% of the generated power. In relation to the full-power processing, the partial-power processing has reduced the losses in 35.9%.**

***Keywords* – Full-Bridge, Grid-Connected, Small Wind Turbines, Partial-Power Processing Converters.**

I. INTRODUCTION

Conventional power generation plants using fossil fuels are determined as unsuitable in long-term strategic plans. Consequently, many researches have been carried out in order to improve renewable energy sources technologies, e.g. photovoltaics (PVs) and high-power wind turbines (WTs) [1]. However, small wind turbines (SWT) systems still need more development and require attention [2], [3]. Some proposals with different characteristics have been suggesting to improve the conversion efficiency, minimize costs and increase the reliability of SWT systems [4].

Three-stage power processing systems, composed of a passive three-phase rectifier, dc-dc converter, and inverter, can enhance the maximum power point tracking (MPPT) range in grid-connected SWT systems [5]. This feature is available due to the power decoupling between the inverter dc bus voltage and rectifier [6]. Nevertheless, the additional dc-dc stage increases the number of components, cost, size and losses [7]. In this structure, the ac-dc, dc-dc and dc-ac power conversion stages processes all the power generated by the SWT system, which is known in the literature as full-power converters (FPC), according to Figure 1.a.

In this context, the application of partial-power converters (PPC) ensure the increase of dc-dc stage efficiency. The idea of partial-power processing (PPP) is established on a fraction of the power being handled by the converter, whereas the remaining power flows through the source to the load without conversion, i.e., with unitary efficiency [8], [9]. The PPC power flow in a three-stage SWT system is depicted in Figure 1.b. In this scenario, only an amount of power is processed by the dc-dc converter, thus the total losses will be naturally lower than with FPC topologies. Consequently, higher efficiency and power density are obtained, as well as lower volume and costs.

Recently, many researches have been published applying series-connected PPC (S-PPC) in PV systems [10]–[16] and battery charging systems [17], [18], resulting in higher efficiency and reduced power rating compared to standard FPC topologies. However, an experimental analysis of S-PPC employed to SWT systems remains to be investigated in depth in the literature. Thus, the purpose of this paper is to continue the initial study published by [19], [20], and evaluate the use of Full-Bridge dc-dc converter with PPP applied to three-stage SWT systems. Experimental results are carried out, in order to corroborate the theoretical analysis of the grid-connected system.

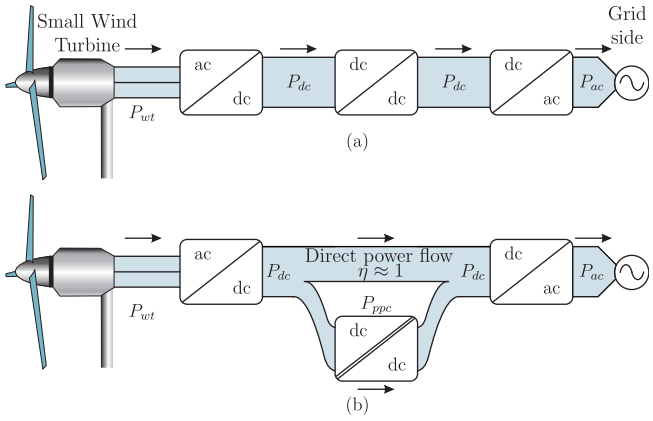

Fig. 1. Power flow of a three-stage SWT processing system employing a: (a) FPC and (b) PPC.

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II. THE PARTIAL-POWER PROCESSING CONCEPT

The use of S-PPC configuration adds a path to active power flow, as depicted in Figure 2, in which the S-PPC structure is configured as two converters: the dc-dc converter and a dummy bypassed converter whose inputs are connected in parallel and outputs are series-connected [21]. In this way, the power flow from input to output is divided between the actual converter and the dummy converter, where a fraction of the input power is directly transferred to the output with unitary efficiency and no conversion stage. It should be highlighted that due to the series connection between input and output, the application of any isolated topology results in the loss of galvanic isolation [22]. Hence, structures based on this concept requires a topology with galvanic isolation inside, in order to avoid a potential short-circuit between positive and negative input terminals in any topological state.

The configurations of S-PPC can be divided into two categories [21]: input-parallel-output-series (type I) structure and input-series-output-parallel (type II) structure, as shown in Figures 3.a and 3.b, respectively.

A. Acitve Power and Efficiency

The S-PPC output active power ($P_{C,out}$) is the average value of instantaneous power in a period, seen at the output terminals. In the S-PPC shown in Figure 3.a, if disregarded current and voltage ripples, the AP $P_{C,out}$ is given by:

$$P_{C,out} = V_C I_{out}, \tag{1}$$

and the output active power for the whole dc-dc stage (P_{out}) is defined by:

$$P_{out} = V_{out} I_{out}. \tag{2}$$

Therefore, the ratio between $P_{C,out}$ and P_{out} in type I configuration is described by:

$$\frac{P_{C,out}}{P_{out}} = \frac{V_C I_{out}}{V_{out} I_{out}} = \frac{V_{out} - V_{in}}{V_{out}} = 1 - \frac{V_{in}}{V_{out}} = 1 - k, \tag{3}$$

where k is the ratio between the input (V_{in}) and output (V_{out}) voltages, i.e. k is the inverse of voltage gain.

On the other hand, the relationship between $P_{C,out}$ and P_{out} for the S-PPC type II, illustrated in Figure 3.b, is given by:

$$\frac{P_{C,out}}{P_{out}} = \frac{V_{out} I_{C,out}}{V_{out} I_{out}} = \frac{I_{out} - I_{in}}{I_{out}} = 1 - \frac{I_{in}}{I_{out}} = 1 - \frac{1}{k}. \tag{4}$$

In order to illustrate this effect, Figure 4 shows the active power processed by the S-PPC versus parameter k. The curves

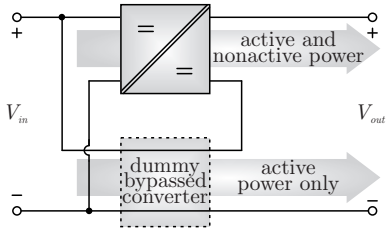

Fig. 2. Active and nonactive power processing on S-PPCs.

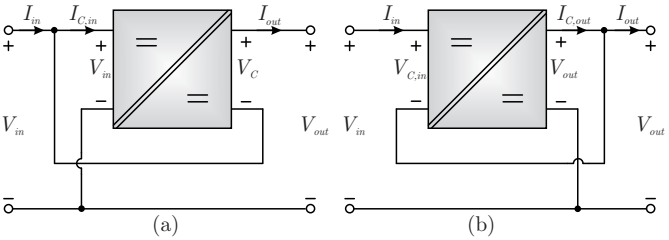

Fig. 3. S-PPC connections schemes. (a) Input-parallel-output-series (Type I). (b) Input-series-output-parallel (Type II).

were calculated by means of (3) and (4) for S-PPC type I and type II, respectively.

According to Figure 4, as lower is the difference between input and output voltages, smaller will be the active power processed by the S-PPC in comparison to the total active power. When the voltage gain ($M = V_{out}/V_{in}$) is close to one, the S-PPC active power approaches to zero. Therefore, the S-PPC can be designed for a portion of the generated power by the SWT system, which provides higher power density and lower volume when it is compared to FPC topologies.

In addition, it is possible to conclude that type I configuration is more suitable when boost characteristic (step-up) is desired, whereas the type II configuration is more suitable for buck characteristic (step-down). Also, an important feature of type I configuration is that the active power in the S-PPC varies linearly with the input voltage variation, as can be seen in (3).

The S-PPC efficiency ($\eta_{regulator}$) is defined by the ratio between the active power at the output and input terminals of the dc-dc converter, given by:

$$\eta_{regulator} = \frac{P_{C,out}}{P_{C,in}}. \tag{5}$$

On the other hand, the global efficiency (η_{global}) is the ratio between the active power at the output and input terminals for the entire dc-dc stage. Once $P_{C,out}$ is smaller than P_{out}, and all losses are concentrated in the S-PPC, η_{global} is greater than $\eta_{regulator}$, and it can be calculated by an equivalent expression presented by [12]:

$$\eta_{global} = \frac{P_{out}}{P_{in}} = 1 - \frac{P_{C,out}}{P_{out}} \left(1 - \eta_{regulator}\right). \tag{6}$$

III. SMALL WIND TURBINE OPERATING RANGE

In this study, the wind power is extracted from a 1.5 kW SWT model Gerar 246, manufactured by Enersud [23], with

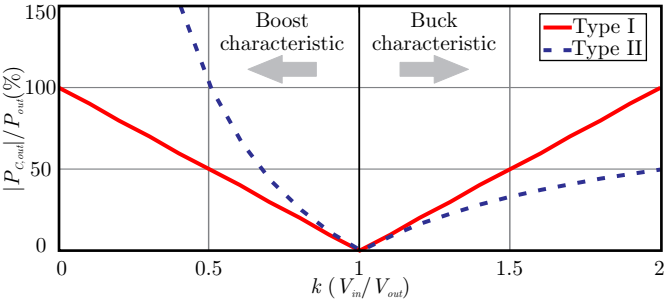

Fig. 4. Active power in S-PPC type I and type II plotted in function of parameter k.

horizontal axis, three blades and active stall, connected to an axial flux permanent-magnet synchronous generator (PMSG). The Gerar 246 power-behavior is typical from a SWT, i.e., this study can be applied to all SWT family.

The power delivered by the SWT system can be estimated in terms of its angular rotational speed (ω_r) for different wind speeds (v_ω). Therefore, the characteristic between mechanical power as a function of angular speed $P_{mec}(\omega_r)$ is created, as depicted in Figure 5. This curve is obtained from [24]:

$$P_{mec}(\lambda, v_w) = \frac{1}{2}\rho\pi r^2 v_w^3 C_p(\lambda) \tag{7}$$

$$\omega_r(\lambda, v_w) = \frac{\lambda v_w}{r} \tag{8}$$

where P_{mec} is the mechanical power on the rotor shaft (W), ρ is the air density (kg/m^3), r is the rotor radius (m), v_w is the wind speed (m/s), C_p is the power coefficient, ω_r is the rotor speed (rad/s), and λ is the tip-speed-ratio (TSR).

Each value of v_w presents an optimum operational point, in which the maximum quantity of mechanical power is obtained [25]. The P_{max} curve shows the range of ideal operation bounded between 400 rpm and 700 rpm.

In relation to the S-PPC project, the operating range of wind speed v_w and output voltage/power levels of the passive three-phase rectifier have to be considered, since it defines the S-PPC input voltage (V_{in}) range, the gain necessary to perform the MPPT, and the fraction of active power processed.

On plotting the rectifier output power characteristic as a function of its output voltage, it can be seen that the SWT presents a single maximum power point for each rotational speed, as illustrated in Figure 6. Therefore, it is possible to define the minimum and maximum parameters of voltage and power in the rectifier output. These values are employed to design the S-PPC operational range.

In order to operate the permanent-magnet synchronous generator in a safe way and to provide an adequate minimum value of voltage on rectifier output, the rotor speed was considered from 400 rpm to 700 rpm (which means a wind speed from 10 m/s to 12 m/s). Additionally, since the electric frequency and peak line voltage are dependent of rotor speed, as can be observed in Figure 6, some equations related to the PMSG have to be included.

By means of (9) and (10) [26], the line-to-line voltage

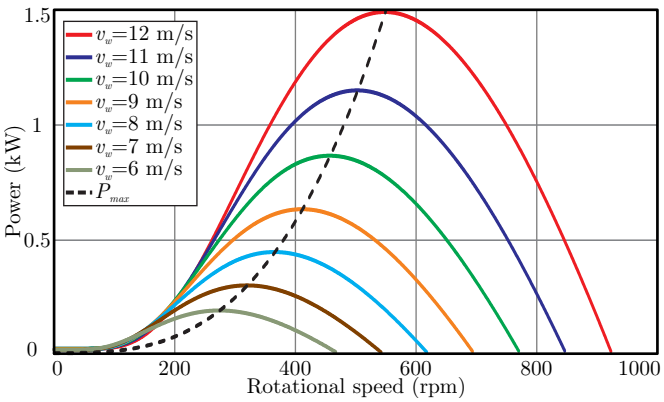

Fig. 5. Curves of mechanical power in function of angular rotational speed $P_{mec}(\omega_r)$ for wind speeds from 6 to 12 m/s.

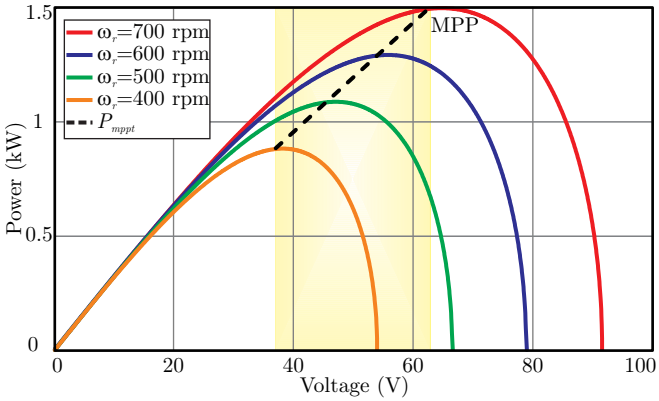

Fig. 6. Electrical power curves (P_{in}) as a function of the S-PPC input voltage (V_{in}) for angular speeds from 400 to 700 rpm.

(V_{Lp}) and electric frequency (f_e) of the PMSG are calculated, respectively, by:

$$V_{Lp} = \sqrt{3}\sqrt{2}K_e\omega_r \tag{9}$$

$$f_e = \frac{\omega_r P}{120} \tag{10}$$

where K_e is the armature constant (mV/rpm) and P is the number of poles, extracted from [23].

According to the limits defined for the rotor speed, as weel as equations (9) and (10), Table I shows the operating range of the SWT system.

IV. FULL-BRIDGE DC-DC CONVERTER WITH PARTIAL-POWER PROCESSING

The topology employed in the structure shown in Figure 2 must have galvanic isolation. Therefore, the Full-Bridge ZVS-PWM [27] topology was chosen since it has already been applied as S-PPC with great performance of efficiency and power density in [12], [22].

Since voltage step-up characteristic is required due to the low levels of V_{Lp} in the PMSG terminals, as can be observed in Table I, the type I configuration is more suitable due to the active power characteristic depicted in Figure 4.

The Full-Bridge ZVS-PWM topology connected as S-PPC in type I configuration is shown in Figure 7, in which is noted that the Full-Bridge topology is not modified, since the unique change in the structure is the connection between the input and output, which performs the partial-power processing. It should be highlighted that the S-PPC type I connection does

TABLE I
Operating Range of SWT System Employing Gerar 246

Parameter	Specification
Minimum rotor speed ($\omega_{r_{min}}$)	400 rpm
Maximum rotor speed ($\omega_{r_{max}}$)	700 rpm
Minimum rectifier output voltage ($V_{in_{min}}$)	35 V
Maximum rectifier output voltage ($V_{in_{max}}$)	64 V
Minimum electric frequency ($f_{e_{min}}$)	46.6 Hz
Maximum electric frequency ($f_{e_{max}}$)	81.6 Hz
Minimum electric power ($P_{in_{min}}$)	880 W
Maximum electric power ($P_{in_{max}}$)	1500 W

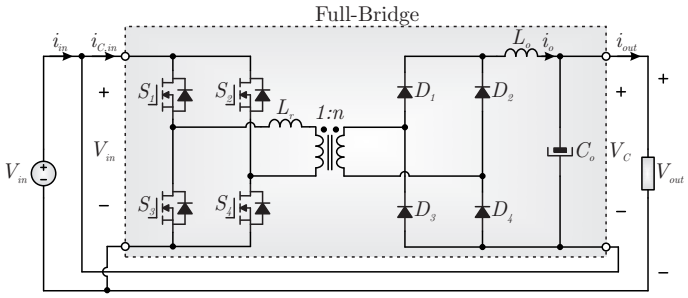

Fig. 7. Full-Bridge ZVS-PWM topology connected as S-PPC in input-parallel-output-series configuration.

not change the static/dynamic analysis, which allows the use of classical Full-Bridge topology to develop the mathematical modeling.

The Full-Bridge ZVS-PWM topology highlighted in Figure 7 includes an output filter inductor, as well as a transformer that transfers energy from the primary to the secondary. The switches in the primary side are controlled by phase-shift modulation with constant switching frequency, and the diodes in the secondary side plays as a rectifier [28]. Furthermore, the Full-Bridge ZVS-PWM topology presents the advantage of zero-voltage switching (ZVS) for wide load range.

The static and dynamic analysis, design equations and transfer functions were derived from [28]. In addition, the small-signal analysis were developed by modeling the effects introduced by the phase-shift modulation and the application of transformer leakage inductance to resonate with the junction capacitance of MOSFETs to achieve ZVS, as depicted in Figure 8.

The adequate value for the dc bus voltage (V_{out}) is defined by the inverter from power grid side (220 V for a single-phase grid of 127 V). The rectifier output voltage varies according to Figure 6. Thus, the active power range processed by the converter can be determined by means of:

$$P_{C,max} = P_{in,max}\left(1 - \frac{V_{in,max}}{V_{out}}\right), \tag{11}$$

$$P_{C,min} = P_{in,min}\left(1 - \frac{V_{in,min}}{V_{out}}\right). \tag{12}$$

Based on (11) and (12), as well as the input voltage variation determined in Table I, it is seen in Figure 9 the input power (P_{in}), active power handled by the Full-Bridge ZVS-PWM S-PPC (P_C), and direct power flow (P_{dir}) for each operating point of the SWT system.

It should be noted in Figure 9 that, for nominal operation

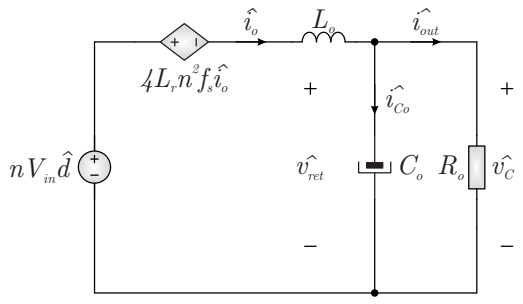

Fig. 8. Small-signal modeling of Full-Bridge ZVS-PWM.

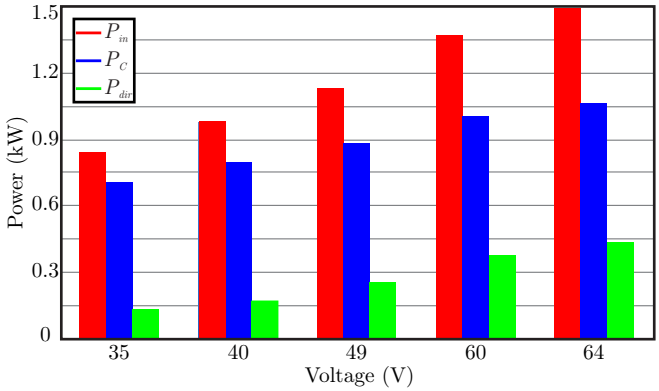

Fig. 9. Input power (P_{in}), active power processed (P_C), and direct power flow (P_{dir}) in Full-Bridge ZVS-PWM S-PPC for different operational points of SWT system.

with rotational speed at 700 rpm ($P_{in} = 1.5\ kW$), the active power processed by the converter (P_C) is close to 1050 W, whereas the direct power flow (P_{dir}) is around 450 W. As a result, the PPP concept applied to the SWT Gerar 246 provides a reduction of 30 % in the active power handled by the dc-dc converter at rated power operation. In other words, for a 1.5 kW system, a dc-dc converter with just 1 kW was designed. Furthermore, as lower is the input voltage, higher will be the active power processed by the S-PPC in comparison to the total active power. This relation can be explained by the fact that, reducing V_{in} for a fixed V_{out}, higher will be the voltage V_C across the Full-Bridge output capacitor C_o, being in accordance with (3).

V. EXPERIMENTAL RESULTS

A. Proposed System Structure and Control Loops

In order to corroborate the theoretical analysis, Figure 10 depicts a general overview of the proposed system. It is observed the integration of rectifier with the Full-Bridge S-PPC of Figure7, as well as the inverter and its control strategy to connect the system in the power grid.

Aiming to obtain the maximum available power from the SWT Gerar 246, the generator reference speed (ω_r^*) have to be controlled by the MPPT algorithm. Thus, measurements of electrical power and rotational speed are necessary in order to determine the maximum power point (MPP) [29]. Taking the MPP parameters for each value of v_w (Figure 5), an optimum power curve can be traced, which is stored in a lookup table. Thus, the MPP can be calculated.

To connect the dc bus to the power grid, a inverter have to be included in the system. In this study, the full-bridge topology with three-level sinusoidal PWM modulation was selected. In order to attenuate high frequency components due to the switching, an LCL low-pass filter was employed. Then, the inverter stage is able to inject a sinusoidal current in the grid with low total harmonic distortion (THD), and in phase with the grid voltage. Also, the dc bus voltage can be regulated by controlling the amplitude of grid current.

B. Design Specifications and Components

Defining the dc-dc stage input voltage range and its active power processed, the whole Full-bridge S-PPC converter design is carried out, and the main results are seen in Table II.

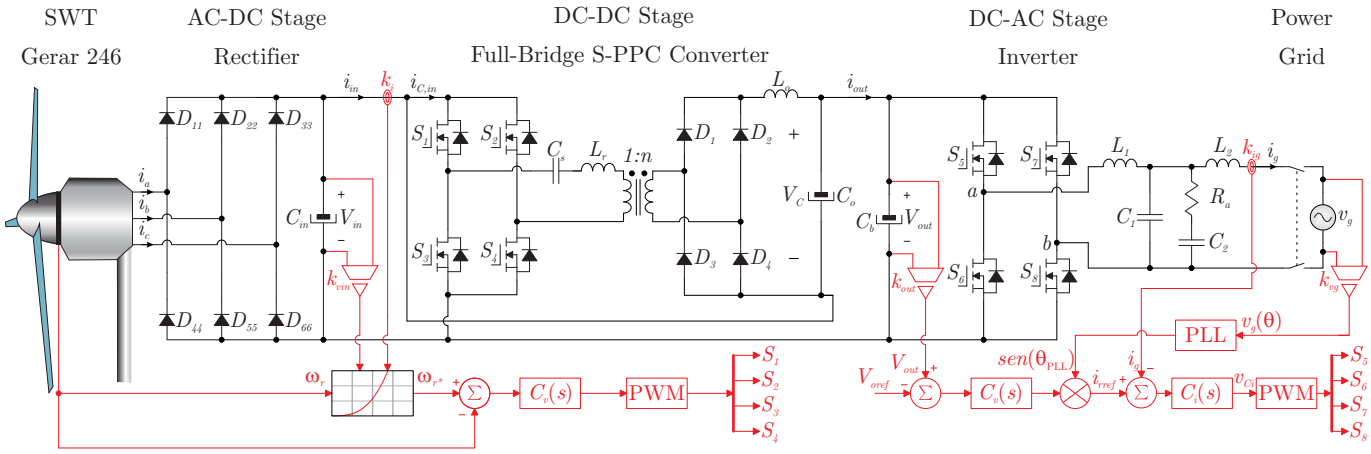

Fig. 10. General overview of the proposed system.

TABLE II
Design Specifications of Full-Bridge S-PPC Converter

Parameter	Specification
Input voltage range (V_{in})	35 - 64 V
DC bus voltage (V_{out})	220 V
Peak voltage grid ($V_{p,grid}$)	179 V
Maximum output voltage (V_C)	185 V
Maximum S-PPC active power ($P_{C,out}$)	1 kW
Output active power (P_{out})	1.5 kW
Switching frequency (f_s)	40 kHz
Sampling frequency (f_a)	40 kHz
Capacitor voltage ripple (Δ_{VC})	1%
Inductor current ripple (Δ_{IL})	7%

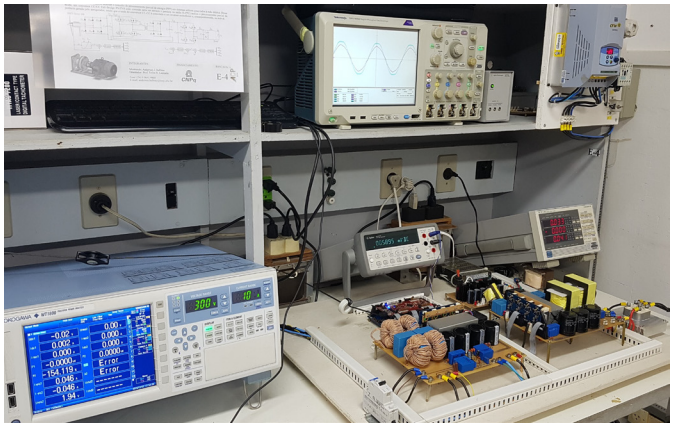

Fig. 11. Workbench developed for experimental tests.

The components employed in the rectifier, Full-Bridge S-PPC, and inverter prototypes are shown in Table III. The workbench developed for the experimental tests is depicted in Figure 11.

C. Experimental Waveforms

The prototype was tested considering the Full-Bridge ZVS-PWM S-PPC converter operating with $V_{in} = 64\ V$, which corresponds a PMSG rotational speed at 700 rpm. Figure 12 shows the experimental waveforms of voltage and current in the output of the dc-dc converter (v_C, i_o) and output of the dc-dc stage (v_{out}, i_{out}).

The partial-power processing concept can be verified by the

TABLE III
Components Employed in the Rectifier, Full-Bridge S-PPC Converter, and Inverter Prototypes

Parameter	Specification
Transformer T_r	n = 6/Epcos NEE-65/32/27
External inductance L_r	0.757 μH/Epcos NEE-42/21/15
Output inductance L_o	1.453 mH/Epcos NEE-65/32/27
Switches $S_1 - S_4$	Infineon IRF200P223
Diodes $D_1 - D_4$	Cree C3D12065A
Capacitors C_o	470 μF/Epcos B43504-B2477-M
Capacitors C_s	2.2 μF/Epcos B32674D
Capacitors C_{in}	3000 μF/Epcos B43501-B2108-M
Diode bridge	Semikron SKD 30/04
Capacitors C_b	4000 μF/Epcos B43501-B2108-M
Switches $S_5 - S_8$	Ixys IXFH60N65X2
Filter inductance L_1	205.8 μH/AmoFlux 0088439A7
Filter inductance L_2	205.8 μH/AmoFlux 0088439A7
Filter capacitance C_1	15 μF/Epcos B32774
Filter capacitance C_2	15 μF/Epcos B32774
Damp resistance R_a	4.1 Ω/10 W

output voltages waveforms, since the converter output voltage v_C (156 V) is equal to 70 % of the dc bus voltage v_{out} (220 V). Moreover, the average output currents i_o and i_{out} are equal to 6.8 A, which results an output active power P_{out} equal to 1.5 kW, while the active power processed P_C by the converter is equal to 1.05 kW.

The experimental waveforms of drain-source voltage of switch S_1 (v_{DS1}), reverse voltage of diode D_1 (v_{D1}), and resonant current (i_{Lr}) are shown in Figure 13. As can be seen, 520 V maximum voltage was measured in D_1, due to the hard-switching of diodes in the bridge rectifier. The RMS resonant current was equal to 31.58 A, with an average value equal to zero. A series capacitor (C_s) was added in series with L_r, and designed with 2% of ripple in order to avoid dc level in i_{Lr}.

The experimental waveforms of transformer primary side voltage (v_{AB}), converter output current (i_o), and resonant current (i_{Lr}) is depicted in Figure 14. It should be noted that the three levels in v_{AB} waveform, which are -V_{in}, 0, and +V_{in}.

In relation to switch S_1, a overvoltage of 28 V was measured in v_{DS1} during the turn-off, due to the hard-switching. On the

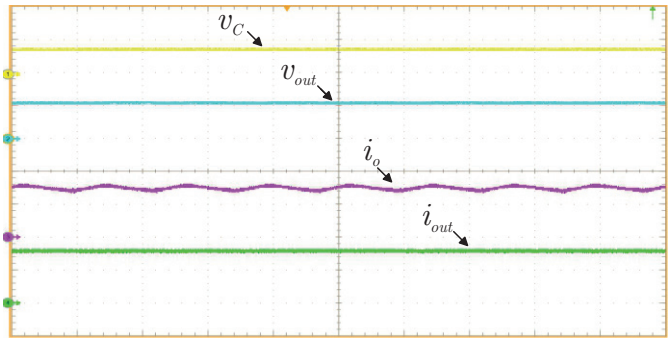

Fig. 12. Experimental waveforms of Full-Bridge ZVS-PWM S-PPC converter for $V_{in} = 64\ V$. Scales - time: 10 μs/div; converter output voltage (v_C): 200 V/div; dc bus voltage (v_{out}): 200 V/div; converter output current (i_o): 4 A/div; dc bus current (i_{out}): 4 A/div.

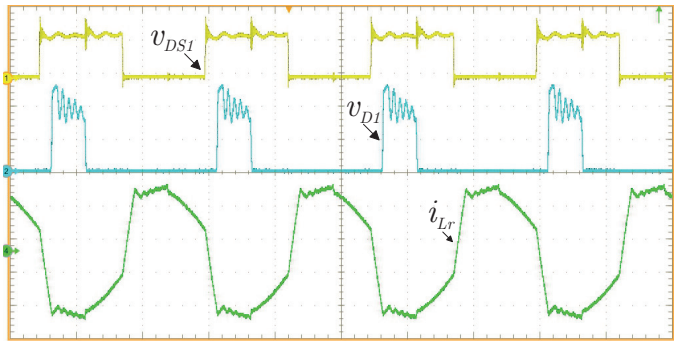

Fig. 13. Experimental waveforms of Full-Bridge ZVS-PWM S-PPC converter for $V_{in} = 64\ V$. Scales - time: 10 μs/div; switch S_1 drain-source voltage (v_{DS1}): 50 V/div; diode D_1 block voltage (v_{D1}): 200 V/div; resonant current (i_{Lr}): 20 A/div.

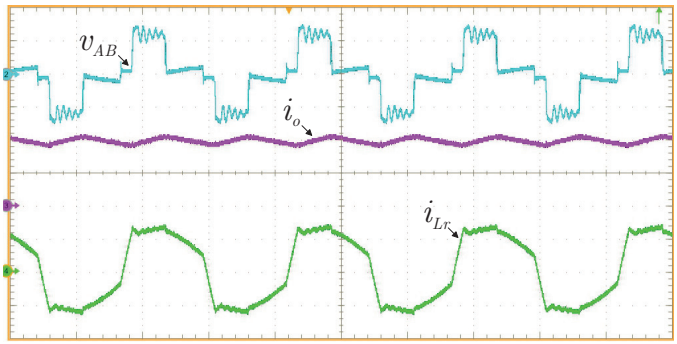

Fig. 14. Experimental waveforms of Full-Bridge ZVS-PWM S-PPC converter for $V_{in} = 64\ V$. Scales - time: 10 μs/div; transformer primary side voltage (v_{AB}): 50 V/div; converter output current (i_o): 3 A/div; resonant current (i_{Lr}): 30 A/div.

other hand, the turn-on commutates with zero-voltage, thus corroborating the soft-switching methodology, as can be seen in Figure 15.

In order to develop the experimental tests of the integrated system connected in the power grid, a startup routine was programmed in a DSP TMS320F28377S, manufactured by Texas Instruments. Figure 16 depicts the experimental waveforms obtained during the system startup, in which the steps from 1 to 6 (E1, E2, E3, E4, E5, and E6) are identified.

The system starts with the eight switches (four of Full-Bridge S-PPC and four of inverter) turned-off. Therefore, the power processed by the system is equal to zero. In state E1, the

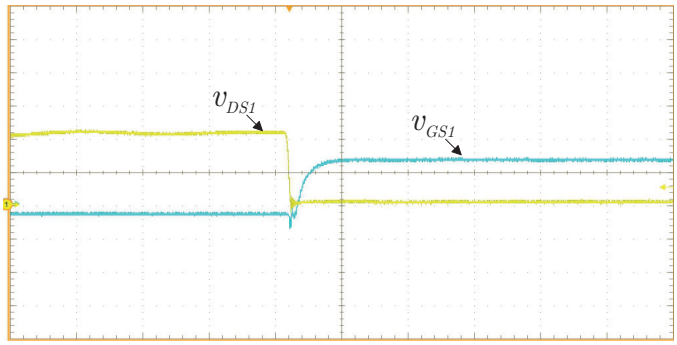

Fig. 15. Experimental waveforms of Full-Bridge ZVS-PWM S-PPC converter for $V_{in} = 64\ V$. Scales - time: 1 μs/div; switch S_1 drain-source voltage (v_{DS1}): 30 V/div; switch S_1 gate-source voltage (v_{GS1}): 10 V/div.

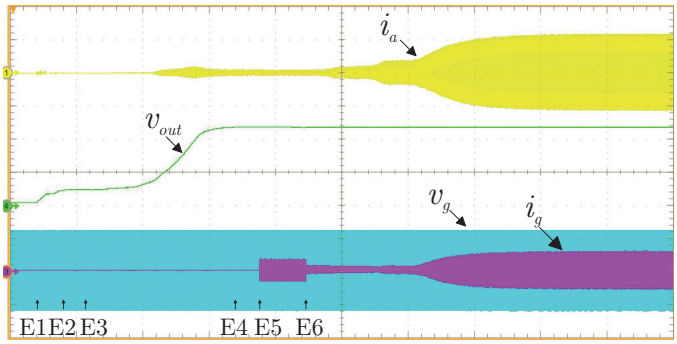

Fig. 16. Experimental waveforms of the proposed system startup connected in the grid. Scales - time: 20 s/div; PMSG phase current (i_a): 20 A/div; dc bus voltage (v_{out}): 100 V/div; grid voltage (v_g): 100 V/div; grid current (i_g): 20 A/div.

DSP has already been initialized and the PMSG is driven, thus emulating the beginning of wind generation. In the sequence, the synchronism with the grid (PLL) is stabilized in the state E2, and the digital control detects in state E3 the minimum threshold of wind power generation. Then, the dc bus is ready to startup, and the generator reference speed (ω_r^*) is increased by a ramp of 30 s to ensure a soft-start. When the dc bus voltage V_{out} is equal to 220 V, the state E4 is detected, thus allowing the connection relay to close in state E5. State E6 enables the switches in the inverter, and the control loops of inverter and MPPT are activated. In this point, the system reached the steady state, injecting 1.5 kW in the power grid.

D. Active Power Processed in Full-Bridge S-PPC

In order to obtain the experimental curve of power processed P_C in the converter as a function of the rotational speed, the input voltage was changed from the minimum value (35 V) up to the maximum value (64 V) (simulating a variation in rotational speed from speed 400 to 700 rpm), considering a constant dc bus voltage V_{out} equal to 220 V. Thus, for each PMSG rotational speed, the converter presents a relationship between the input power (P_{in}), the processed power (P_C), and the direct power flow (P_{dir}), as illustrated in Figure 17.

It is analyzed by means of Figure 17 that, as lower is the difference between V_{in} and V_{out}, smaller is the active power processed P_C by the converter in relation to the total input power P_{in}, while the amount of direct power flow P_{dir} increases. Lastly, the experimental results are in agreement

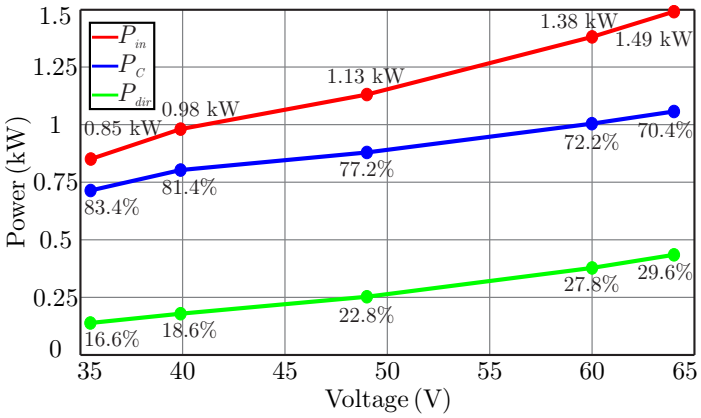

Fig. 17. Experimental curves of input power (P_{in}), processed power (P_C), and direct power (P_{dir}) in Full-Bridge ZVS-PWM S-PPC for different input voltages.

with the theoretical values of Figure 9, corroborating the proposed methodology.

E. Efficiency Analysis

The dc-dc stage efficiency-curve was obtained using a digital wattmeter Yokogawa WT1800, as illustrated in Figure 18. The results demonstrated that the dc-dc stage reaches the peak overall efficiency (96.5%) close to 50% at rated power, verifying the main advantages of the Full-Bridge ZVS-PWM S-PPC converter, i.e., reduced losses and increased overall efficiency.

In order to obtain a comparative result between the partial-power processing and full-power processing, a losses analysis was performed. The study compares through simulation the efficiency curves and voltage/current stresses of both power processing strategies. The non-idealities considered in the analysis were: capacitors series resistance, MOSFET on-resistance, diode forward voltage, winding resistance of external resonant inductor, transformer winding resistance, diode voltage drop, clamping and winding resistance of output filter. Besides that, the same physical components (MOSFETs, diodes and passive elements) were considered in both simulations, since the same components were suitable to FPP and PPP.

The efficiency curves of partial-power processing in comparison to full-power processing obtained through simulation are shown in Figure 19. It should be noted

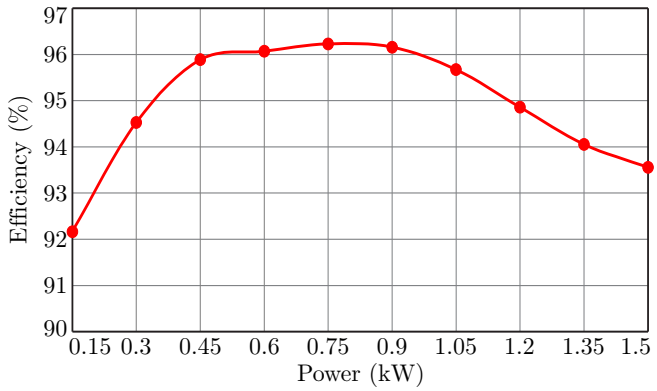

Fig. 18. Experimental efficiency of Full-Bridge ZVS-PWM S-PPC converter.

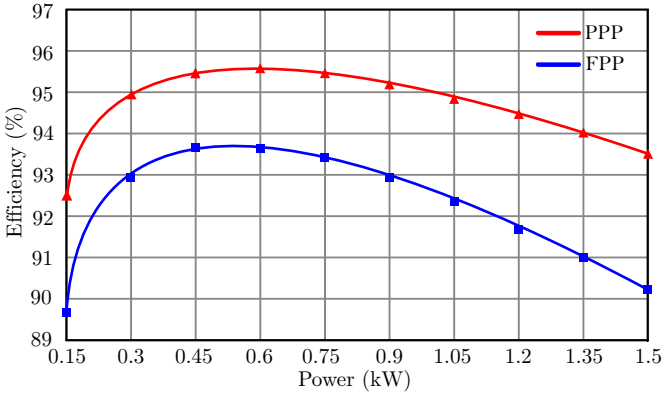

Fig. 19. Simulated efficiency of partial-power processing (PPP) and full-power processing (FPP).

that at rated power the partial-power processing and full-power processing achieved an efficiency equal to 93.51% and 90.22%, respectively. In terms of energy processing, the partial-power processing reduces the losses in 35.97% in relation to the full-power processing.

Furthermore, the partial-power processing reduces around 25% the current stresses in the primary switches and the voltage stresses in the rectifier diodes, when it is compared to full-power processing.

VI. CONCLUSIONS

This paper described a theoretical and experimental study on a Full-Bridge ZVS-PWM topology operating as series-connected partial-power converter (S-PPC) applied to small wind turbine (SWT) systems connected in the grid. The main advantages of this structure are related to the fraction of power processed by the converter, which increases the overall efficiency and reduces the total losses of the system, since a part of the input power is directly transferred to the output with unitary efficiency and no conversion stage.

Knowing the mechanical parameters of SWT model Gerar 246, manufactured by Enersud, the operating range of rotational speed and output voltage/power levels of the rectifier stage was defined. Thus, the input voltage range of Full-Bridge ZVS-PWM S-PPC converter was specified, which determined the active power range processed by the dc-dc converter, as well as the direct power flow range from input to output.

In order to corroborate the theoretical analysis and evaluate the performance of the proposed structure, a workbench was designed, built, and tested. The experimental results showed for a 1.5 kW SWT corroborate the partial-power processing concept, since the Full-Bridge ZVS-PWM S-PPC processed 70 % of the generated power by the SWT, while 30 % flows directly from the rectifier to the dc bus. The overall efficiency obtained experimentally was above 96 % for a wide load range, reaching 96.5 % of efficiency peak. In terms of energy processing, the partial-power processing reduces the losses in 35.97% at rated power in relation to the full-power processing. Also, the proposed system (rectifier, dc-dc converter, and inverter) was tested with grid-connection, with a startup routine of control loops and protections. With a view to reduce even more the active power processed by the dc-dc

converter and increases the efficiency, SWT with higher output voltages should be employed.

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