AN IMPROVED METHODOLOGY FOR SWITCHING LOSSES ESTIMATION IN SiC MOSFETs

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***Abstract* – This work presents an improved analytical model concerning the prediction of switching losses in power MOSFETs by considering the influence of parasitic elements in the high-frequency operation of devices. By using the transistor voltage and current waveforms, it is possible to predict switching losses under hard-switching conditions adopting only parameters that can be obtained from the device datasheet. The method employs the nonlinearities associated with the junction capacitances, which are incorporated into the model through curve fitting. Besides, the sensitivity analysis is used to identify which parameters have a major influence on the estimated losses. The methodology is described in details and verified by means of experimental results concerning a SiC MOSFET, which is tested under various current and voltage conditions.**

***Keywords* – Power MOSFET, Sensitivity analysis, Silicon carbide, Switching losses prediction**

NOMENCLATURE

C_{ak}	Diode Capacitance.
C_{GD}	Gate-drain capacitance.
C_{GS}	Gate-source capacitance.
C_{iss}	Input capacitance.
C_{oss}	Output capacitance.
C_{rss}	Reverse transfer Capacitance.
E_{ins}	Instantaneous energy.
g_{fs}	MOSFET Transconductance.
i_D	Drain current.
I_{dd}	Load current.
i_G	Gate current.
L_s	Source inductance.
L_d	Drain inductance.
P	Instantaneous power.
R_g	Total gate resistance.
$R_{g(int)}$	Internal gate resistance.
$R_{g(int)}$	External gate resistance.
V_{ak}	Schottky diode voltage.
V_{dd}	Input voltage.
v_{DS}	Drain-source voltage.
v_{GD}	Gate-drain voltage.
V_{gg}	Voltage driver.
$V_{gg(on)}$	High-level for turn-on the MOSFET.
$V_{gg(off)}$	Low-level for turn-off the MOSFET.
v_{GS}	Gate-source voltage.
V_{pl}	Miller plateau voltage.

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I. INTRODUCTION

The choice of a power transistor for a given application depends not only on the voltage and current levels required but also on the switching characteristics. Currently, the silicon power metal-oxide-semiconductor field-effect transistor (MOSFET) is one of the most used semiconductor devices in low to medium-powered high-frequency power processing applications [1], [2]. More recently, wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC) MOSFETs and diodes, as well as gallium nitride power FETs (GaN FET) offer several noteworthy physical properties that have conquered the interest of manufacturers and product designers [3]. In this context, the aspects addressed to such devices are increased power density, high voltage withstanding capability, fast switching characteristics, and high-temperature operation without losing efficiency [4], [5].

The estimation or calculation of the switching losses in power MOSFETs has been extensively investigated in the technical literature although it is not yet consolidated because of the inaccuracy or the complexity of some prediction methods. Therefore, a reliable and more accurate model to evaluate the switching and conduction losses in such components becomes crucial for the design, sizing, and implementation of the main types of static converters [6], [7]. A more accurate assessment of such losses can reduce the design and optimization time of a static converter without needing to build various prototypes for experimental comparison purposes.

There is a variety of methods for switching losses estimation. Physical models use finite-element simulations and report best results, but they could take a few days to simulate a complete static converter [8]. Behavioral models use circuit simulation software such as SPICE and are faster than physical models, but show long execution times when associated with small timesteps. In addition, they present large errors when compared to the experimental results. Alternatively, MOSFET switching losses can be calculated using analytical models, which are mathematical models based on equal circuits that use parameters from the device datasheet or obtained by measurements. Some approaches are based on the calculation of turn-on time and turn-off time, while stray inductances and parasitic capacitances are often neglected [6], [7], [9]. Typically, such models state that turn-on and turn-off losses are nearly equal. However, if a real converter is operating at a high switching frequency, this assumption is highly inaccurate since turn-off losses are greater than turn-on losses due to parasitic inductances.

Seeking for improved accuracy, some authors have addressed the dynamic behavior of a power transistor in terms of operating stages [7], [10]–[13]. A common characteristic, in this case, is that the switching cycle is divided into several time intervals. In this context, the turn-on and turn-off intervals are constituted by multiple stages associated to a typical switching circuit.

The method proposed by Ahmed et al. [12] is adopted as the basis for this work. This choice is due to the accurate results which can be attained by this method, as stated in [13]. In this case, the Ahmed method takes into account some circuit-level analytical models for hard-switching transients, consequently improving its accuracy. The model includes the main circuit parasitic elements, such as the parasitic inductances in the commutation loops, L_d and L_s, as well as parasitic capacitances, such as input capacitance, output capacitance, and transfer reverse capacitance of the MOSFET (C_{iss}, C_{oss}, and C_{rss}, respectively).

It is worth mentioning that the numerical calculation of the switching losses requires the knowledge of many important input parameters, *e.g.*, the source inductance, the drain inductance, the total gate resistance R_g, the threshold voltage V_{th}, and transconductance g_{fs}. The aforementioned quantities often present uncertainties associated with measurement and parametric variation within a specified range, which are normally defined in the datasheet device. A wrong choice of these parameters can lead to an unrealistic estimation of losses. Thus, one of the main contributions of this work is to present a sensitivity analysis and identify which input parameters have the strongest influence on the performance of the predicted switching losses. Finally, a more accurate methodology for the parameter extraction is also presented, thus leading to a remarkable improvement of the predicted results when compared with experimental measurements.

This paper is organized as follows: Section II outlines the prediction method for power MOSFET switching losses considering the parasitic elements in the double-pulse test circuit (DPT circuit) [12]. Section III presents a sensitivity analysis of inaccuracy and uncertainties of the input parameters within the method previously mentioned. Section IV explains the procedures to obtain the threshold voltage by using a curve provided in the datasheet. To validate the proposed switching loss model, experimental results obtained from the double-pulse circuit in different operating conditions using a SiC power MOSFET are discussed in section V. Finally, the main conclusions of this work are highlighted in Section VI.

II. OVERVIEW OF POWER MOSFET HARD-SWITCHING TRANSIENTS

As mentioned before, the Ahmed *et al.* method is presented in [12] and adopt a similar approach as described in [10], with the difference of the incorporation of the major circuit parasitic components in all the transient stages. Additionally, a more accurate method that includes the influence of junction capacitance using the curves provided in the device datasheet is used.

To investigate hard-switching, the double-pulse test circuit as shown in Figure 1.a is the preferred test method to measure the switching parameters of MOSFETs or IGBTs is the double-pulse-test method. It is also adopted by most semiconductor switches manufacturers. The switching cell of a DPT circuit represents a typical PWM hard-switching power converter feeding or being fed by an inductive branch, which is a common condition in most PWM converters. By looking at turn-on and turn-off transitions, engineers can thoroughly evaluate the dynamic behaviors of power devices under a range of conditions. Furthermore, it is possible to analyze the MOSFET behavior in any combination of current level and input voltage, without significant variation in the junction temperature of the device. The DPT circuit includes the main circuit parasitic elements, such as the MOSFET common source inductance ($L_s + L_d$), drain inductance, as well as the parasitic capacitances of the MOSFET C_{GS}, C_{GD}, and C_{DS}. Other elements of the DPT circuit are also taken into consideration, such as the Shottky diode, D_s, the lumped parasitic capacitance of the load, C_{ak}, and the equivalent resistance of the power loop, R_s. In addition, Figure 1.b shows simplified turn-on waveforms for the generic power SiC MOSFET, including drain-to-source voltage v_{DS}, drain current i_D, gate-to-source voltage v_{GS} and the Schottky diode voltage, V_{ak}.

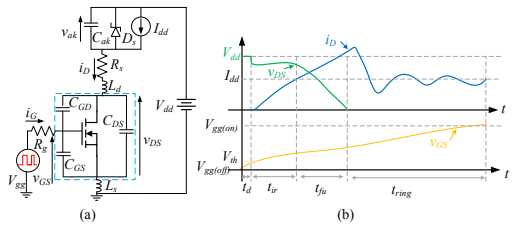


Fig. 1. (a) Equivalent circuit of DPT circuit of SiC MOSFET and (b) DPT circuit waveforms during turn-on transient.

For modeling the power MOSFET turn-on and turn-off transients it is required the solution of four subcircuits corresponding to the four distinct stages of each transient as shown in Figure 2. The four subperiods during the turn-on transient are turn-on delay, drain current rise, drain-source voltage fall, and ringing stages, respectively. In this analysis, the gate inductance L_g was neglected because of its small value when compared with the power loop inductances L_s and L_d.
1) Subperiod 1 (t_d – turn-on delay)(Figure 1.b and Figure 2.a): After pulse gate swings from $V_{gg(off)}$ to $V_{gg(on)}$, i_G charges the MOSFET input capacitances C_{GS} and C_{GD}. The MOSFET stays off until v_{GS} reaches V_{th} and I_{dd} flows through the freewheeling diode. The expressions that describe this subperiod are stated in (1) to (5).

$$R_g \cdot i_G + v_{GS} + L_s \cdot \frac{di_D}{dt} + L_s \cdot \frac{di_G}{dt} = V_{gg(on)}. \tag{1}$$

$$\frac{dv_{GS}}{dt} = \frac{i_G}{C_{iss}} = \frac{i_G}{C_{GS} + C_{GD}}. \tag{2}$$

$$v_{GS} = v_{GD} + v_{DS}. \tag{3}$$

$$C_{iss} = C_{GS} + C_{DS}. \tag{4}$$

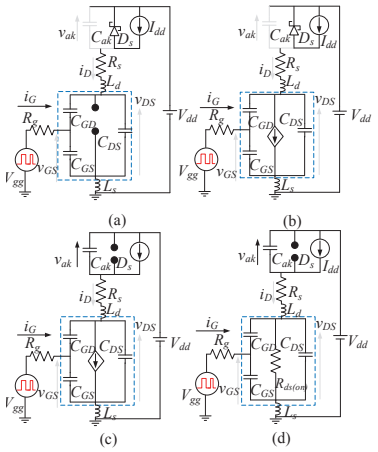


Fig. 2. Equivalent circuits for turn-on and turn-off sub-periods corresponding to the hard-switching DPT circuit (a) subperiod 1 (turn-on delay); (b) subperiod 2 (Current Rise Time); (c) subperiod 3 (Voltage Fall Time), and (d) subperiod 4 (Ringing Period), adapted from [12].

$$\left(\frac{-v_{GS}-R_g i_G+V_{gg(on)}}{L_s}\right)=\frac{d_{i_G}}{dt}. \tag{5}$$

2) Subperiod 2 (t_{ir} – current rise time) (Figure 1.b and Figure 2.b): The current commutation between the diode and MOSFET is characterized in this stage. As the MOSFET is in the saturation region, its channel current will be proportional to the difference between the gate to source voltage and the threshold voltage ($v_{GS}-V_{th}$). The current rise time is the time required for v_{GS} to reach the Miller plateau voltage, V_{pl}, where $V_{pl}=I_{dd}/g_{fs}+V_{th}$ and g_{fs} is the transconductance of the MOSFET. The expressions that describe this subperiod are presented in (6) to (9).

$$v_{DS}=V_{dd}-(L_s+L_d)\cdot\frac{di_D}{dt}-R_s\cdot i_D. \tag{6}$$

$$i_D=g_{fs}\cdot(v_{GS}-V_{th})+C_{oss}\cdot\frac{dv_{DS}}{dt}. \tag{7}$$

where,

$$C_{oss}=C_{DS}+C_{GD}. \tag{8}$$

$$R_g\cdot i_G=V_{gg(on)}-v_{GS}-L_s\frac{di_D}{dt}. \tag{9}$$

3) Subperiod 3 (t_{fu} – voltage fall time) (Figure 1.b and Figure 2.c): The voltage fall time is the time required for v_{DS} to reach $V_{ds(on)}$, which is derived by the product i_D times $R_{ds(on)}$.The expressions that describe this subperiod are presented in (10) and (11).

$$\frac{dv_{ak}}{dt}=\frac{1}{C_{ak}}\cdot(i_D+I_{dd}). \tag{10}$$

$$V_{dd}-(L_s+L_d)\frac{di_D}{dt}-v_{ak}-R_s\cdot i_D=v_{DS}. \tag{11}$$

4) Subperiod 4 (t_{ring} – ringing period) (Figure 1.b and Figure 2.d): It is considered the time to overcharge the input capacitance, C_{iss}, and to completely turn-on the gate channel. The expressions that describe this subperiod are presented in (2), (5), and (9)–(12).

$$\frac{v_{DS}}{R_{ds(on)}}+C_{oss}\frac{dv_{DS}}{dt}=i_D. \tag{12}$$

Regarding the switching turn-off stages, the events occur similarly to the switching turn-on stages, although the circuit should be analyzed in the opposite way. The detailed modeling will be suppressed here, as it can be found in [12].

A. Model Implementation

Figure 3 presents the flowchart of the turn-on solution process.

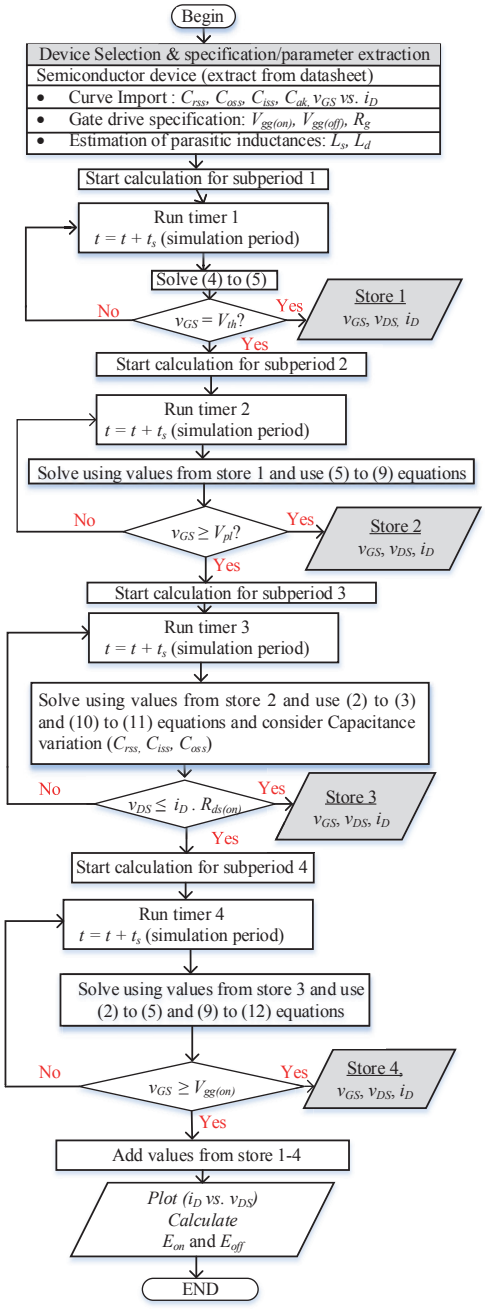


Fig. 3. Flowchart for calculating the MOSFET turn-on losses.

At first, the previous declared set of equations (1)-(12) are organized in the form of a state-space system. This system is, then, solved by means of a MATLAB function named

"ode45". This function returns a time-dependent solution vector concerning the desired set of system variables. Those vectors are associated to a correspondent transition stage, which depends on specific process conditions. After the conclusion of a given stage solution, its vector of values is used to feed up the subsequent stage calculation. It is worth mentioning that the prediction of switching losses value is an offline method. Thus, the required variables and some parameters are provided at the beginning of calculation, as shown in the flowchart of Figure 4, so that typical values are used. On the other hand, the value of V_{th} is previously calculated according to the methodology that will be described in section IV. Furthermore, it is important to emphasize that during the subintervals where the drain-source voltage changes abruptly (*i.e.* high dv/dt occurrences), namely the subperiod 3, it is required to discretize the parasitic capacitances C_{iss}, C_{oss} and C_{rss}. Those voltage quick transitions take place because of the nonlinear nature of the capacitances. Hence, the capacitance discretized values are used to lead the process solution to its stop condition.

Upon the complete calculation of all the transition stages, the whole turn-on or turn-off solution, *i.e.*, the time behaviours of drain current, $i_D(t)$, and drain-to-source voltage, $v_{DS}(t)$, are obtained by merging the correspondent subinterval solutions. Finally, the energies related to the switching losses, E_{on} and E_{off}, are calculated by integrating the result of the product of $i_D(t) \cdot v_{DS}(t)$ using the trapezoidal numeric method, as shown in (13) and represented in Figure 4.

$$E_{inst}(i) = \frac{(p(i)+p(i+1))\Delta t}{2} + E_{inst}(i-1). \qquad (13)$$

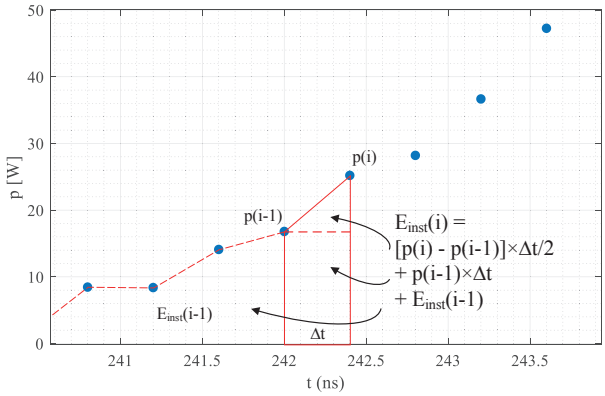


Fig. 4. Interactive calculation of accumulated instantaneous energy.

III. SENSITIVY ANALYSIS

The method proposed in [12] presents significant relative errors in some operating conditions. The main sources of error are the inaccuracy and uncertainty of the input parameters obtained from the device datasheet. Therefore, it is essential to evaluate the influence of such parameters on the results provided by the mathematical models used to estimate the switching losses in power MOSFETs. In this context, this section presents the study of the relative sensitivity regarding the method used to estimate the switching losses with respect to different sources of uncertainty, by varying them according to typical specific ranges. In this work, a SiC MOSFET (SCT3120AL) is used as an example in the sensitivity analysis.

The main evaluated parameters with their range of values are listed in Table I. It can be seen from the data in Table I that the transconductance, threshold voltage, and gate resistance parameters were extracted from the device datasheet, while the values of drain inductance and source inductance have been considered twice the measured value as the greatest value. It worth to mentioning that R_g is given by

$$R_g = R_{g(\text{int})} + R_{g(ext)}, \qquad (14)$$

where $R_{g(\text{int})}$ is the internal gate resistance and $R_{g(\text{ext})}$ is the external gate resistance.

The parasitic inductances L_s and L_d are strongly dependent on the design of the PCB and the arrangement of the components as well as the internal bonding of the die. Usually, the parasitic inductances introduced by the loops in the commutation path as well as in the connection of the gate drive are minimized to achieve high performance. In this paper, the power circuit parasitic values were measured using a precision impedance analyzer, from Agilent E4980A and the values were close to those adopted in [12] and [14]. Those conditions contribute to a fair comparison between the Ahmed method and the one proposed in this paper.

TABLE I
SiC MOSFET SCT3120AL Evaluated Parameters

MOSFET	Range of the evaluated parameters				
	L_d [nH]	L_s [nH]	g_{fs} [S]	V_{th} [V]	$R_{g(ext)}$ [Ω]
SCT3120AL	0 – 40	0 – 10	0.5 – 5.6	2.7 – 5.6	10 – 15
Base Value	20	5	2.7	4.15	10

Each parameter is normalized according to its respective base value, as defined in the following expression:

$$\overline{X}_{norm} = \frac{X}{X_b}. \qquad (15)$$

where X represents the parameter being evaluated, X_b is the base value, and $\overline{X}_{norm}$ is the normalized value. The sensitivity relates the influence that the uncertainties of the MOSFET input parameters cause in the total losses E_{sw}. The calculation of the parameter sensitivity (X_{sens}) is performed by the following equation:

$$X_{sens} = \frac{(E_{\max} - E_{\min})/E_{base}}{\overline{X}_{norm(\max)} - \overline{X}_{norm(\min)}}. \qquad (16)$$

where E_{max} and E_{min} are the greatest and least values of the given switching characteristic, respectively; $\overline{X}_{norm(max)}$ and $\overline{X}_{norm(min)}$ are the greatest and least normalized parameter values, and E_{base} corresponds to the energy value at X_b. It is important to notice that E_{base} is used to normalize the switching characteristic values, being X_{sens} a dimensionless quantity.

Figure 5 depicts the influence of each evaluated parameter on the estimated switching energy, E_{sw}, given in joules. It is important to highlight that for the switching losses evaluation of a certain parameter, the other ones were kept constant and

equivalent to their nominal values.

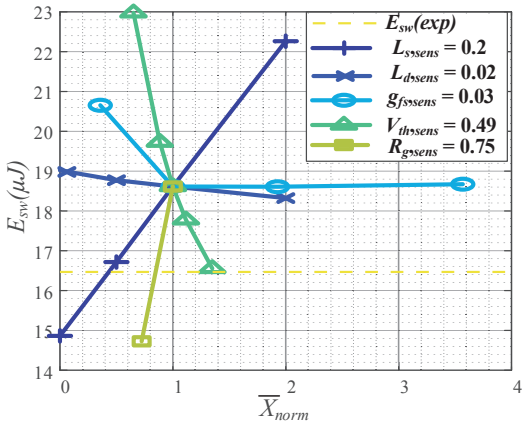


Fig. 5. Sensitivity analysis of the total switching losses E_{sw} with respect to the varied parameters in MOSFET SCT3120AL (evaluated parameters are according to Table I).

The results shown in Figure 5 for the MOSFET SCT3120AL indicate that the most sensitive parameters are $L_{s,sens} = 0.2$, $V_{th,sens} = 0.49$, and $R_{g,sens} = 0.75$, which are higher than those associated with the other parameters. For example, the transconductance and drain inductance, presented a much lower sensitivity of 0.03 and 0.02, respectively. The source inductance tends to have a high influence on the analyzed method. On the other hand, the drain inductance presented minor relative sensitivity values. The sensitivity analysis was also tested using different current and voltage levels, being the results very similiar to that in Figure 5. Therefore, it is important to determine the threshold voltage and source inductance as accurate as possible to decrease the errors associated with the switching loss estimation.

IV. METHODOLOGY FOR THRESHOLD VOLTAGE CALCULATION

As previously demonstrated, the threshold voltage is essential for determining the switching losses in power transistors. Since V_{th} has a predominant effect on the circuit operation, it is often used to monitor process variations. Thus, the choice of a higher or lower threshold voltage value may result in the crossing of voltages and current at incorrect points, which will substantially impair the switching losses calculation.

During switching transitions, the MOSFET device swings from cutt-off to triode region, passing by saturation mode (pinch-off). In this operating region, the threshold voltage is a function of the MOSFET drain current [15], which can be expressed as

$$i_D = g_{fs} \cdot (v_{GS} - V_{th})^2. \tag{17}$$

where,

$$g_{fs} = \mu_n \cdot C_{ox} \cdot \frac{W}{2L}. \tag{18}$$

and C_{ox} is the oxide capacitance per unit area, W is the channel width, L is the effective free-carrier mobility, and μ_n is directly related to the mobility of majority carriers (which are electrons, in this case of NMOS device). Some of these constructive parameters are not available in most datasheets. So, an alternative methodology must be used in order to calculate V_{th}, which can be estimated more accurately by using the v_{GS}-to-i_D transfer curve provided in the device datasheet. In order to exemplify this novel methodology, the v_{GS} vs. i_D typical curve obtained from the device datasheet MOSFET SCT3120AL, at 25° C, is depicted in Figure 6 [16].

At this point, it is important to emphasize that the authors of [12] consider the typical values of threshold voltage in the calculation of losses. However, according to the manufacturer's datasheet, the value of the threshold voltage varies with the current applied to the device as is shown in Figure 6. The graph shows that the simplified assumption performed in [12] can lead to significant error levels since the typical value provided by the device datasheet corresponds to a specific operating condition, which dramatically differs from the application that is under investigation. Therefore, by considering the large influence of V_{th} in the losses calculation, it is necessary to determine this parameter with a more accurate procedure, which takes into account the application specificities. The methodology used for the extraction of the threshold voltage is based on [16]. Besides, it is important to mention that the methodology adopted in this work considers the rated current.

The following steps summarize the process of obtaining the threshold voltage:
Step 1: Import the transfer curve using curve-fitting software. (In this work it was used the "digitize.m" Matlab function);
Step 2: Define a project current, *i.e*, the drain current, i_D;
Step 3: Choose two read points between the rated current and record the corresponding drain currents as well as gate-to-source voltages;
Step 4: Select the drain currents corresponding to the vertical grid lines in the graph;
Step 5: Use (19) and the current values (i_{D1}, i_{D2}) corresponding to v_{GS1} and v_{GS2}, respectively, to estimate the mean value of V_{th}.

So, the threshold voltage can be calculated by

$$V_{th} = \frac{v_{GS1} \cdot \sqrt{i_{D2}} - v_{GS2} \cdot \sqrt{i_{D1}}}{\sqrt{i_{D2}} - \sqrt{i_{D1}}}. \tag{19}$$

It is common for manufacturers to make two $i_D \times v_{GS}$ curves available for two different temperatures. From these curves, it is possible to calculate the temperature coefficient, k_T, which relates the variation of the threshold voltage with temperature according to

$$\frac{\Delta V_{th}}{\Delta T_k} = k_T \cdot \tag{20}$$

By using to the electrothermal equation presented in (20), temperature effects can also be taken into account and incorporated in the model, if desired. Moreover, it is important to note that the threshold voltage decreases as the temperature increases.

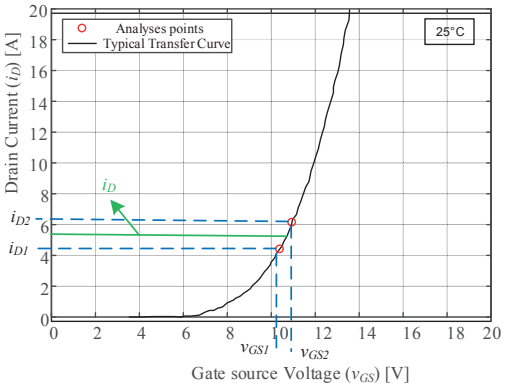
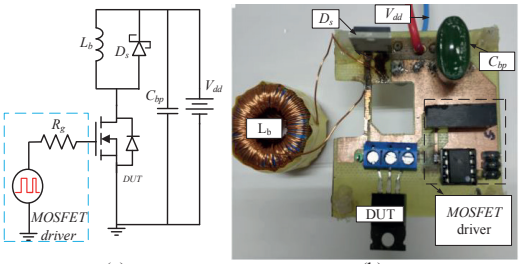


Fig. 6. Methodology to calculate V_{th} using typical transfer curve of $(i_D)vs.(V_{GS})$.

V. EXPERIMENTAL RESULTS AND DISCUSSION

In order to validate the proposed methodology, a laboratory setup based on the double-pulse circuit has been developed aiming at a thorough comparison between the experimental and the theoretical prediction of the switching losses in power MOSFETs [7].Figure 7 shows the schematic, a photograph of the printed-circuit board (PCB) and the key elements used in the experiment as summarized in Table II.



(a) (b)

Fig. 7. Experimental setup of a double-pulse circuit. (a) schematic and (b) PCB picture.

TABLE II
Parameter and Parasitic Values

Section	Parameter	Value
Power circuit	V_{dd}	100 – 300V
	I_{dd}	1 – 10 A
	L_d	20 nH
	L_s	5 nH
	C_{bp}	1920 nF
	L_b	4.67 mH
Gate driver circuit	$V_{gg(on)}$	18 V
	$R_{g(in)} + R_{g(ext)}$	(18 + 10) Ω
SiC MOSFET (SCT3120AL)	$R_{ds(on)}$	120 mΩ
	g_{fs}	2.7 S
Shottky Diode (C3D16065A)	r_d	60 mΩ
	V_F	1.5 V

In this circuit, the driver was placed on the board to reduce the influence of parasitics. So, it is located as close as possible to the DUT (device under test). In this board, a proper windowed hole was made in the PCB board to fit the current probe so that it was not necessary to add external wiring for measuring the DUT current. Furthermore, a SiC freewheeling diode, D_s, with a small reverse recovery charge is used to avoid affecting the overall MOSFET switching losses. Multiple ceramic capacitors (480 nF, 600 V), C_{bp}, are placed in parallel to further reduce the equivalent stray inductance (these are arranged on the bottom layer of the board). High-bandwidth passive probes (500 MHz) have been used to sense v_{DS} and v_{GS}, respectively and TCP305 currrent probe to sense i_D (please, note the proper hole in the printed circuit board close to the device connector at Figure 7b). The gating schemes were implemented digitally with an FPGA Development Kit Altera DE0-Nano. It is worth mentioning that a deskew procedure had to be performed in the oscilloscope Tektronix (DPO3014) to compensate for the different propagation delays between the probe measurements regarding the drain-to-source voltage and drain current. For the analysis and losses calculation, the data gathered by the oscilloscope, concerning v_{DS}, v_{GS} and i_D signals, are stored and processed by a personal computer using MATLAB routines. A function was created in this software tool aiming the analysis of the collected data for a specific sample set and to return the desired information regarding the DUT energy losses.

Concerning the electrothermal characterization, the experimental setup proposed is shown in Figure 8. This experiment employs the DUT and a Peltier board [17], which keeps the MOSFET electrical parameters at the same temperature conditions as defined in the datasheet. The Peltier board temperature control was performed by means of a dc voltage power supply with the aid of an external monitoring thermometer. In this analysis, several values of the junction temperature can be achieved. It is important to emphasize that the thermal steady-state behavior must be assumed for each measurement, which ensures $T_j \approx T_a$, ambient temperature.

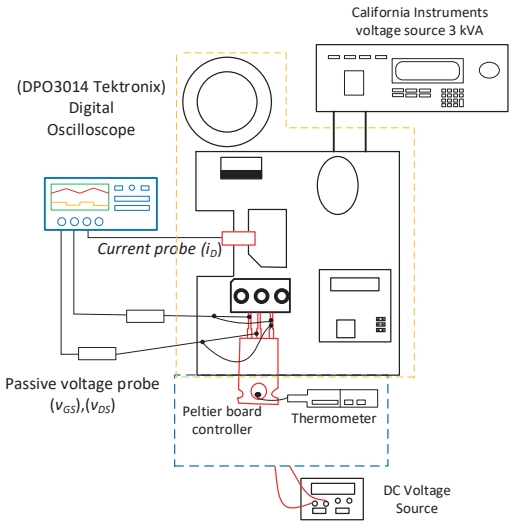


Fig. 8. Experimental setup employed for switching losses characterizations.

Figure 9 shows a comparison between the proposed methodology and the one proposed in [12]. It is important to notice that the comparison of the proposed method and the

Ahmed approach can be considered fair enough because the source inductance (5 nH) and the drain inductance (20 nH) were the same in both works. By analyzing the results, one can see that the proposed methodology yields a theoretical prediction that is closer to the experimental waveforms, achieving higher accuracy for several test conditions. It is important to mention that the improvement in the definition of V_{th} was essential better to predict the stage times, which allowed for better overall accuracy. This improvement can also be observed in the losses prediction, which was better than the technique proposed in [12], as can be seen in Table III.

One can note that for the evaluated conditions, the error of the proposed methodology is less than 15% in most cases, being at most 22.8% for each loss and around 18% for the total switching losses. In addition, the last column of the table presents the improvement obtained when using the refinement of V_{th} defined by the percentage difference between the proposed method and Ahmed method [12]. It is possible to see that the proposed methodology allowed for accuracy of up to 30% higher for the evaluated cases. Also, the DPT circuit was tested using higher and lower gate resistances and the percentage errors in the predicted switching losses were found to be likewise those in Figure 9.

Moreover, the proposed method can provide a good prediction of the DPT circuit transient response, during turn-on and turn-off intervals, with smooth behaviors of current and voltages, in a similar way as the Ahmed's method. In order to further evaluate the improved method, some tests were performed at two different temperatures (25°C and 50°C) for a range of currents. The main temperature-sensitive parameters are the on-resistance and the device transconductance, both with a positive temperature coefficient, as well as the threshold voltage, which has a negative temperature coefficient [12].The behavior of the aforementioned parameters according to the temperature are available in some device datasheets, however, some manufacturers do not provide such curves, so that they must be obtained experimentally. Once the expressions $g_m(T_{jc})$,$V_{th}(T\,jc)$ and $R_{ds(on)}(T_{jc})$ are known, they can be used to correctly determine the values of the device transconductance, threshold voltage and on-resistance at a certain operating temperature, respectively. Figure 10 presents the calculation switching losses (turn-on and turn-off) and (total) experimental switching losses for two different temperature levels, of 25° and 50° with V_{dd} fixed at 250 V. One can note that the value of turn-on losses reduces (Figure 10a) and turn-off losses are increases (Figure 10b) as the junction temperature increases. As expected, the turn-on losses have been reduced and turn-off losses are increased with the high junction temperature (consistent with the MOSFET datasheet) [18]. It is important to emphasize that the proposed model provides acceptable prediction of the device switching losses for both temperature ranges, *i.e*, at 25 °C and 50 °C. The experimental setup employed a Peltier board (TEC1-12706 by HB Corporation), which was limited to some specific supply current, voltage and temperature ranges, so that authors have opted to not reach temperatures greater than 50 °C for safety reasons. Anyway, the model has presented a good behavior considering the temperature variation and can be extended to other temperatures by changing the temperature-dependent parameters, such as the MOSFET transconductance, threshold voltage and on-resistance.

inally, it is important to emphasize that the experimental setup and assessment have produced good confidence in results. Concerning the tests, this work includes the results on five samples of a single SiC Mosfet commercial brand, the SCT1320AL of Rohm Semiconductor. Those units have been tested at least three times each and the losses average error revealed to be less than 5%, which can be considered fairly acceptable. Regarding the DUT connection, it is important to mention that although it adds some parasitic elements to the test circuit, those conditions did not impair the comparison between the Ahmed method [12] with the method proposed in this paper.

VI. CONCLUSION

This paper has presented a methodology for refining the accuracy of switching losses estimation by improving the analytical model presented in [12]. As a result of the sensitivity analysis included at the beginning of the paper, it has been verified that the MOSFET threshold voltage, V_{th}, is one of the parameters that most influence the estimation error. A second contribution was the proposal of an alternative methodology for calculating V_{th} based only on the device datasheet information. According to the results, it was possible to verify that the calculation of V_{th} as a function of the current variation, and not a fixed value (typical value) as used in Ahmed method, brings significant improvements as shown in Table 3. In this context, a straightforward and reproductive methodology has been introduced to get the threshold voltage in a more accurate way using only the transfer characteristic provided in the device datasheet. Another significant contribution lies in the fact that it is possible to estimate switching losses in power MOSFETs without the use of complex circuitry and experimental setups.

Lastly, it is important to notice that the analytical methods provide a straightforward mechanism to obtain a first insight regarding the switching losses with an acceptable convergence time (less than 1 min *). On the other hand, physical-based models, which employ special computer techniques, may offer much better accurate results, though require intensive computational efforts and need detailed information on physical material properties being not very suitable for circuit simulation. Moreover, as reported in [7], those methods may require a few days to simulate a complete static converter. Thus, they are more likely to be used by engineers for project optimization and device development.

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*Intel Core i5 2.3 GHz computer

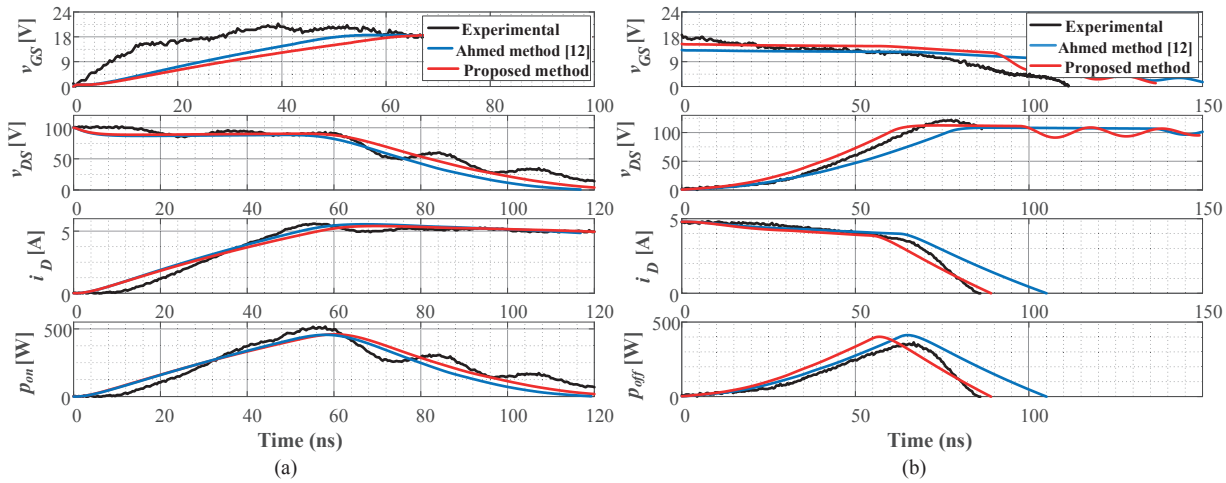

Fig. 9. Measured and predicted results with SIC MOSFET SCTAL3120 at $T_j = 25°$ during (a) turn-on and (b) turn-off (100 V, 5 A).

TABLE III
Switching Loss Comparison at 25°C Operation Analytical and Experimental Methods

Conditions	State	Loss (μJ)			
		Exp.	Ahmed (%error)	Proposed method (%error)	Accuracy Improvement (%)
(100 V-2A)	*Turn-on*	5.79	5.69 (−1.73%)	5.74 (−0.86%)	0.87%
	Turn-off	4.00	4.27 (6.75%)	4.12 (+3.00%)	3.75%
	Total	9.79	9.96 (+1.74%)	9.86 (+0.72%)	1.02%
(100 V-5A)	*Turn-on*	32.41	22.38 (−30.95%)	27.42 (−15.39%)	15.55%
	Turn-off	13.12	18.60 (+41.77%)	15.47 (+17.91%)	23.85%
	total	45.53	40.98 (−9.99%)	42.89 (−4.7%)	4.19%
(150 V-5A)	*Turn-on*	36.90	26.39 (−28.48%)	35.34 (−4.24%)	24.26%
	Turn-off	20.14	35.80 (+77.75%)	22.15 (9.98%)	67.78%
	Total	57.04	62.19 (+9.02%)	57.49 (+0.79%)	8.24%
(300 V-6A)	*Turn-on*	83.72	69.20 (−17.34%)	72.42 (−13.50%)	3.84%
	Turn-off	59.97	106.87 (+78.20%)	96.39 (+60.73%)	17.47%
	Total	143.69	176.07 (+22.53%)	168.81 (+17.48%)	5.05%

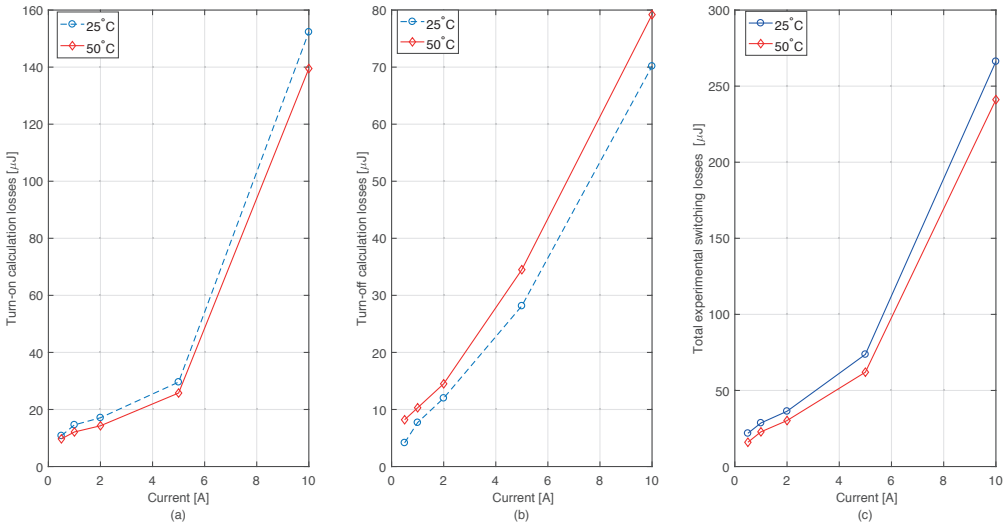

Fig. 10. (a) Calculated turn-on losses (b) Calculated turn-off losses and (c) Total experimental switching losses for different currents for T_j =25C and 50C @ V_{dd} =250 V.

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