HYBRID DUAL-LOOP CONTROL FOR CURRENT REGULATION AND LOW-FREQUENCY RIPPLE REJECTION IN LED DRIVERS

Maikel F. Menke[1,2], J. Marcos Alonso[3], Rodrigo V. Tambara[1], Álysson R. Seidel[1]
[1]Federal Institute of Santa Catarina, Florianópolis – SC, Brazil
[2]Federal University of Santa Maria, Santa Maria – RS, Brazil
[3]University of Oviedo, Gijón, Astúrias, Spain
e-mail: maikel.menke@ifsc.edu.br

Abstract – This paper presents a new hybrid dual-loop control system for the DC/DC LLC resonant converter, operating as a downstream DC/DC converter in a two independent stage offline LED driver. The outer loop employs a PI controller to maintain the average LED current regulated at the reference value and reject parametric variation. The inner loop implements an adaptive periodic disturbance rejection (APDR) subsystem, thus conceiving the hybrid PI&APDR controller. The APDR subsystem is designed to strictly reject the bus voltage ripple and limit its transmission to the LED current. Experimental results show the proposed controller feasibility in achieving good tracking behavior, reduced output current ripple under different bus voltage ripple amplitude and frequency, robustness against parametric variations, and simple implementation and design. For the sake of completeness, the proposed PI&APDR is compared with the conventional proportional resonant controller employing experimental results and extra analysis based on simulations.

Keywords – Current Ripple reduction, Dual-loop control, Hybrid control, LED driver, LLC resonant converter.

I. INTRODUCTION

Artificial lighting systems (ALS) have been widely discussed in the literature, where currently, light-emitting diodes (LED) are accepted as the most efficient, flexible, and reliable electric light source [1], [2]. Owing to the LED output light direct relationship with its forward current, and its voltage source electrical behavior, combined with the necessity to present a regulated average current to perform dimming and reduced current ripple to avoid flicker [3], the LED driver has to be designed as a current-controlled system to properly supply the LED load [4]. For high-performance medium-to-high power (>70 W) applications, offline LED drivers are usually implemented by a two independent stage structure, given by the AC/DC front-end power factor correction (PFC) stage followed by a DC/DC current controlled converter with isolated output, where a DC-link capacitor (C_{BUS}) decouples both stages [5].

Among several topologies, the half-bridge (HB) LLC resonant converter with full-wave rectifier is becoming the usual choice to implement the DC/DC stage in the offline LED driver because of its characteristics, which provides a wide operating range with high efficiency, together with the high power density and low EMI [6]–[10]. Besides, LLC features also match with the amplitude modulation (AM) dimming method, usually employed in medium-to-high power due to its simplicity in comparison to pulse-width modulation (PWM) dimming method.

To enhance the offline LED driver reliability, the C_{BUS} bulky electrolytic capacitors (E-Cap) are being substituted by long lifespan film capacitors (F-Cap) [1], [11]. However, usually reduced capacitance values are employed to avoid volume and cost increases due to the low energy density of F-Cap, which causes the negative effect of producing a higher bus voltage ripple (ΔV_{BUS}). To avoid that ΔV_{BUS} excite throughout the DC/DC stage a low-frequency (LF) output LED current ripple (ΔI_{LED}) and so deteriorate the ALS operation due to the resultant flicker, several studies propose to design the control system of the DC/DC stage in the way to satisfactory reject ΔV_{BUS} disturbance [12], [13].

Employing classical control theory, in [14] the Integrator Quasi-resonant (IQR) controller is designed for the LLC LED driver to achieve reduced ΔI_{LED} over a wide dimming range even with a considerable ΔV_{BUS} at 120 Hz. Similarly, in [15] a proportional-integral resonant (PIR) controller is employed to suppress the LF output current ripple (ΔI_O) in an LLC based electrical vehicle battery charger. Investigating the mechanism of ΔI_O propagation in a digitally controlled LLC converter, in [16] the synchronous frequency dither is proposed to reduce the quantization error and attenuate ΔI_O. Without compromise with ΔI_O reduction, a three-pole two-zero (3P2Z) controller is designed in [17] and [18] to assure stability and good performance for the LLC converter over a wide operation range. Notwithstanding, all these approaches based on classical control theory are subjected to an unpredictable and deteriorated performance when the converter is exposed to a wide operating range, since linear controllers, such as Proportional-Integral (PI), IQR, PIR, 3P2Z, and PID are only valid near a particular operating point due to limitations of the employed small-signal models [19].

To overcame small-signal model limitations, nonlinear controllers have been proposed in the literature presenting strong robustness against disturbances, parameters uncertainties, parametric variation, unmodelled dynamics, and load variations. Specifically, to control the DC/DC LLC converter, sliding-mode control is proposed in [20], bang-bang control in [21], robust control in [22], model reference adaptive control (MRAC) in [23], and optimal

trajectory control in [24]. To improve the nonlinear controllers' performance in rejecting periodic disturbances, the adaptive periodic disturbance rejection (APDR) controller has been developed for active noise and vibration control applications [25]–[27]. Nevertheless, compared to the linear compensation, the nonlinear controller's performance is still undesirable either in terms of dynamic response or steady-state or ΔI_O reduction. Besides, these nonlinear techniques usually require further computations to be carried out during the control-law execution cycle, or the computations need to be done at the converter's switching frequency (f_{sw}), which is usually high (>100 kHz) in resonant power converters. Therefore, a high-performance microcontroller (MCU) is required, increasing the cost considerably and rendering it impracticable for LED drivers where simple implementations are desired.

As a conclusion of the previous exposition, the main challenge on current-controlled LED driver conception is the design of a stable control system that is capable of regulating the LED average current (I_{LED}) over a wide dimming range, attenuate LF (< 120 Hz) ΔI_{LED} excited by ΔV_{BUS}, and provide to the driver a transient response with a reduced overshoot to avoid electrical stress in the LED, and a short settling time (< 100 ms), preserving overall a simple implementation simultaneously. However, it is well-known that the PI controller presents both simplicity and a prominent capability in tracking a DC reference, but a limited loop gain at different frequencies diminishes its capacity of rejecting periodic disturbances [28]. On the other hand, APDR controllers have strong robustness against different disturbances and unmodelled dynamics at the expense of being a more complex system [27], [29]. Therefore, combining the advantages of both PI and APDR controllers, this paper proposes a novel hybrid dual-loop controller, namely PI&APDR control, proper for the DC/DC stage of the offline LED drivers where a low ΔI_{LED} and DC regulation is required. The outer loop employing PI controller is responsible for regulating I_{LED} over a wide operating range and for dictating the transient performance of the whole system. The inner loop subsystem employs an APDR controller being strictly responsible for attenuating ΔI_{LED} regardless of ΔV_{BUS} amplitude and frequency. Nevertheless, seeking a solution that presents robustness at the same time that preserves simplicity, the APDR subsystem is simplified as much as possible, making it possible to be implemented with a low-cost MCU.

Finally, as will be demonstrated, the proposed PI&APDR controller overcomes the aforementioned main challenges on the current-controlled LED driver conception. Thus, the PI&APDR controller structure proposal, together with its analysis, detailed design, and experimentation, are the main contributions of this paper, respectively described in the remaining sections of this manuscript.

II. PROPOSED HYBRID CONTROLLER ANALYSIS

Figure 1 shows the LLC resonant converter circuit diagram with a high-level representation of the proposed control system, operating as a downstream DC/DC converter in a two independent stage LED driver. The instantaneous LED current

$i_{LED}(t)$, and bus voltage $v_{BUS}(t)$ are sampled by the MCU and fed into the PI&APDR controller, being the desired I_{LED} defined by the reference $r[k]$. Inside the MCU, control action $u[k]$ throughout the digitally controlled oscillator (DCO) and digital PWM (DPWM) module determine the modulated HB f_{sw}, which signal feeds the HB gate-driver. Besides, in comparison with classical solutions, no additional sensors are necessary to implement the PI&APDR controller because v_{BUS} is usually measured to perform the PFC stage control. Finally, as can be seen in Figure 1, since the focus of this work lies on the control system of the DC/DC stage, the PFC stage is not here implemented, being $v_{BUS}(t)$ emulated by a voltage source. It is important to highlight that the PI&APDR controller does not have the function of controlling v_{BUS}.

Figure 2 shows the PI&APDR controller scheme. The outer loop employing a PI controller is responsible for regulating I_{LED} over a wide operating range and for dictating the whole system's transient performance. Besides, the PI is accountable for ensuring robustness against parametric variations. The inner loop, adopting a simplified adaptive controller, is strictly responsible for attenuating ΔI_{LED} regardless of ΔV_{BUS} amplitude and frequency $f_{\Delta V}$. Differing from the conventional dual-loop, where the outer loop usually sets up the reference for the inner loop, in the proposed PI&APDR, each loop produces a control action aiming to carry out its task. So, two decoupled components made up the LLC converter control action $u[k]$, the PI $u_{PI}[k]$ and the APDR one $u_{ADR}[k]$.

During the offline LED driver operation, the LLC resonant converter shown in Figure 1 is subjected to parametric variations (V_{BUS}, and filter components), periodic bus voltage disturbance which is given by ΔV_{BUS}, and load variation due to the AM dimming. Besides, for an LED driver with universal input voltage, $f_{\Delta V}$ ranges between $100 - 120$ $Hz \pm 10\%$. In this way, considering the internal model principle (IMP)
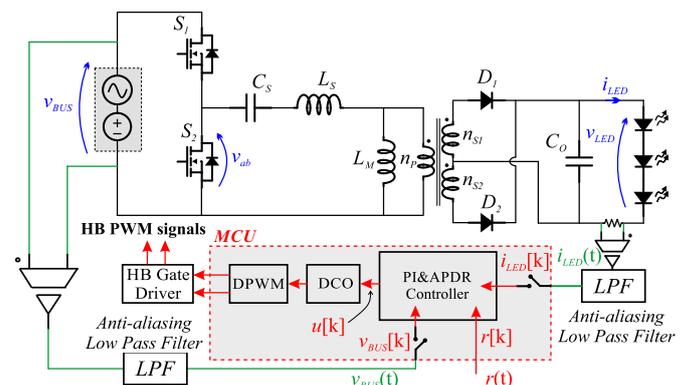
Fig. 1. Circuit diagram of the LLC converter implementing the DC/DC stage of an offline LED driver.
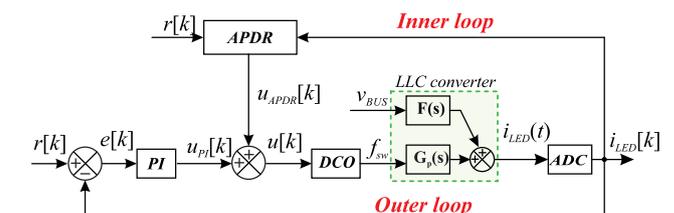
Fig. 2. General overview of the proposed hybrid dual-loop based control scheme for LLC resonant converter.

that establishes that the controller should include a model of the disturbance, it can be stated that the control action $u[k]$ required by the LLC converter to track the output DC reference and reject ΔV_{BUS} as well as reject parametric variations, will present a DC component summed to a periodic signal with the same frequency of the disturbance. Therefore, assuming a sinusoidal periodic disturbance, in steady-state $u[k]$ is given by (1), where T_s is the digital controller sampling period, and A and B are constant values.

$$u[k] = A + B\sin(2\pi f_{\Delta V} kT_S + \phi). \quad (1)$$

Translated into frequency domain analysis of the loop gain $T(s)$, the Bode Diagram for PR, PIR, or IQR compensated loop-gain $T(s)$ presents a high DC gain and a high gain (>30 dB) around $f_{\Delta V}$. Phase and gain margins and the crossover frequency are adjusted to achieve an acceptable dynamic performance. Unfortunately, as it will be shown, one single linear PR, PIR or IQR controller designed to accomplish these guidelines will present a poor performance when the converter is subjected to a wide operating range. The performance is even worse when parametric variations are taking into account. In fact, considering the resonant-based controllers, there is a trade-off between stability margin gains and ΔI_O rejection for $f_{\Delta V}$ variation, where a better ΔI_O rejection results in a smaller phase margin [15] and vice-versa. Besides, it is impossible to overcome this issue in the design step due to the limitations of the small-signal models for the LLC converter considering operation beyond the series resonance [19]. Notwithstanding, it should be noted that the expression given by (1) remains valid. The problem is due to the difficulty of linear controllers to properly generate the signal in (1).

However, employing the proposed PI&APDR controller to generate (1), an enhanced controlled current can be achieved since the DC reference tracking is decoupled from the ripple attenuation action, allowing each loop to be optimized in terms of robustness and performance. Thus, the DC tracking decoupling from periodic disturbance rejection, together with the PI and APDR subsystems analysis and design, is highlighted as the main contribution of this paper.

A. PI Controller Subsystem Analysis and Design Guidelines

Assuming that the inner loop is fully functional in rejecting the sinusoidal ΔV_{BUS}, and assuring that the outer loop crossover frequency is a decade below $f_{\Delta V}$, the inner loop can be omitted during the outer loop analysis and design since it does not affect the DC regulation. Hence, the outer loop is designed following the classical frequency-response method, which is based on the analysis of the compensated loop gain $T(s)$.

The outer loop has to track i_{LED} DC reference in the LLC resonant LED driver, as well as to reject dynamic and parametric variations, and so theoretically achieve zero steady-state error. Therefore, a PI controller will be employed in the outer loop. The PI compensated loop gain can be easily adjusted to present mathematically infinite DC gain and increased phase and gain margins. High gain and phase margins will improve the controller robustness against the converter dynamic and parametric variation. The mentioned dynamic variation can occur due to parametric variations

and also because of the converter wide operating range to supply the LED load with different current levels to perform dimming. Besides, this dynamic variation is also affected by the resonant converter strong non-linearity, highlighting the necessity of a robust system. On the other hand, since the PI is not responsible for compensating the periodic bus voltage disturbance at $f_{\Delta V}$ frequency, no requirements are imposed to the PI compensated loop gain around $f_{\Delta V}$.

Taking into account the IMP and considering the reference and parametric variation as step signals, the outer loop control action will then be a DC signal under steady-state operation, providing the DC term in (1). Besides, to avoid interaction with the inner loop, the PI compensated loop gain has to present a crossover frequency below $f_{\Delta V}$, which demand a low gain at $f_{\Delta V}$. These design guidelines will stamp to the outer loop a dynamic that follows a first-order behavior avoiding electrical stress in the LED load that otherwise could be caused by overshooting. In order to elucidate the outer loop design, further details are presented in next section.

B. APDR Subsystem Analysis and Design Guidelines

Figure 3 shows the detailed block diagram of the proposed PI&APDR controller; further details of the APDR subsystem will be described later in this section.

As aforementioned, the inner loop is strictly responsible for the periodic ΔV_{BUS} disturbance rejection. Assuming a sinusoidal ΔV_{BUS}, it is known from the IMP that a sinusoidal component should appear at the control action to reject this disturbance. Indeed, the inner loop function is intended to generate this sinusoidal component. Nevertheless, since the ΔV_{BUS} can present different frequencies due to the universal input voltage, different amplitude depending on PFC topology and output power, and its rejection also depends on the LLC converter dynamic, a versatile and robust inner loop must be developed. To tackle this task, a robust APDR controller is employed to implement the inner loop.

Therefore, under steady-state operation, the inner loop has to generate a control action given by (2). Alternatively, $u_{APDR}[k]$ in (2) can be rewritten by (3), wherein $V_{\sin}[k] = V_s\sin(2\pi f_{\Delta V} kT_S)$ and $V_{\cos}[k] = V_c\cos(2\pi f_{\Delta V} kT_S)$ are respectively sine and cosine signals with frequency $f_{\Delta V}$, and V_s and V_c amplitudes; and, $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ are constant values under steady-state operation, which will define B and phase ϕ of $u_{APDR}[k]$ in (2). Defining the vectors in (4), the APDR control law can rewritten by (5).

$$u_{APDR}[k] = B\sin(2\pi f_{\Delta V} kT_S + \phi) \quad (2)$$
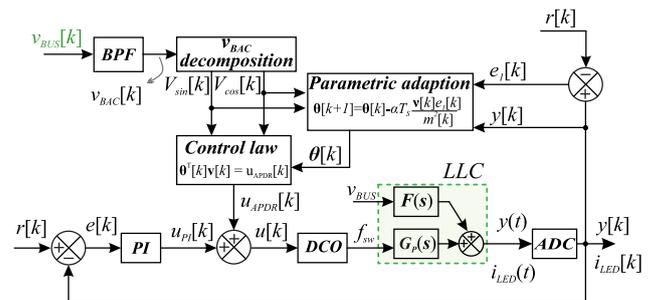
Fig. 3. Proposed hybrid dual-loop PI&APDR controller scheme for LLC resonant converter.

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

317

$$u_{APDR}[k] = \theta_{\sin}[k]V_{\sin}[k] + \theta_{\cos}[k]V_{\cos}[k] \qquad (3)$$

$$\boldsymbol{\theta}^T[k] = \begin{bmatrix} \theta_{\sin}[k] & \theta_{\cos}[k] \end{bmatrix} \qquad (4a)$$

$$\mathbf{v}^T[k] = \begin{bmatrix} V_{\sin}[k] & V_{\cos}[k] \end{bmatrix} \qquad (4b)$$

$$u_{APDR}[k] = \boldsymbol{\theta}^T[k]\mathbf{v}[k]. \qquad (5)$$

Since $u_{APDR}[k]$ and ΔV_{BUS} must have the same $f_{\Delta V}$, and being the frequency of $u_{APDR}[k]$ function of $V_{\sin}[k]$ and $V_{\cos}[k]$, it is reasonable to derive these sine and cosine signals from v_{BUS}. Therefore, as can be seen in Figure 3 the sampled $v_{BUS}[k]$ signal is filtered by a digital band pass filter (BPF) with the aim to extract the sinusoidal fundamental AC component ($v_{BAC}[k]$) from ΔV_{BUS}. Following, $v_{BAC}[k]$ is then defined as $V_{\sin}[k]$, and $V_{\cos}[k]$ is obtained from $V_{\sin}[k]$ differentiation. With $V_{\sin}[k]$ and $V_{\cos}[k]$ known, the required control action $u_{APDR}[k]$ to reject ΔV_{BUS} can be defined by properly determining $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$. Actually, $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ correspond to the automatically adapted parameters of the APDR subsystem.

To determine these adapted parameters, a gradient automatic parameter estimation algorithm is designed due to its simplicity [29], [30], given by (6). Where α is a design constant, that dictates the automatic parameters adaptation speed; $e_1[k] = y[k] - r[k]$ is the APDR tracking error, wherein $y[k]$ is the measured LED current $i_{LED}[k]$, and $r[k]$ the I_{LED} reference; and, $m^2[k]$ is a function used to add robustness to the APDR controller. The function $m^2[k]$ is expressed by (7), whose outcome is always ≥ 1. The main purpose of $m^2[k]$ is to stop the sharp variation of $\boldsymbol{\theta}$ due to abrupt changes in $u_{APDR}[k]$, $y[k]$, or $\mathbf{v}[k]$, thus adding robustness to the APDR subsystem [29], [30].

$$\boldsymbol{\theta}[k+1] = \boldsymbol{\theta}[k] - \frac{\alpha T_s e_1[k]}{m^2[k]}\mathbf{v}[k] \qquad (6)$$

$$m^2[k] = 1 + u_{APDR}^2[k] + y^2[k] + \mathbf{v}^T[k]\mathbf{v}[k]. \qquad (7)$$

Now, with $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ also defined, the control action $u_{APDR}[k]$ is easily determined by computing (5).

The inner loop design corresponds precisely to the definition of α constant, highlighting its simple design. The BPF parameters, and the v_{BAC} decomposition algorithm, are the same regardless of the switched converter topology used in the PFC stage. Besides, it can be noticed that the proposed controller presents a simple structure when compared to reported APDR controllers since only two parameters are adapted ($\theta_{\sin}, \theta_{\cos}$), and no parameters estimator is required, thus making it possible the use of low-cost MCUs and highlighting its simple implementation feature.

III. PI&APDR DESIGN EXAMPLE

Table I shows the LLC LED driver parameters. To design the resonant tank elements, the procedure detailed in [31] has been employed. Analyzing Table I, it can be noticed that the converter is designed to operate with a variable V_{BUS} ranging between 360 V and 420 V, and a variable output

TABLE I
LLC Resonant LED Driver Parameters

Parameter	Designator	Value
LLC LED driver design specification		
Nominal DC input voltage	V_{BUS}	400 V
Minimum DC input voltage	$V_{BUS.MIN}$	360 V
Maximum DC input voltage	$V_{BUS.MAX}$	420 V
Bus voltage ripple frequency	$f_{\Delta V}$	$100 - 120$ Hz
LLC series resonant frequency	f_o	100 kHz
LLC converter output power	P_O	$15 - 100$ W
ADC sampling period	T_s	25 μs
Designed LLC LED driver resonant converter		
Average LED current range	I_{LED}	$0.2 - 1.15$ A
Average LED voltage	V_{LED}	$80.4 - 87.3$ V
Resonant capacitor	C_S	12 nF
Resonant inductor	L_S	211 μH
Magnetizing inductance	L_M	633 μH
Output capacitor (Film capacitor)	C_O	10 μF/100V
Transformer turns ratio (n)	N_P/N_S	2.29
Half-bridge power MOSFETs	S_1-S_2	STD10NM60N
Output rectifier diodes	D_1-D_2	SB3200TA

current to perform dimming at least between 100% and 20%, which corresponds to the reference dimming range for outdoor applications established in [32]. Regarding the LED module, three BXRC-50C4000-F-04 devices are connected in series [33]. The LED module piece-wise-linear equivalent circuit [34] presents a series resistance of $r_d = 6.28$ Ω and a threshold voltage of $V_{th} = 80$ V.

A. PI Subsystem Design

As aforementioned, the PI subsystem design is based on the frequency-response method. Therefore, it is necessary to define the transfer function (TF) that relates the converter output (i_{LED}) with their control action (f_{sw}), denoted as $G_P(s)$. Furthermore, as can be seen in Figure 1, to avoid the aliasing effect on the digital system, as well as to protect the MCU ADC module, the measured i_{LED} is filtered by a low pass filter (LPF), whose TF is defined as $H_i(s)$. So, to consider the LPF dynamics during PI design, the uncompensated loop gain $T(s)$ will be given by $G_P(s)H_i(s)$.

As a practical rule, the ADC sampling frequency $f_s = 1/T_s$ is usually selected to be 10 times faster than the highest crossover frequency of interest, and the LPF bandwidth is commonly designed to be lower than $1/2$ of the f_s. Thus, $f_s = 40$ kHz is selected in order to be able to assess different controllers with a cut-off frequency lower than 4 kHz while keeping the same experimental setup. In this way, the LPF is implemented through the Sallen Key topology, with a cut-off frequency of 15 kHz, a quality factor of 0.5, and a damping ratio equal to 1, yielding in (8).

$$H_i(s) = \frac{1 \cdot 10^{10}}{(s + 1 \cdot 10^5)^2}. \qquad (8)$$

Given the parameters in Table I and considering the nominal operating conditions, the modeling procedure presented in [14] has been employed to obtain $G_P(s)$. Now, taking into account $H_i(s)$ and the $G_P(s)$, and neglecting the high-frequency right half-plane zero, and poles and zeros higher than the f_{sw}, a nominal sixth-order system is obtained for $T(s) = G_P(s)H_i(s)$, given by (9).

$$T(s) = \frac{-2.2591 \cdot 10^{21}}{(s^2 + 1.594 \cdot 10^4 s + 9.973 \cdot 10^8)}$$

$$\frac{1}{(s^2 + 1.346 \cdot 10^5 s + 2.453 \cdot 10^{11})} \frac{10^{10}}{(s + 10^5)^2}. \quad (9)$$

Even though the controller will be digitally implemented, the design of the PI controller is performed employing the well-established frequency-response method. However, since frequency-response methods do not apply to the z plane, the w transformation is employed, which transforms a TF in the z plane into that in the w plane [35]. Afterwards, conventional frequency-response techniques can be used in the w plane. Therefore, based on the procedure presented in [35] (pg. 234) , firstly $T(s)$ is discretized with a zero-order hold (ZOH) considering f_s. In the next step, to model the transportation time and obtain a strictly proper TF for the controller, the unit delay (z^{-1}) is added to the TF in the z plane $(T(z))$. Subsequently, using the bilinear transformation, $T(z)$ is converted into a rational function in the w plane, yielding the uncompensated loop gain $T(w)$. In this procedure, the ADC gains are neglected, being their effect compensated in the implementation. At this point, working in the w plane, the PI regulator is finally designed employing the frequency-response technique. With the pole in origin, the gain and zero position are adjusted to obtain: i) a 10 Hz crossover frequency, which is a decade below the minimum value of $f_{\Delta V}$; and, ii) High gain and phase margins, respectively, 44.7 dB and 89.6 deg. With these parameters, a first-order behavior is achieved with a settling time of around 60 ms, which is considered adequate for this particular application. The PI in w domain is given by

$$PI(w) = -\frac{0.00024(w + 28320)}{w}. \quad (10)$$

For the sake of comparison, an IQR controller is also designed. The integrator provides ideally an infinite DC gain to track DC reference and reject parametric variations, while the quasi-resonant response is tuned to provide a high gain ($>$ 30 dB) around $f_{\Delta V}$ in order to attenuate ΔI_{LED}. However, due to IQR inherent trade-off, the designed compensator provides a 9.79 dB gain margin, 59.8 deg. phase margin at 753 Hz, 12% overshoot and 5 ms settling time. The IQR TF is given by

$$IQR(w) = \frac{-500(w^2 + 816.8w + 667200)}{w(w^2 + 1.382w + 477700)}. \quad (11)$$

To implement (10) and (11) in the MCU, both equations are first discretized employing the bilinear method. Then, z^{-1} considered under design to obtain a strictly proper controller, is added to the discretized form of (10) and (11). If one step delay is not enough to perform all required calculations, the controller must be redesigned, considering further step delays. In the sequence, applying inverse Z transformation the difference equation for each controller is obtained.

It is worth mentioning that the PI&APDR is compared with its main counterpart considering the same application, which corresponds to the classical resonant-based controller; here,

the IQR is selected. Advanced state-of-the-art controllers, for instance, MRAC, among others, are not practical solutions for LED drivers due to their complexity and high implementation cost. Thus, further comparisons will be omitted.

B. Adaptive Periodic Disturbance Rejection Design

In order to extract the AC component from $v_{BUS}(t)$, its sampled signal $v_{BUS}[k]$ is filtered by a digital BPF. Considering a PFC stage with the universal input voltage, the $f_{\Delta V}$ ranges between $100 - 120\ Hz$. Thus, dealing with the BPF design, initially, a second-order BPF is defined in the continuous domain, given by (12). Wherein, $f_o = 2\pi\omega_o$ is the center frequency; BW is the filter bandwidth in rad/s; and H_o is the circuit gain.

$$BPF(s) = \frac{H_o \cdot BW \cdot s}{s^2 + BW \cdot s + \omega_o^2}. \quad (12)$$

The BPF design is accomplished by defining $f_o = 110\ Hz$, whose value is at the center of the $f_{\Delta V}$; and, $BW = 2\pi 60\ rad/s$ and $H_o = 1.1$ are so determined in order to avoid attenuation of the filtered AC component of the bus voltage ripple within $100 - 120\ Hz$. Following, $BPF(s)$ is discretized using bilinear transformation with $T_s = 25\ \mu s$. Then, with inverse Z transformation, the BPF recursive form $v_{BAC}[k]$ is obtained. Manipulating $v_{BAC}[k]$, the determination of $V_{\sin}[k]$ and $V_{\cos}[k]$ is given by (13) and (14), respectively.

$$V_{\sin}[k] = v_{BAC}[k] \quad (13)$$

$$V_{\cos}[k] = \frac{v_{BAC}[k] - v_{BAC}[k-1]}{4\pi T_s f_{\Delta V}}. \quad (14)$$

The main purpose of measuring $v_{BUS}(t)$ is to obtain the fundamental frequency of the periodic disturbance, being the amplitude and phase of u_{APDR} defined by $\theta_{\sin}$ and $\theta_{\cos}$. For instance, if the gain H_o changes, the obtained values for $V_{\sin}[k]$ and $V_{\cos}[k]$ will also change, thus $\theta_{\sin}$ and $\theta_{\cos}$ will converge to a different value in order to compute the correct amplitude and phase for u_{APDR}.

At this point, $V_{\sin}[k]$ and $V_{\cos}[k]$ are known. To define the automatic adapted parameters $\theta_{\sin}[k]$ and $\theta_{\cos}[k]$ the algorithm given in (6) is rewritten in (15) for the sake of readability.

$$\theta_{sin}[k+1] = \theta_{sin}[k] - \frac{\alpha T_s e_1[k] V_{sin}[k]}{m^2[k]} \quad (15a)$$

$$\theta_{cos}[k+1] = \theta_{cos}[k] - \frac{\alpha T_s e_1[k] V_{cos}[k]}{m^2[k]}. \quad (15b)$$

Analyzing (15) it is noticed that α is the only undefined parameter. Actually, α is the unique parameter of the APDR subsystem whose definition depends on the application and control-loop performance specifications. Thus, to develop a design procedure for α, the APDR subsystem is analyzed from the stability point of view. In this way, Appendix A presents an alternative way to determine e_1, whose definition is essential to analyze the APDR stability in Appendix B. Finally, from the APDR subsystem stability analysis, the constraints to define α are obtained as follows: i) the sign of α have to be equal to the

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

319

sign of the plant high frequency gain, i.e., $sign(\alpha) = sign(k_p)$; ii) the absolute value of α rad/s must be very small in comparison to the plant bandwidth BW_p rad/s.

In this way, analyzing $T(s)$ in (9), a negative sign for k_p is noticed. Besides, assuming that $|T(s)| \approx |T(w)|$, a bandwidth around $BW_p \approx 44$ k rad/s is computed from (9). However, before defining $|\alpha| << BW_p$, it should be carried in mind that the LLC is strongly non-linear, and the converter is subjected to a wide operating range. Thus, to obtain a conservative design, $|\alpha| \leq BW_p/100$ should be employed.

On the other hand, during the transient response of the whole control system, it is expected that the dynamic behavior follows the PI response. In this way, assessing (15), it can be seen that as greater α greater will be the variation of θ during the transient response when e_1 differs from zero. Consequently, greater will be u_{APDR} during this transition, impacting the whole system response. In other words, the greater α the greater the deviation of the system transient behavior from the expected one dictated by the PI is. To elucidate this scenario, Figure 4 shows simulation results of the LED current response under a reference step for different values of $|\alpha|$. In this simulation, the LLC parameters given in Table I are employed, and ΔV_{BUS} is set to zero. Then, employing the proposed PI&APDR controller, the response is obtained for different values of $|\alpha|$. The response labeled as PI (gray trace) employs the single PI, being $u_{APDR} = 0$. As can be seen, the higher $|\alpha|$ more the transient response diverges from PI ones. In addition, also employing simulation results, Figure 5 shows the LED current waveform during the transition from the use of the single PI to PI&APDR controller for different values of $|\alpha|$. As shown, for $|\alpha| = 1000$ the system is unstable. On the other hand, if $|\alpha| = 1$, it can be
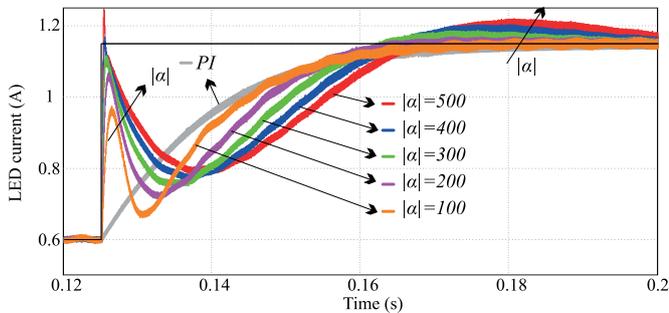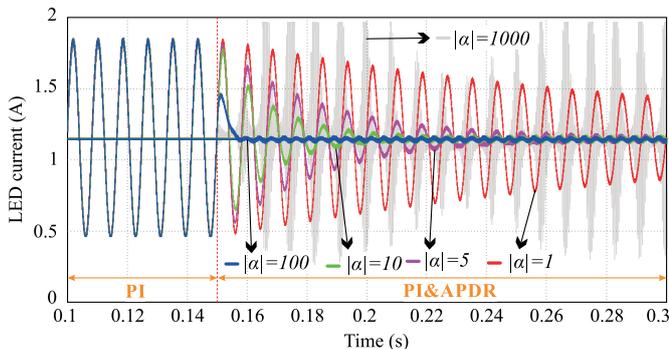
seen that the current ripple is going to be rejected, but with a prolonged transition.

Gathering these results, the following procedure is proposed for α design: i) $sign(\alpha) = sign(k_p)$; ii) Restrain the value of α taking into account $|\alpha| \leq BW_p/100$; iii) in order to optimize the design, the transient behavior of the system under load step should be analyzed for different values of α, while satisfying (ii). Following this methodology, it culminates in selecting $\alpha = -250$ for the presented LLC resonant LED driver. It is worth mentioning that refining the adjustment of design parameters based on experimental and/or simulation results is usual in adaptive controllers. Nevertheless, it must be noted that only one parameter is analyzed, which simplifies this optimization.

IV. EXPERIMENTAL RESULTS

Experimental results are presented in this section to evaluate the performance of the proposed PI&APDR control system for the LLC resonant converter supplying an LED load over a wide amplitude dimming range. Table I presents the employed components to build up the digitally controlled LLC LED driver shown in Figure 1. To realize the digital control system, a TM4C1294NCPDT MCU from Texas Instruments has been employed, which contains a 120 MHz clock and 12 bits ADC converter [36]. Figure 6 shows the laboratory prototype.

Since the focus of this study lies on the control system of the DC/DC stage, the PFC is not implemented, and the v_{BUS} is provided by a controllable voltage source (Keysight 6812B). Nevertheless, in order to emulate the real conditions established by the PFC stage, it is taken into account the ΔV_{BUS} variation as a function of the output power (P_O), $f_{\Delta V}$, average bus voltage (V_{BUS}), C_{BUS} and converter efficiency (η), as given by (16). The C_{BUS} is assumed to be 25 μF and $\eta = 90\%$.

$$\Delta V_{BUS} = \frac{P_O}{\pi f_{\Delta V} V_{BUS} C_{BUS} \eta}. \quad (16)$$

Fig. 4. LED current transient behavior under reference step for different values of α.

Fig. 5. LED current i_{LED} waveform during the transition from single PI to PI&APDR controller for different values of α.
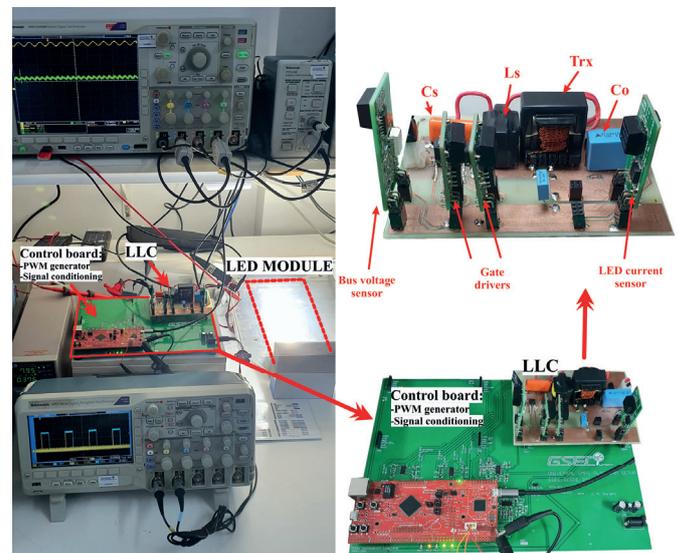
Fig. 6. Photography of the laboratory prototype.
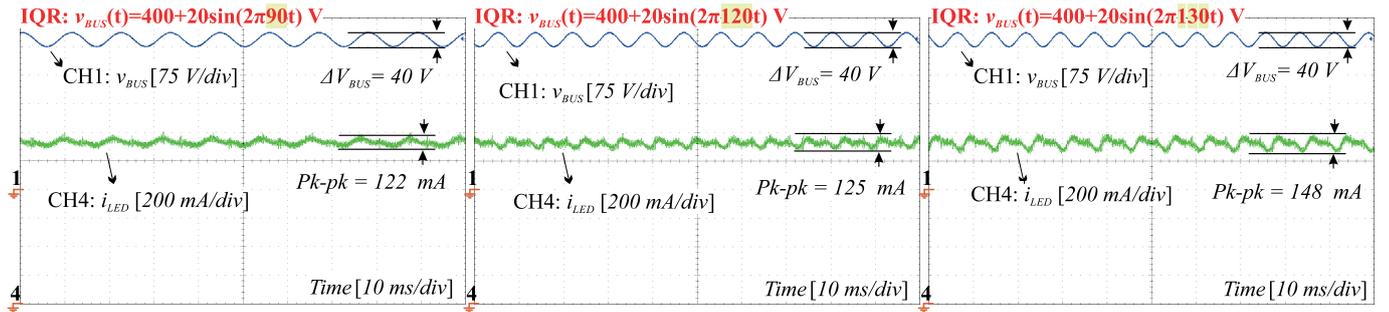
Fig. 7. Steady-state v_{BUS} and i_{LED} of the LLC LED driver at nominal LED current employing the IQR controller under different values of $f_{\Delta V}$.
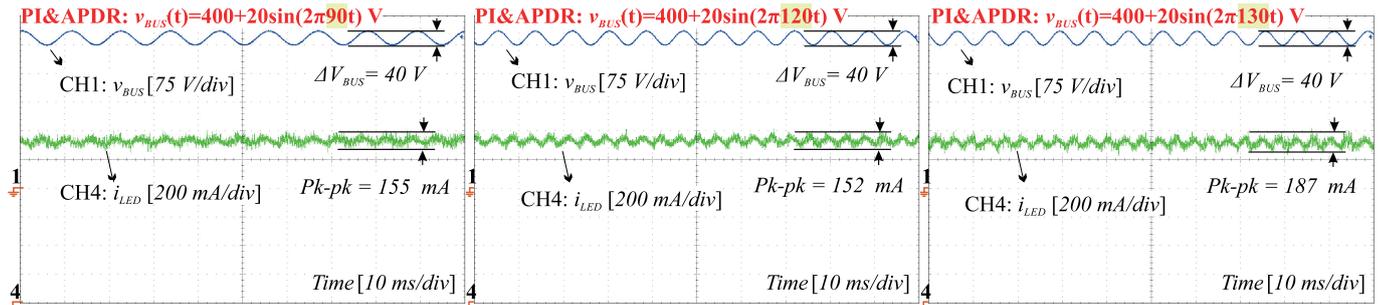
Fig. 8. Steady-state v_{BUS} and i_{LED} of the LLC LED driver at nominal LED current employing the PI&APDR controller under different values of $f_{\Delta V}$.

A. Steady-State Operation of the Closed-Loop LLC LED Driver

Figure 7 shows v_{BUS} and i_{LED} measurement for LLC LED driver operating with the IQR controller at the nominal LED current for different values of $f_{\Delta V}$. Figure 8 shows the same measurement when the proposed PI&APDR controller is employed. As can be seen in these results, the DC reference is tracked, and regardless the $f_{\Delta V}$, a reduced peak-to-peak current ripple is measured even with a high ΔV_{BUS}. In order to compare the computational effort, the time required to execute each control law is measured during steady-state operation. The proposed PI&APDR controller needs 7.52 μs to finish all their calculations, which is similar to the value of 6.56 μs required by IQR. Therefore, it can be inferred that the proposed controller implementation is as simple as conventional controllers. On the other hand, analyzing the experimental measurements, no impact of the controller over the efficiency curve is noticed. Thus, further results comparing the efficiency curve are omitted.

In order to better compare the action of IQR and PI&APDR,
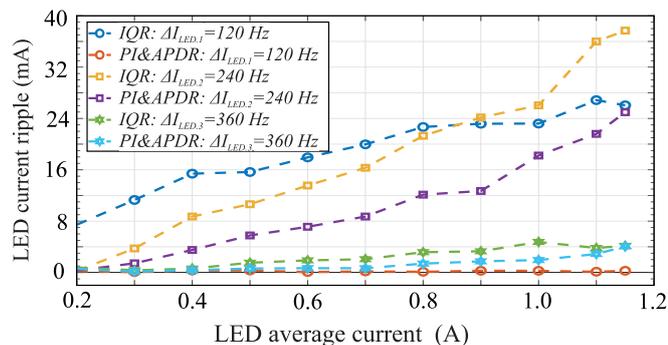
Fig. 9. ΔI_{LED} for the first three harmonics when $f_{\Delta V} = 120\ Hz$.

the first three harmonics of ΔI_{LED} in Figure 8 and Figure 7 have been calculated using FFT, as shown in Figure 9 for $f_{\Delta V}$ = 120 Hz. Analyzing the fundamental harmonic of the LED current ripple $\Delta I_{LED.1}$, it can be noticed a superior performance of the PI&APDR in reducing this ripple component in comparison to IQR controller over the whole output current range. Regarding the second harmonic $\Delta I_{LED.2}$ at 240 Hz, it can be seen that this harmonic correspond to the main component when PI&APDR is employed. However, its amplitude is lower than IQR ones. For the third harmonic, both PI&APDR and IQR present a similar amplitude over the whole dimming range. Nevertheless, in order to obtain a better insight of the ΔI_{LED} reduction, the LED driver flicker in comparison to the IEEE Std 1789-2015 [3] limits is analyzed in next subsection.

B. LED Driver Flicker Assessment

To evaluate the level of flicker for an output light that presents several harmonics, the IEEE Std. 1789-2015 recommends the computation of the normalized modulation (NM) [3], where a value of $NM < 1$ is an acceptable level of flicker. Basically, the NM corresponds to the weighted sum of the light output different harmonics below 1250 Hz. Assuming that the LED operates in its linear region, where the output light is directly proportional to i_{LED}, the NM can be estimated from the FFT decomposition of the measured i_{LED}. In this way, the NM is estimated by (17), wherein I_{LED} is the LED average current, N is the number of harmonic components below 1250 Hz, and $\tilde{i}_m$ is the weighted LED current Fourier amplitude coefficient ($|i_m|$) corresponding to frequency f_m, which is given by (18).

$$NM = \sum_{m=1}^{N} \left(\frac{\tilde{i}_m}{I_{LED}} \right) \tag{17}$$

$$\tilde{i}_m = \begin{cases} \dfrac{4000|i_m|}{f_m} & \text{if } f_m < 90 \text{ } Hz, \\ \dfrac{1250|i_m|}{f_m} & \text{if } 90 \text{ } Hz \leq f_m \leq 1250 \text{ } Hz. \end{cases} \tag{18}$$

Figure 10 shows the computed *NM* levels for the cases where the IQR and PI&APDR controllers are employed. These results consider the LLC resonant LED driver operating with nominal and minimal output current and different $f_{\Delta V}$, covering the range of a front-end PFC with the universal input voltage, where the frequency can change around $50/60 \text{ } Hz$. Under this analysis, ΔV_{BUS} is adjusted for each test as defined by (16). As can be seen in Figure 10, both IQR and PI&APDR controllers yield in $NM < 1$. However, it should be noticed that the IQR presents a deteriorated performance when $f_{\Delta V}$ is away from the IQR resonance ($110 \text{ } Hz$), which outcome in a reduced robustness against ripple current rejection for $f_{\Delta V}$ variation. So, since low-frequency ripple ($< 1250 \text{ } Hz$) is strongly attenuated when employing PI&APDR, it would be possible to employ even lower C_{BUS}, enhancing the LED driver power density, as well as increasing its operational range, which highlights the proposed controller improved performance in comparison to IQR.

C. Step Signal Perturbations

Figure 11 shows the measured waveform of v_{BUS} and i_{LED} for LLC LED driver operating with IQR or PI&APDR controller under a DC step in V_{BUS} for $f_{\Delta V} = 120 \text{ } Hz$. On the other hand, Figure 12 shows the transient performance of the LLC LED driver employing IQR and proposed PI&APDR controller when subjected to step in the reference ($\approx 50\%$ to 100%). Analyzing Figure 11 and Figure 12, it can be seen that after a transient period i_{LED} reaches its reference value for both controllers. However, the PI&APDR presents a dynamic that is dictated by the PI loop, which follows the first-order behavior avoiding electrical stress in the LED load caused by overshooting. For LED drivers, a smooth transient behavior is preferred to a fast dynamic system with overshoot. To avoid overshoot when IQR is employed, it is necessary to reduce its crossover frequency, which on the other hand, reduces the controller gain around $f_{\Delta V}$ and impairs the ΔI_{LED} attenuation. This trade-off between dynamic performance and ΔI_{LED} reduction capacity noticed in IQR design does not occur

Fig. 11. LLC LED driver transient response for an input voltage step up: with conventional IQR (upper trace) and proposed PI&APDR (lower trace) controllers.
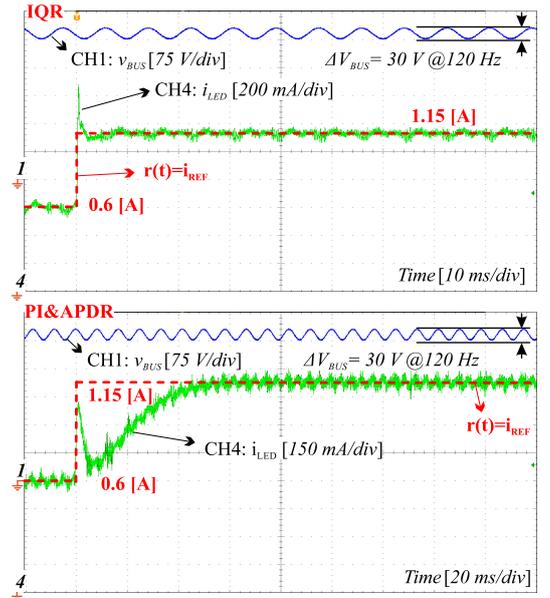
Fig. 12. LLC LED driver transient response when reference changes: with conventional IQR (upper trace) and proposed PI&APDR (lower trace) controllers.

when the proposed PI&APDR controller is employed.

D. Reference Tracking Evaluation

In order to further evaluate the capability of each controller to track I_{LED} reference and reduce ΔI_{LED}, Figure 13 shows the measurement of v_{BUS} and i_{LED} when the IQR or PI&APDR controller is employed considering the same dimming profile. For both controllers i_{LED} tracks the reference, differing in the transient performance and peak-to-peak reduction. As expected, the PI&APDR controller presents a dynamic which is dictated by the PI loop. Regarding ΔI_{LED} reduction, it can be noticed a deteriorated performance for the IQR controller when it goes to deeper dimming levels and when $f_{\Delta V}$ diverges

Fig. 10. NM for the LLC LED driver operating with IQR and PI&APDR controllers under different ΔV_{BUS} frequencies $f_{\Delta V}$.
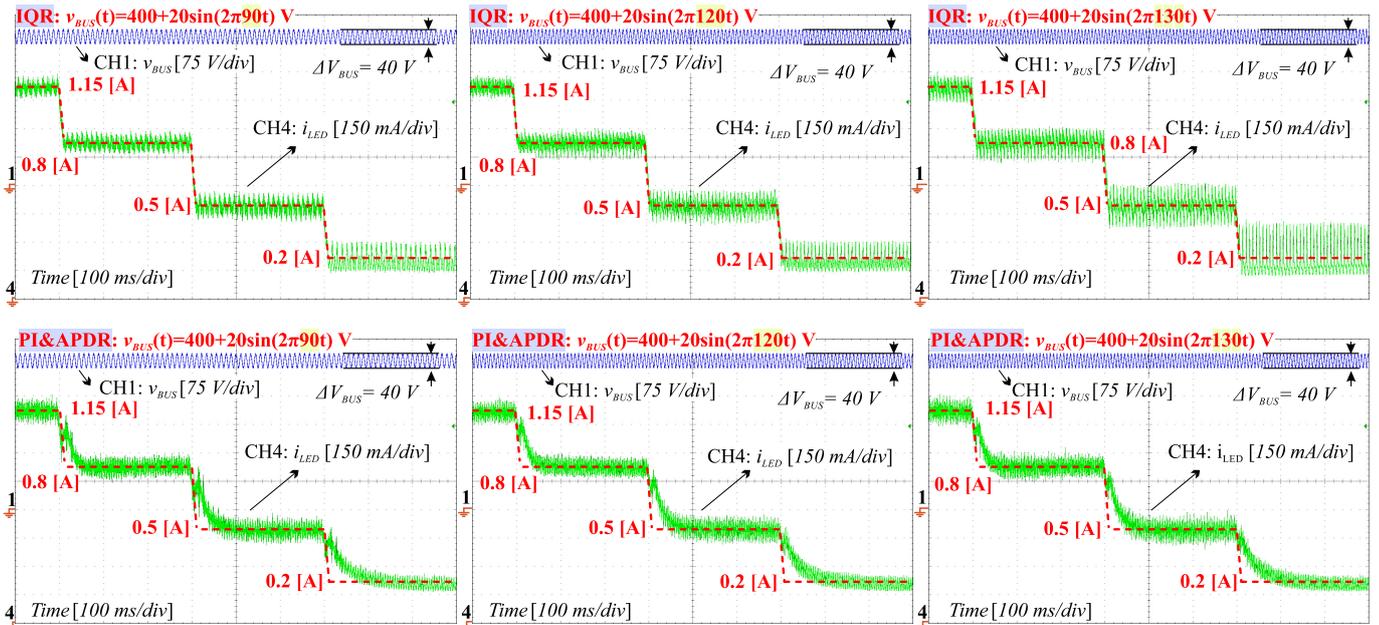
Fig. 13. LLC LED driver v_{BUS} and i_{LED} waveforms during dimming profile; Upper traces: Operating with IQR controller; Lower traces: Operating with PI&APDR controller.

from resonant frequency of IQR, which is also expected and explained by the changing of converter dynamic behavior.

E. Controllers Robustness Analysis

This final assessment investigates the robustness of each controller. Therefore, considering a hypothetical scenario, the filter components are reduced in 10%, L_M is increased in 10%, transformer turn ratio is reduced in 5%, and LED module threshold voltage is reduced in 10%, emulating the worst case where the frequency range is shifted to higher values. Under this condition, the LLC LED driver operating with the IQR controller becomes unstable when it goes to deeper dimming levels. In order to elucidate this outcome, the compensated loop gain is obtained from an AC-sweep analysis employing simulation results, as shown in Figure 14. As can be seen,

the IQR compensated loop is shown for an output reference of 1.15 A, 0.8 A, and 0.4 A, where the phase margin reduction is evident as I_{LED} is diminished, reaching almost 0 deg. for 0.4 A. For $I_{LED} < 0.4$ the system becomes unstable when IQR is employed. On the other hand, analyzing the PI&APDR compensated $T(s)$, for $I_{LED} = 0.4$ A and $I_{LED} = 1.15$ A the phase margin is around 90 deg. with gain margins greater than 40 dB, being so stable. However, a gain crossover frequency

Fig. 14. Simulation results of the compensated loop gain analysis for LLC LED driver with parametric variations: $L_M = 700$ μH, $n = 2.17$, $L_S = 190$ μH, $C_S = 10.9$ nF.
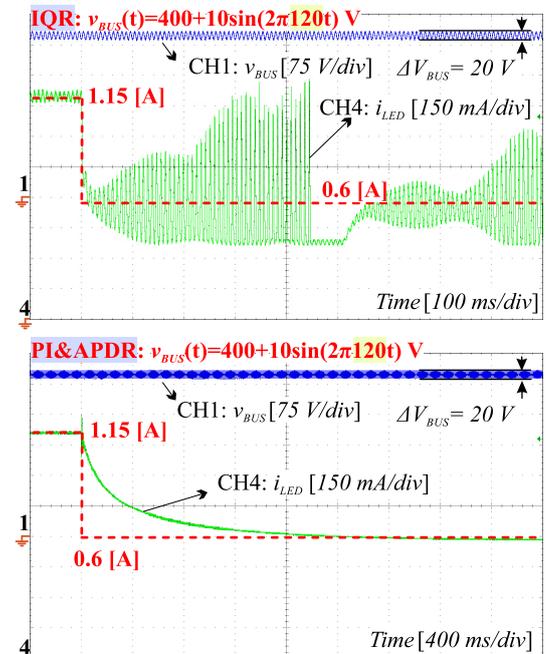
Fig. 15. Transient response under reference step for the LLC LED driver with parametric variations $L_M = 683$ μH, $n = 2.17$, $L_S = 190$ μH, $C_S = 10$ nF, and one LED device short-circuited: Upper trace:Employing IQR controller; Lower trace: Employing proposed PI&APDR controller.

reduction is evident, which increases the system settling time.

With similar parametric changes, except by the LED threshold voltage, Figure 15 shows the experimental measurement of v_{BUS} and i_{LED} during the reference step-down condition, where one of the three LED devices is short-circuited ($V_{LED} \approx 58\ V$). As can be seen, even with the parametric variation and bus voltage periodic disturbance the LED current is stable and regulated at reference when the proposed PI&APDR controller is employed. On the other hand, when IQR is employed, the system becomes unstable when the reference changes.

This final assessment reinforces the enhanced performance of the proposed PI&APDR controller compared to resonant-based controllers. In a general way, employing the PI&APDR, outstanding performance is demonstrated, where the system becomes robust against parametric variations and robust against different bus voltage ripple frequencies and amplitude.

V. CONCLUSION

This paper has presented the conception, analysis, design, and experimentation of a new hybrid dual-loop control system, based on PI and APDR controllers, named PI&APDR controller. Although the results are only presented for the LLC resonant converter, the PI&APDR controller can be efficiently designed to regulate the LED current for the cases where other DC/DC converters are employed. The proposed controller is suited for applications where a low output current ripple is required simultaneously with a DC regulation over a wide operation range.

Experimental results and simulation analysis show the outstanding performance of the proposed controller in comparison to conventional counterpart resonant-based controllers. Employing the PI&APDR controller the LED current DC reference is tracked over a wide operating range, even under parametric variations such as average bus voltage, resonant tank elements, and LED module. Besides, enhanced performance is achieved in reducing the output current ripple raised from the bus voltage ripple, where different bus voltage ripple frequencies are also considered. The maximum *NM* is given by 0.11 and 0.58, respectively for the proposed PI&APDR and conventional IQR controller. Both controllers are in accordance with IEEE Std. 1789-2015, which limits the NM < 1. In a general way, conventional resonant-based controllers present deteriorated dynamic performance, higher LED ripple current, and even instabilities when subjected to these same conditions.

Finally, it is essential to mention that the proposed controller, even employing non-linear adaptive controllers, preserves the feature of having a simple design and implementation. Besides, knowing that adaptive controllers naturally require more computational resources, it is important to highlight that the computational effort of the proposed PI&APDR controller is quite similar to the conventional resonant-based controller's, allowing the designer to use conventional microcontrollers. As a suggestion, future studies should analyze the hybridization of the APDR subsystem with different linear controllers, such as PID, allowing the converter to obtain a faster dynamic response with high gain and phase margins, thus ensuring strong robustness.

APPENDIX A

Tracking error definition

For the sake of simplicity, both PI and APDR subsystems are considered decoupled. Thus, since the APDR is strictly responsible for rejecting the bus voltage periodic disturbance d, and assuming that PI is fully functional in regulating the DC value at $r = 0$, the system can be represented as shown in Figure 16. So, the output y can be defined by

$$y = y_1 + y_2 = G_p(s)u_{APDR} + F(s)d. \qquad (19)$$

The periodic sinusoidal disturbance d can be defined by a linear combination of V_{sin} and V_{cos}, with weighting parameters $\bar{\theta}^*_{sin}$ and $\bar{\theta}^*_{cos}$, as given by

$$d = -\bar{\theta}^*_{sin}V_{sin} - \bar{\theta}^*_{cos}V_{cos} = -\bar{\boldsymbol{\theta}}^{*T}\mathbf{v} \qquad (20)$$

where $\bar{\boldsymbol{\theta}}^* = \left[\bar{\theta}^*_{sin}; \bar{\theta}^*_{cos}\right]^T$.

Following (5), in continuous time, the APDR subsystem control action is given by

$$u_{APDR} = \boldsymbol{\theta}^T \mathbf{v}. \qquad (21)$$

With $r = 0$, the APDR tracking error $e_1 = y - r$, is reduced to $e_1 = y$. Hence, substituting (21) and (20) into (19), yields

$$e_1 = G_p(s)\boldsymbol{\theta}^T \mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v}. \qquad (22)$$

Inspecting (22), it is noticed that e_1 depends of $\boldsymbol{\theta}$ and $\bar{\boldsymbol{\theta}}^*$. Where $\boldsymbol{\theta}$ origin is in the APDR control action, and $\bar{\boldsymbol{\theta}}^*$ is related to the periodic disturbance d. From the APDR subsystem point of view, it is assumed that there is a correct solution called $\boldsymbol{\theta}^*$ for the adapted $\boldsymbol{\theta}$ that reject the disturbance d and brings e_1 to zero. Thus, the parametric adaption error ($\tilde{\boldsymbol{\theta}}$) is defined by

$$\tilde{\boldsymbol{\theta}} = \boldsymbol{\theta} - \boldsymbol{\theta}^*. \qquad (23)$$

Now, substituting the identity $\boldsymbol{\theta} = \tilde{\boldsymbol{\theta}} + \boldsymbol{\theta}^*$ in (22) yields in

$$e_1 = G_p(s)\tilde{\boldsymbol{\theta}}^T \mathbf{v} + G_p(s)\boldsymbol{\theta}^{*T}\mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v}. \qquad (24)$$

Defining $p = G_p(s)\boldsymbol{\theta}^{*T}\mathbf{v} - F(s)\bar{\boldsymbol{\theta}}^{*T}\mathbf{v}$, (24) is rewritten as

$$e_1 = G_p(s)\tilde{\boldsymbol{\theta}}^T \mathbf{v} + p. \qquad (25)$$
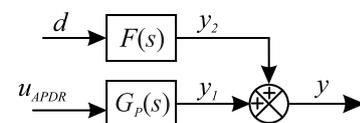
Fig. 16. Simplified block diagram of the LLC resonant LED driver employing PI&APDR controller.

324

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

The signal p is bounded once $\mathbf{v}$ is finite and $G_p(s)$ and $F(s)$ represent stable systems. Besides, since there is a solution for $\bar{\boldsymbol{\theta}}^*$ and $\boldsymbol{\theta}^*$, which means that these parameters are constant, the signal p tends to zero in steady-state. Furthermore, the dynamic variation of p is defined by $G_p(s)$ and $F(s)$.

APPENDIX B

Analysis of the APDR subsystem stability

Consider the LLC resonant converter as an LTI system, whose TF is

$$G_p(s) = k_p \frac{Z_p(s)}{R_p(s)} = k_p \frac{s^n + a_{n-1}s^{(n-1)} + ... + a_1 s + a_0}{s^n + b_{n-1}s^{(n-1)} + ... + b_1 s + b_0} \quad (26)$$

Where Z_p is a monic Hurwitz polynomial, R_p is a monic polynomial, and k_p is the high-frequency gain with known sign.

In continuous time, the APDR control action is given by (27), and the parametric adaptive law is defined by (28).

$$u_{APDR} = \boldsymbol{\theta}^T \boldsymbol{v} \quad (27)$$

$$\dot{\boldsymbol{\theta}} = -\frac{\alpha \mathbf{v} e_1}{m^2}. \quad (28)$$

Employing Lyapunov's second method, the adopted defined positive V scalar function is given by

$$V = \frac{1}{2}\tilde{\boldsymbol{\theta}}^T \tilde{\boldsymbol{\theta}}. \quad (29)$$

Now, if it is proved that the gradient of V is negative, it means that $\tilde{\boldsymbol{\theta}}$ tends to zero. Consequently, the tracking error also tends to zero, and the APDR subsystem will be stable. The derivative of (29) with respect to t yields

$$\dot{V} = \frac{1}{2}\dot{\tilde{\boldsymbol{\theta}}}^T \tilde{\boldsymbol{\theta}} + \frac{1}{2}\tilde{\boldsymbol{\theta}}^T \dot{\tilde{\boldsymbol{\theta}}} = \tilde{\boldsymbol{\theta}}^T \dot{\tilde{\boldsymbol{\theta}}}. \quad (30)$$

From (23), the time derivative of parametric adaption error gives $\dot{\tilde{\boldsymbol{\theta}}} = \dot{\boldsymbol{\theta}}$. Now, considering e_1 defined by (25), defining $\delta = d/dt$ as the differential operator, and taking into account (28), $\dot{\tilde{\boldsymbol{\theta}}}$ can be rewritten as (31). Substituting (31) in (30) yields (32). To avoid the use of time and frequency domain in the same equations, the differential operator δ is defined. So, $G_p(s)$ and $G_p(\delta)$ are equivalent.

$$\dot{\tilde{\boldsymbol{\theta}}} = \dot{\boldsymbol{\theta}} = -\alpha \frac{\mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T \mathbf{v} + p\right)}{m^2} \quad (31)$$

$$\dot{V} = -\alpha \frac{\tilde{\boldsymbol{\theta}}^T \mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T \mathbf{v}\right)}{m^2} - \alpha \frac{\tilde{\boldsymbol{\theta}}^T \mathbf{v} p}{m^2}. \quad (32)$$

At this point, the sign (32) has to be carefully analyzed in order to assess system stability. Because p tends to zero in steady-state with the dynamic of $G_p(\delta)$ and $F(\delta)$, which means, much faster than the variation of $\tilde{\boldsymbol{\theta}}$, only the first

term in the right side of (32) is analyzed under stability point of view. Therefore, to ensure a negative gradient, the sign of α ($sign(\alpha)$) must have the same sign of the plant high frequency gain k_p. Besides, if $G_p(\delta)$ owned a constant value, $\dot{V}$ would be negative tending to zero while e_1 is decreasing. However, $G_p(\delta)$ is a system with limited bandwidth. In this way, since m^2 is positive and α is constant with same sign as k_p, to guarantee that $\dot{V}$ is negative, it is necessary to ensure that term $\tilde{\boldsymbol{\theta}}^T \mathbf{v}\left(G_p(\delta)\tilde{\boldsymbol{\theta}}^T \mathbf{v}\right)$ remains predominantly with the same signal. To address this last constraint, it is required that the dynamic behavior of the parametric adaptation law must be considerable slower than $G_p(\delta)$. Once the dynamic behavior of the parametric adaptation law is a function of α it is inferred that $G_p(\delta)$ bandwidth (BW_p) must satisfy (33) to ensure system stability.

$$BW_p >> |\alpha|. \quad (33)$$

Actually, the constraint given in (33) can be seen as a design guideline for the magnitude of α. Being $sign(\alpha) = sign(k_p)$ as above mentioned.

REFERENCES

[1] P. S. Almeida, D. Camponogara, M. A. D. Costa, J. M. Alonso, "Matching LED and Driver Life Spans: A Review of Different Techniques"*IEEE Industrial Electronics Magazine*, vol. 9, no. 2, pp. 36–47, Jun. 2015.

[2] C. Branas, F. J. Azcondo, J. M. Alonso, "Solid-state lighting: A system review"*IEEE Industrial Electronics Magazine*, vol. 7, no. 4, pp. 6–14, Dec. 2013.

[3] IEEE Power Electronics Society, *IEEE Std 1789 – Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers*, 2015.

[4] M. Schratz, C. Gupta, T. J. Struhs, K. Gray, "A New Way to See the Light: Improving Light Quality with Cost-Effective LED Technology"*IEEE Industry Applications Magazine*, vol. 22, no. 4, pp. 55–62, May 2016.

[5] S. Li, S. C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, C. K. Tse, "A Survey, Classification, and Critical Review of Light-Emitting Diode Drivers"*IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[6] Y. Wang, Y. Guan, J. Huang, W. Wang, D. Xu, "A Single-Stage LED Driver Based on Interleaved Buck - Boost Circuit and LLC Resonant Converter"*IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 3, pp. 732–741, Sep. 2015.

[7] Y. Wang, S. Gao, Y. Guan, J. Huang, D. Xu, W. Wang, "A Single-Stage LED Driver Based on Double LLC Resonant Tanks for Automobile Headlight With Digital Control"*IEEE Transactions on Transportation Electrification*, vol. 2, no. 3, pp. 357–368, Sep. 2016.

[8] J. Ma, X. Wei, L. Hu, J. Zhang, "LED driver based on boost circuit and LLC converter"*IEEE Access*, vol. 6, pp. 49588–49600, 2018.

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

325

[9] H. Ma, Y. Li, Q. Chen, L. Zhang, J. Xu, "A Single-Stage Integrated Boost-LLC AC-DC Converter with Quasi-Constant Bus Voltage for Multichannel LED Street-Lighting Applications"*IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1143–1153, Sep. 2018.

[10] H. Dong, X. Xie, F. Mao, L. Zhang, Y. He, "A Novel Primary-Side Regulation Control Scheme for CCM and DCM LLC LED Driver Based on 'Magnetizing Current Cancellation Method'"*IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12223–12237, Nov. 2020.

[11] H. Ma, W. Yu, C. Zheng, J. S. Lai, Q. Feng, B. Y. Chen, "A universal-input high-power-factor PFC pre-regulator without electrolytic capacitor for PWM dimming LED lighting application"*in IEEE Energy Conversion Congress and Exposition*, 2011.

[12] G. M. Soares, J. M. Alonso, H. A. Braga, "Investigation of the Active Ripple Compensation Technique to Reduce Bulk Capacitance in Offline Flyback-Based LED Drivers"*IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5206–5214, Jun. 2018.

[13] H. A. Ahn, S. K. Hong, O. K. Kwon, "A Highly Accurate Current LED Lamp Driver with Removal of Low-Frequency Flicker Using Average Current Control Method"*IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8741–8753, Oct. 2018.

[14] M. F. Menke, A. R. Seidel, R. V. Tambara, "LLC LED Driver Small-Signal Modeling and Digital Control Design for Active Ripple Compensation"*IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 387–396, Jan. 2019.

[15] C. Liu, J. Wang, K. Colombage, C. Gould, B. Sen, D. Stone, "Current Ripple Reduction in 4kW LLC Resonant Converter Based Battery Charger for Electric Vehicles"*in Energy Conversion Congress and Exposition (ECCE)*, pp. 6014–6021, 2015.

[16] Z. Zhang, Y. Q. Wu, D. J. Gu, Q. Chen, "Current Ripple Mechanism with Quantization in Digital LLC Converters for Battery Charging Applications"*IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1303–1312, Feb. 2018.

[17] J. Jang, M. Joung, B. Choi, S. Hong, S. Lee, "Dynamic analysis and control design of optocoupler-isolated LLC series resonant converters with wide input and load variations"*IET Power Electronics*, vol. 5, no. 6, pp. 755–764, Jul. 2012.

[18] S. K. Pidaparthy, J. Jang, B. Choi, "Push-pull mode digital control for LLC series resonant dc-to-dc converters"*IET Power Electronics*, vol. 8, no. 11, pp. 6098–6113, Nov. 2015.

[19] Z. Fang, J. Wang, S. Duan, K. Liu, T. Cai, "Control of an LLC Resonant Converter Using Load Feedback Linearization"*IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 887–898, Jan. 2018.

[20] H. Ma, Q. Liu, J. Guo, "A Sliding-Mode Control Scheme for LLC Resonant DC/DC Converter with Fast Transient Response"*in IEEE Energy Conversion Congress and Exposition*, pp. 161–166, 2012.

[21] Z. Zhiyuan Hu, Y.-F. Yan-Fei Liu, P. C. Sen, "Bang-Bang Charge Control for LLC Resonant Converters"*IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 1093–1108, Feb. 2015.

[22] T. Nishimura, Y. Adachi, Y. Ohta, K. Higuchi, E. Takegami, "Robust Digital Control for an LLC Current- Resonant DC-DC Converter"*in 9th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, pp. 1–4, 2012.

[23] M. F. Menke, R. V. Tambara, Á. R. Seidel, "Model reference adaptive control in discrete-time applied on the LLC LED driver"*in Congresso Brasileiro de Automática CBA2018*, João Pessoa, 2018.

[24] W. Feng, F. C. Lee, P. Mattavelli, "Optimal Trajectory Control of Burst Mode for LLC Resonant Converter"*IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 457–466, Jan. 2013.

[25] M. Bodson, Scott Douglas, "Adaptive algorithms for the rejection of sinusoidal disturbances with unknown frequency"*Automatica*, vol. 22, no. 12, pp. 2213–2221, Dec. 1997.

[26] S. Pigg, M. Bodson, "Adaptive rejection of sinusoidal disturbances of known frequency acting on unknown systems"*Proceedings of the American Control Conference*, vol. 2006, no. 2, pp. 4777–4781, 2006.

[27] W. Kim, H. Kim, C. C. Chung, M. Tomizuka, "Adaptive output regulation for the rejection of a periodic disturbance with an unknown frequency"*IEEE Transactions on Control Systems Technology*, vol. 19, no. 5, pp. 1296–1304, Sep. 2011.

[28] R. Erickson, D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Springer, 2001.

[29] P. A. Ioannou, K. S. Tsakalis, "A robust direct adaptive controller"*IEEE Transactions on Automatic Control*, vol. 31, no. 11, pp. 1033–1043, Nov. 1986.

[30] P. A. Ioannou, J. Sun, *Robust Adaptive Control*, 1st ed., Nov. 2012.

[31] H. Wu, *Multi-Channel Constant Current (MC 3) LED Driver for Indoor LED Luminaries*, Master of science thesis, Faculty of the Virginia Polytechnic Institute, 2011.

[32] ENERGY STAR, "Program Requirements for Luminaires Partner Commitments - Version 2.2", 2019.

[33] Bridgelux, "Bridgelux Vero 18 array series - Product Data Sheet DS3", 2013.

[34] R. L. Lin, S. Y. Liu, C. C. Lee, Y. C. Chang, "Taylor-series-expression-based equivalent circuit models of LED for analysis of LED driver system"*IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1854–1862, Jul./Aug. 2013.

[35] K. Ogata, *Discrete-time control systems*, 2nd ed., Prentice Hall, 1995.

[36] Texas Instruments, "Tiva TM4C1294NCPDT Microcontroller", 2014.

326

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

BIOGRAPHIES

Maikel F. Menke, born in 1989, in Três de Maio - RS. He received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 2015, 2016, and 2021, respectively.

Since 2019, he is a Professor at the Federal Institute of Santa Catarina (IFSC). His research interests include lighting applications, dc-dc converters, power factor correction, resonant converters, and self-oscillating converters. Dr. Menke is member of the SOBRAEP, and IEEE.

J. Marcos Alonso received the M. Sc. Degree and Ph.D. Degree (with honors) both in electrical engineering from the University of Oviedo, Spain, in 1990 and 1994 respectively.

Since 2007, he is a full Professor of the Electrical Engineering Department of the University of Oviedo. Prof. Alonso is co-author of more than 450 journal and conference publications, including more than 120 publications in highly referenced journals, 3 books and 2 book chapters. His research interests include lighting applications, dc-dc converters, power factor correction, resonant inverters, and single-phase power electronics in general. He is the holder of 8 national and international patents. Prof. Alonso holds 11 IEEE awards. He currently serves as a Co-Editor-in-Chief of the IEEE Transactions on Power Electronics and Associate Editor of the IEEE Journal on Emerging and Selected Topics on Power Electronics. He was the Chair of the IEEE IAS Industrial Lighting and Displays Committee.

Rodrigo V. Tambara was born in Santa Maria, Brazil, in 1987. He received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil, in 2008, 2010, and 2014, respectively.

From 2014 to 2016, he was an Adjunct Professor with the Universidade Franciscana, Santa Maria, Brazil. From 2016 to 2018, he was an Adjunct Professor with the Federal University of Santa Maria, Cachoeira do Sul, Brazil. Currently, he is with the Federal University of Santa Maria, where he is a Adjunct Professor with the Colégio Técnico Industrial de Santa Maria. He has been a Researcher with Power Electronics and Control Group (GEPOC) since 2004, and with the Electrical and Computational Systems Research and Development Group (GSEC) since 2015. His research interests include adaptive control, grid-connected converters, dimming systems, and LED drivers. Dr. Tambara is a member of the Brazilian Power Electronics Society and also a member of the Brazilian Automatic Control Society.

Álysson R. Seidel was born in São Pedro do Sul, Brazil, in 1975. He received the B.S. and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil, in 1999 and 2004, respectively.

From 2004 to 2008, he was an Associate Professor in the Department of Electrical Engineering, University of Passo Fundo, Passo Fundo, Brazil. Currently, he is at Federal University of Santa Maria, where he is a Professor at the Technical Industrial School of Santa Maria and a Researcher in Electronic Ballast Research Group (GEDRE) since 1997 and Electrical and Computational Systems Research and Development Group (GSEC) since 2010. His research interests include resonant converters, dimming systems, simulation, discharge lamps, and lighting systems.

Eletrôn. Potên., Fortaleza, v. 26, n. 3, p. 315-327, jul./set. 2021

327