PROPOSAL, ANALYSIS AND EXPERIMENTAL VERIFICATION OF NONISOLATED DC-DC CONVERTERS CONCEIVED FROM AN ACTIVE SWITCHED-CAPACITOR COMMUTATION CELL

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***Abstract* – This paper introduces a new family of nonisolated dc-dc converters that are generated by the integration of the active switched-capacitor (ASCC) and the conventional commutation cell (CCC). Based on the commutation cell concept, the new conceived hybrid active commutation cell (HACC) provides three different types of hybrid converters: buck, boost and buck-boost. All three converters are investigated in this study through the following approaches: topological stages, static gain analysis considering the switched - capacitor features, generalization of the HACC and gain for *M* cells and steady-state analysis. The buck version presents a high conversion rate, which demonstrates that it has potential for step-down applications. To verify the proposed topologies, a prototype was built with the following specifications: 600 V input voltage, 150 V output voltage, 70 kHz switching frequency and 1 kW rated power. Efficiency close to 95% was obtained at 1 kW for the buck topology, which demonstrates that the proposed HACC can provide gain and high efficiency at the same time.**

***Keywords* – Active Switched-Capacitor Cell, Commutation Cell Concept, Experimental Results.**

I. INTRODUCTION

The recent growth in the development and use of HVDC transmission systems, DC distributed systems, DC smart grids, electrical vehicles, energy storage systems, renewable sources, and telecommunication systems has enhanced the need for new solutions for dc-dc conversion. This scenario brings new applications for dc-dc converters and challenges associated with managing the energy flow in these systems.

More specifically, the current challenge in relation to dc-dc conversion is to offer a high conversion ratio without isolation, for step-up or step-down applications. The isolated converters use the transformer turns ratio value to provide gain. However, the transformer is a bulky component and when a high gain is required the intrinsic parameters become significant and this offsets its benefits [1], [2]. Recently, topologies based on switched-inductor [3]–[8], switched-capacitor [3], [6]–[14], coupled inductor [3], [15], [16], impedance source circuit [3], [17], [18], series and parallel connections [19], [20], ladder [12], [14] and stacked connection [21]–[23] have provided alternative ways to obtain high gain, but all of them use a higher number of components.

The switched capacitor (SC) principle is one way to multiply or divide dc voltage. The SC converters are applied in boost topologies [10], [24], [25] as well as in buck topologies [26]. They are capable of supplying a high conversion ratio and they are magneticless topologies. Almost all the structures have good voltage stress sharing across components and, when they are properly designed, they can provide high efficiency, high power density and low weight [27]. However, the output voltage regulation is not as easy as in a conventional converter and this represents a challenge in the design of SC converters. Many authors have addressed this issue in the literature [10], [26].

On the other hand, the conventional converters present good output voltage regulation, but are not capable of providing a high conversion ratio. Hence, the integration between SC and conventional circuits could allow the combination of the advantages of the two groups of converters while overcoming the drawbacks [7], [11], [26]. This new family of converters is referred to in the literature as hybrid converters.

In general, SC cells are integrated with conventional converters to generate new topologies [7], [11], [28]-[30]. However, this concept was approached in relation to commutation cell, and a passive ladder SC cell was integrated with conventional commutation cell [11]. The new converters are analyzed through the commutation cell.

In this context, this paper proposes a hybrid active commutation cell (HACC) generated through the integration of the active switched-capacitor cell (ASCC) and the conventional commutation cell (CCC). The proposed cell generate three hybrid converters of different types: hybrid buck, hybrid boost and hybrid buck-boost. These structures present modified static gain in relation to [11] and the conventional converters. Hence, they have advantages that can be used in certain applications and thus, they can expand the range of applications of hybrid converters. A preliminary study just about buck topology was presented in [31], in which the topology was approached without considering the commutation cell principle.

The paper is divided as follows: firstly, the way in which the ASCC was integrated with the CCC is described and the

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new converters generated by this combination are presented. Subsequently, a theoretical analysis of the hybrid buck topology is shown, addressing the main characteristics of the topology. Finally, experimental results are presented to validate the proposed topologies.

II. . INTEGRATION OF AN ACTIVE SWITCH CAPACITOR CELL WITH THE CONVENTIONAL DC-DC CELL

The conventional dc-dc cell (see Figure 1.a) is employed to generate the buck, boost and buck-boost classical converters. The ladder SC cell is used to provide step-up or step-down circuits, where the gain can be increased by adding more cells in a ladder connection [32]. This implementation can use passive (diodes) or active (MOSFET, IGBT, SIC, GAN) switches. The cell proposed herein is generated connecting the CCC (Figure 1.a) and the ASCC (Figure 1.b) in a ladder configuration. To generate the proposed HACC (Figure 1.c), the terminals n_1 and c_1 of the CCC are connected, respectively, with the terminals b_2 and a_2 of the ASCC, as shown in Figures 1.a, 1.b and 1.c. The HACC employs three switches (S_1, S_2 and S_3), one diode (D_1), three capacitors (C_1, C_2 and C_3) and one inductor (L). The resultant cell has three terminals, labelled 'a', 'b' and 'c', in which the input dc-dc source and the output load are connected.

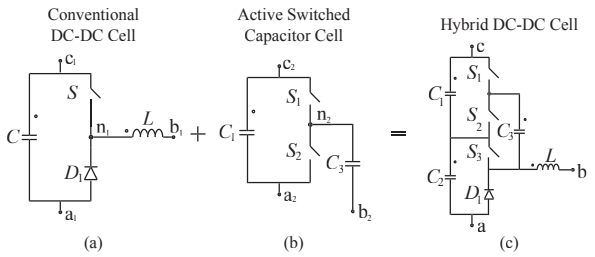


Fig. 1. (a) Conventional dc-dc cell (CCC); (b) active switched-capacitor cell (ASCC), and; (c) hybrid dc-dc cell (HACC).

The topologies derived from the HACC have the input and output connections described in Table I. With these connections, a family of three new nonisolated dc-dc converters is generated, as is shown in Figures 2.a, 2.b and 2.c. The topologies are named as follows: hybrid dc-dc buck converter (Figure 2.a), hybrid dc-dc boost converter (Figure 2.b) and hybrid dc-dc buck-boost converter (Figure 2.c). It should be highlighted that the names buck, boost and buck-boost are used in relation to the connections between input and output stages and do not necessarily reflect the gain characteristics of the structures.

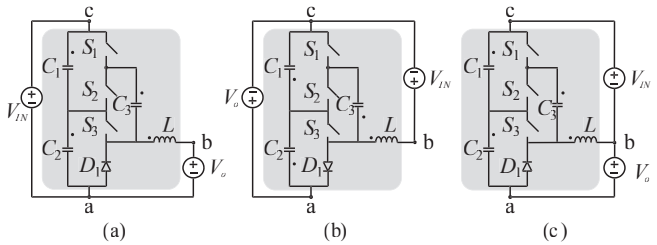


Fig. 2. (a) Hybrid dc-dc buck converter; (b) hybrid dc-dc boost converter, and; (c) hybrid dc-dc buck-boost converter.

A similar approach was proposed in [11], where a hybrid commutation cell was derived from a passive switched-capacitor cell (implemented only with diodes). The two commutation cells are similar, with the ladder configuration and the same number of semiconductors, however, the proposed HACC uses three active and one passive switch while the commutation cell in [11] employs one active and three passive switches. Additionally, the converters generated by the integration of an active and a passive cells present different static gains, different topological stages and are suitable for different applications, as will be presented and discussed in greater detail in Section III and IV.

One of the advantages of SC circuits is that more SC cells ('*M*' cells) can be used to increase the conversion rate, as shown in Figure 3. This figure present the generalized hybrid dc-dc buck converter, which can provide a high step-down gain. The generalized boost and buck-boost topologies can be also obtained, following the input and output connections shown in Table I. The ladder configuration has the advantage that the voltage stress on the power components are equally divided and clamped by the switched capacitors, thus when more SC cells are added the gain will increase but the voltage stress will remain constant.

TABLE I
Connections Used to Generate the Three Proposed dc-dc Converters

Converter	Terminals connected	
	Input	Output
H-buck	ca	ba
H-boost	bc	ac
H-buck-boost	cb	ba

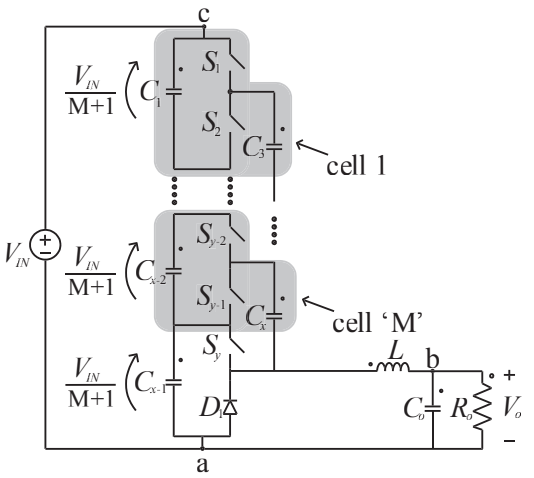


Fig. 3. Generalization of the switched-capacitor cell for the proposed hybrid dc-dc buck converter.

III. THEORETICAL ANALYSIS OF THE BUCK TOPOLOGY

This section presents the theoretical analysis for the buck converter (Figure 2.a), which is then extended to the boost and buck-boost topologies (Figures 2.b and 2.c).

A. Topological Stages

The topologies presented in Figures 2.a, 2.b and 2.c have two topological stages, as shown in Figure 4 and detailed below:

- ***First Topological Stage:*** the PWM1 signal turns on S_1 and S_3, while PWM 2 (complementary to the PWM1 signal) turns off S_2. With this driving command, capacitors C_1 and C_3 are parallel connected and both capacitors charge, while capacitor C_2 discharges. In this topological stage, the inductor stores energy. The equations extracted from this stage are given in (1). The equivalent series resistance of the capacitors (r_C) was considered during the analysis.
- ***Second Topological Stage:*** the PWM2 signal drives switch S_2, which turns on it, while PWM 1 turns off S_1 and S_3. Capacitor C_3 starts to discharge and hence diode D_1 is forward biased. The capacitor C_1 discharges, capacitor C_2 charges and the inductor provides energy to the load. The equations extracted from this stage are given in (2).

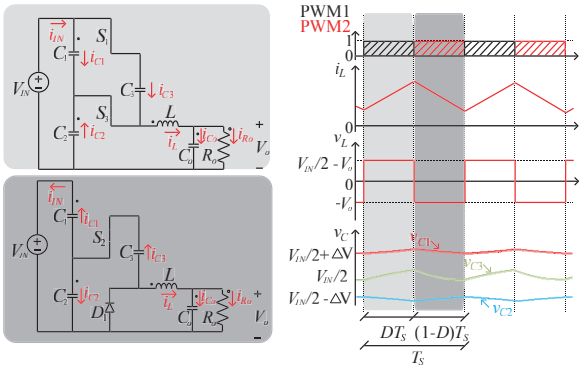


Fig. 4. Hybrid dc-dc buck converter: First (upper figure in light gray) and second (lower figure in dark gray) topological stages, and main waveforms for one switching period (right figure).

$$\begin{cases} v_L = i_{C2}r_C + v_{C2} - v_o \\ V_{IN} = i_{C1}r_C + v_{C1} + i_{C2}r_C + v_{C2} \\ i_L = i_{C1} + i_{C2} + i_{C3} \\ i_{C1}r_C + v_{C1} = i_{C3}r_C + v_{C3} \\ i_L = i_{Co} + i_{Ro} \end{cases}. \quad (1)$$

$$\begin{cases} v_L = -v_o \\ V_{IN} = i_{C1}r_C + v_{C1} + i_{C2}r_C + v_{C2} \\ i_{C3} = i_{C1} + i_{C2} \\ i_{C2}r_C + v_{C2} = i_{C3}r_C + v_{C3} \\ i_L = i_{Co} + i_{Ro} \end{cases}. \quad (2)$$

It should be highlighted that there is no discontinuous conduction mode (DCM) in the proposed HACC. During the second topological stage, if the inductor current reaches zero, it will become negative, because there is a closed circuit between C_2, C_3, S_2, L and R_o for this current to flow. Thus, there is no DCM. The topological stages described in this section are valid for the three converters generated from the HACC.

B. Switched-Capacitor Cell

The SC cell can be modeled as an equivalent resistance (R_{eq}), as shown in Figure 5, and the value of this resistance is defined in (3) [33] as a function of the switched frequency (f_s), the duty cycle (D) and the time constant (τ) given by (4):

$$R_{eq} = \frac{1}{f_s C_3} \frac{1 - e^{\frac{-1}{f_s \tau}}}{1 - e^{\frac{-D}{f_s \tau}} - e^{\frac{-(1-D)}{f_s \tau}} + e^{\frac{-1}{f_s \tau}}}, \quad (3)$$

$$\tau = C_3 \underbrace{\left(r_{on} + r_C\right)}_{r}, \quad (4)$$

where, r is the total conduction resistance of the multiplier cell and r_{on} is the conduction resistance of the semiconductors.

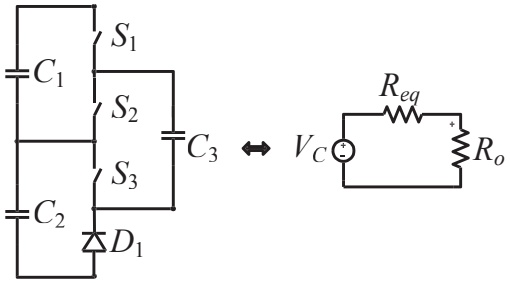


Fig. 5. Complete SC cell and equivalent circuits.

Isolating C_3 in (4) and substituting in (3), the behavior of R_{eq} as a function of $f_s\tau$ is shown in Figure 6.a, for a fixed D equal to 0.5, which provides the maximum cell gain, as seen in Figure 7. It should be noted that the equivalent resistance value affects the mode of operation of the SC cell. There are three different modes of operation: total charge, partial charge and no charge. In total charge mode, Figure 6.b, the capacitor current has higher peak values, which will lead to greater losses. In no charge mode, Figure 6.d, there are no current peaks, however, high capacitance values are required. In the partial charge mode, Figure 6.c, the current peaks are smaller than in the total charge mode and it is not necessary to use high capacitance values. Thus, the partial charge mode provides a better cost/benefit in terms of volume and efficiency.

It should be noted that, the partial charge mode is obtained when the charging interval (DT_s) is lower than 5τ [33]:

$$DT_s \leq 5\tau = 5rC_3 = 5\left(r_{on} + r_C\right)C_3, . \quad (5)$$

The minimum capacitance, for a fixed D equal to 0.5, is given by:

$$C = C_1 = C_2 = C_3 \geq \frac{0.1}{f_s\left(r_{on} + r_c\right)}. \quad (6)$$

The boundary between partial charge and no charge mode occurs in $f_s\,\tau$ equal to 1.44 [33]. In this point, the equivalent resistance varies less than 1%, when the $f_s\,\tau$ is increased. Thus, after this point the no charge mode can be considered. Based on that point, the maximum capacitance can be calculated by:

$$C = C_1 = C_2 = C_3 \leq \frac{1.44}{f_s\left(r_{on} + r_c\right)}. \quad (7)$$

On analyzing the circuit of Figure 5, the real gain of the SC cell, considering the charge and discharge of the capacitors, is given by:

$$G_{SC} = \frac{V_{Ro}}{V_C} = \frac{R_o}{R_o + R_{eq}}, \quad (8)$$

and thus, the generalized gain is given by:

$$G_{SCM} = \frac{MR_o}{R_o + R_{eq}}. \quad (9)$$

The SC cell static gain for '*M*' cells is shown in Figure 7, considering $R_o >> R_{eq}$ (about 100 times). It should be highlighted that the maximum gain occurs close to D=0.5.

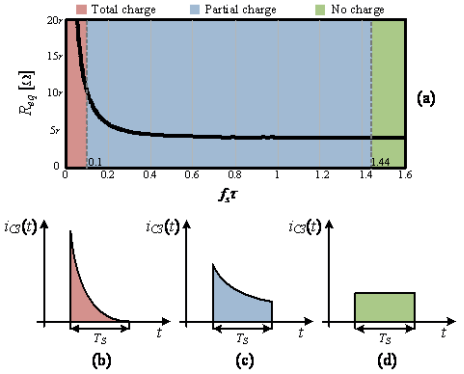


Fig. 6. SC cell behavior: (a) R_{eq} as a function of $f_s\tau$, and with current in C_3 for (b) total charge mode, (c) partial charge mode and (d) no charge mode.

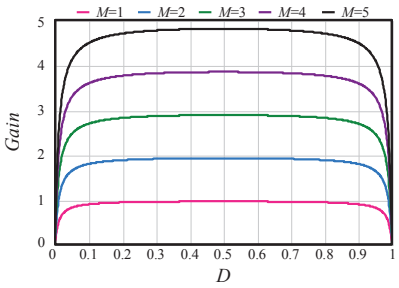


Fig. 7. Voltage gain for 'M' SC cells.

C. Static Gain of the Proposal Topologies

The ideal static gain of the buck converter derived from HACC can be obtained from the energy balance in the inductor:

$$v_{C2}D - v_oD = v_o(1-D), \quad (10)$$

where:

$$v_{C2} = \frac{V_{IN}}{M+1}. \quad (11)$$

Substituting (11) in (10), the static gain of the topology as a function of the number of SC cells (M) is described as:

$$G_{buck} = \frac{v_o}{V_{IN}} = \frac{D}{M+1}. \quad (12)$$

Similarly, the gains of the proposed hybrid boost and buck-boost converters can be given as follows:

$$\begin{cases} G_{boost} = \dfrac{(M+1)}{(M+1)-D} \\ G_{buck\_boost} = \dfrac{D}{(M+1)-D} \end{cases}. \quad (13)$$

The static gains provided by (12) and (13) are valid for the whole operation range of these topologies, because they have no DCM. This is an important feature provided by the proposed HACC, which distinguishes it from other solutions (such as [11]).

The real static gain of the hybrid buck, boost and buck-boost can be described as a function of the SC gain given by (14). The real static gain considers the SC losses due to the charge and discharge of the capacitors, which are inherent to the principle of SC operation.

In Figures 8.a, 8.b and 8.c the ideal static gain behavior for equations (12) and (13) can be observed, considering '*M*' ASCC for the buck, boost and buck-boost converter, in this order. The addition of the ASCC does not change the linear gain characteristic of the buck converter, as shown in Figure 8.a. For the boost and buck-boost topologies derived from the ASCC cell, the gain behavior is still non-linear, however it is limited, respectively, to between $1 < G_{boost} < 2$ and $0 < G_{buck\text{-}boost} < 1$.

It should be noted that the converters received the names buck, boost and buck-boost because of the input and output connections on the hybrid cell, and this does not necessarily mean that their behavior is similar with the conventional dc-dc converters. For example, the buck-boost converter obtained from the hybrid dc-dc cell proposed herein only operates as a step-down converter, while the conventional buck-boost can operate as a step-down and step-up converter.

$$\begin{cases} G_{r\_buck} = \left(\dfrac{D}{M+1}\right)\left(\dfrac{R_o}{R_o+R_{eq}}\right) \\ G_{r\_boost} = \left(\dfrac{(M+1)}{(M+1)-D}\right)\left(\dfrac{R_o}{R_o+R_{eq}}\right) \\ G_{r\_buckboost} = \left(\dfrac{D}{(M+1)-D}\right)\left(\dfrac{R_o}{R_o+R_{eq}}\right) \end{cases}. \quad (14)$$

Figures 8.d, 8.e and 8.f show the static gain curve considering the real gain of the SC cell given by (14), considering $R_o >> R_{eq}$ (about 100 times). When comparing the real gain curve with the ideal curve it should be highlight that for D<0.1 and D>0.9 the gain of the converters decreases.

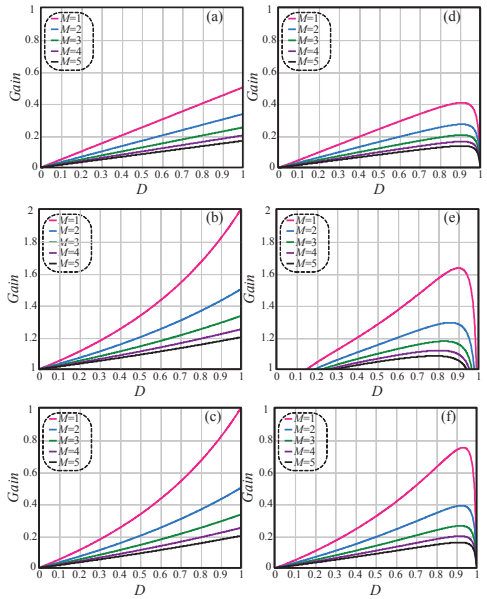


Fig 8. Static gain of the three converters derived from the hybrid dc-dc cell for different numbers of SC cells: (a) buck ideal static gain; (b) boost ideal static gain; (c) buck-boost ideal static gain; (d) buck real static gain; (e) boost real static gain; and (f) buck-boost real static gain.

D. Steady-State Analysis

The equations in (1) and (2) can be used to obtain the coefficients of the matrixes A_1 and B_1, for the first topological stage, and A_2 and B_2 for the second topological stage, respectively. Capacitances C_1, C_2 and C_3 are considered equal in this analysis, and the result is presented in Table II for the buck converter conceived from the HACC.

To be able to calculate the steady-state equations of the system, the matrixes shown in Table II are substituted in:

$$\begin{cases} A = A_1 D + A_2 (1-D) \\ B = B_1 D + B_2 (1-D) \end{cases}, \tag{15}$$

and, after mathematical manipulations using:

$$\dot{x} = Ax + Bu \xrightarrow{\text{steady state}} 0 = Ax + Bu, \tag{16}$$

where u is the input voltage (V_{IN}) of the circuit, the steady-state equations for the inductor current and the voltage across all of the capacitors are given in (17), including and not including the *ESR* resistance r_C.

On analyzing the topological stages shown in Figure 4, the semiconductors from the power stage are submitted to a voltage stress equal to half of the input voltage, instead of the entire input voltage, as occurs in the conventional buck converter. This feature is confirmed by theoretical steady-state analysis described by:

$$\underbrace{\begin{pmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{Co} \end{pmatrix}}_{X_o} = \begin{pmatrix} \frac{4V_{IN}D(1-D)}{8(1-D)R_o + 3Dr_C} \\ \frac{V_{IN}\left[4(1-D)R_o + Dr_C(D+2)\right]}{8(1-D)R_o + 3Dr_C} \\ \frac{(1-D)V_{IN}(4R_o + Dr_C)}{8(1-D)R_o + 3Dr} \\ \frac{V_{IN}\left[4(1-D)R_o + Dr_C(2D+1)\right]}{8(1-D)R_o + 3Dr} \\ \frac{4V_{IN}DR_o(1-D)}{8(1-D)R_o + 3Dr} \end{pmatrix} \xrightarrow{r_c = 0} \begin{pmatrix} \frac{V_{IN}}{2R_o} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}D}{2} \end{pmatrix} \tag{17}$$

It should be noted that the element X_{51} of the resulting vector presented in (17) is similar to (12), which represents the gain of the buck converter in CCM, corroborating the steady-state analysis presented above. The analysis can be directly extended to the boost and buck-boost converters derived from the proposed HACC.

IV. COMPARISON BETWEEN THE PROPOSED CONVERTERS AND OTHER SOLUTIONS

Table III shows a comparison of the topologies proposed herein with conventional topologies (buck, boost and buck-boost), the 3-level buck converter and structures proposed in [11]. The comparison is made in relation to the static gain range, voltage stress on the power semiconductors, and number of components.

In the buck structure, the addition of one ASCC to the conventional commutation cell reduces the voltage stress on the power semiconductors to half in relation to the conventional buck converter. However, as a drawback, the new topology has two extra controllable switches and three more capacitors. The proposed buck topology presents a limited voltage gain from zero to half of the input voltage, and thus a comparison is made in Table III in relation to the 3-level buck converter [31], since both topologies present the same static gain.

The proposed boost topology can be compared to the conventional boost and buck-boost converters. The voltage gain profile of the proposed boost converter starts from unity and stops at twice, when operating with the maximum duty cycle. A similar gain is obtained either with a conventional boost topology working in a limited duty cycle range of 0 to 0.5, or with a conventional buck-boost topology with a duty cycle range of 0.5 to 0.67. However, despite using a greater number of components, the proposed boost topology presents a significant reduction in the stress in all power switches ($V_o/2$) and more accurate output voltage variation, as previously mentioned.

The proposed buck-boost topology is a step-down converter, which is equivalent to either the conventional buck-boost topology operating with a duty cycle range of 0 to 0.5 or the conventional buck converter. A disadvantage of the proposed buck-boost topology is the greater number of components compared to conventional converters. Nevertheless, the buck-boost converter offers lower voltage stress in all power switches ($(V_{IN}+V_o)/2$) in relation to the conventional buck-boost converter ($V_{IN}+V_o$). Thus, it is suitable for high voltage applications.

TABLE II

Matrix Analysis to Obtain the Steady-State Equations that Represent the Main Characteristics of the Hybrid dc-dc Buck Converter.

A_1	A_2	B_1	B_2
$\begin{pmatrix} \frac{-r_C}{3L} & \frac{-1}{3L} & \frac{1}{3L} & \frac{-1}{3L} & \frac{-1}{L} \\ \frac{1}{3C} & \frac{-2}{3r_CC} & \frac{-1}{3r_CC} & \frac{1}{3r_CC} & 0 \\ \frac{-1}{3C} & \frac{-1}{3r_CC} & \frac{-2}{3r_CC} & \frac{-1}{3r_CC} & 0 \\ \frac{1}{3C} & \frac{1}{3r_CC} & \frac{-1}{3r_CC} & \frac{-2}{3r_CC} & 0 \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{R_oC_o} \end{pmatrix}$	$\begin{pmatrix} 0 & 0 & 0 & 0 & \frac{-1}{L} \\ 0 & \frac{-2}{3r_CC} & \frac{-1}{3r_CC} & \frac{-1}{3r_CC} & 0 \\ 0 & \frac{-1}{3r_CC} & \frac{-2}{3r_CC} & \frac{1}{3r_CC} & 0 \\ 0 & \frac{-1}{3r_CC} & \frac{1}{3r_CC} & \frac{-2}{3r_CC} & 0 \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{R_oC_o} \end{pmatrix}$	$\begin{pmatrix} \frac{2}{3L} \\ \frac{1}{3r_CC} \\ \frac{2}{3r_CC} \\ \frac{1}{3r_CC} \\ 0 \end{pmatrix}$	$\begin{pmatrix} 0 \\ \frac{2}{3r_CC} \\ \frac{1}{3r_CC} \\ \frac{1}{3r_CC} \\ 0 \end{pmatrix}$

TABLE III
Qualitative and Quantitative Comparison between the Proposed Topologies and Other Converters

Topology	Gain	V_{S1}	V_{Dmax}	Number of			
				C	S	D	L
C-Buck[1]	D	V_{IN}	V_{IN}	1	1	1	1
3-Level Buck [26]	$\frac{D}{2}$ to (D<0.5) $\frac{1+D}{2}$ to (D>0.5)	$\frac{V_{IN}}{2}$	$\frac{V_{IN}}{2}$	2	4	0	1
H-Buck[2]	$\frac{1+D}{2}$ to $(0 \le D \le 1)$	$\frac{V_{IN}}{2}$	$\frac{V_{IN}}{2}$	3	1	3	1
H-Buck[3]	$\frac{D}{2}$ to $(0 \le D \le 1)$	$\frac{V_{IN}}{2}$	$\frac{V_{IN}}{2}$	4	3	1	1
C-Boost[1]	$\frac{1}{1-D}$	V_o	V_o	1	1	1	1
H-Boost[2]	$\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	3	1	3	1
H-Boost[3]	$\frac{2}{2-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	4	3	1	1
C-Buck-Boost[1]	$\frac{D}{1-D}$	$V_{IN}+V_o$	$V_{IN}+V_o$	1	1	1	1
H-Buck-Boost[2]	$\frac{1+D}{1-D}$	$\frac{V_{IN}+V_o}{2}$	$\frac{V_{IN}+V_o}{2}$	3	1	3	1
H- Buck-Boost[3]	$\frac{D}{2-D}$	$\frac{V_{IN}+V_o}{2}$	$\frac{V_{IN}+V_o}{2}$	4	3	1	1

[1] Conventional DC-DC converters.
[2] Converters proposed in [11].
[3] Converters proposed in this paper based on the HACC.

On comparing the topologies proposed in this paper with those addressed in [11], it is possible to conclude that the two types of topology together reconstruct the static gain behavior of the conventional buck, boost and buck-boost converters, as can be seen in Table III. This is obtained with less effort in relation to the voltage stresses and duty cycle. Hence, when a higher conversion rate is needed, one of the topologies proposed herein or in [11] can be used. Therefore, the specification will determine which topology is more adequate. It should be noted that the HACC-based topologies present a larger number of controlled semiconductors when compared to the structures discussed in [11], however they always operate in CCM.

V. EXPERIMENTAL RESULTS

A prototype was designed and used to corroborate the topologies proposed in this paper, which is seen Figure 9. The prototype was built for the buck topology specification (as described in Table IV) and the components used are exposed in Table V. Using the commutation cell concept, the same prototype was also employed to verify the boost and buck-boost topologies, following the connections presented in Table I.

A. Boost Topology

To verify the hybrid boost topology (shown in Figure 2.b), an input voltage of 300 V was used and the duty cycle was set at 0.5. According to (13), an output voltage of 400 V is expected, since the gain of the structure is 4/3. Figure 10 shows V_o and V_{IN}. The output voltage measurement was 403 V, which validates the static gain of the structure. Figure 10 also shows the voltage stress of S_1, which is half of the output voltage (200 V). These results verify the gain of the proposed switched-capacitor cells and voltage stresses on the semiconductors.

B. Buck-Boost Topology

The buck-boost converter derived from the HACC (Figure 2.c) was verified with an input voltage of 300 V and duty cycle of 0.4. The theoretical gain calculated from (13) was ¼, which provides an output voltage of 75 V. The experimental results presented in Figure 11 show an output voltage of 79 V, which is only 4 V higher than the theoretical voltage (this error of 5.33% is due to the open-loop operation of the converter).

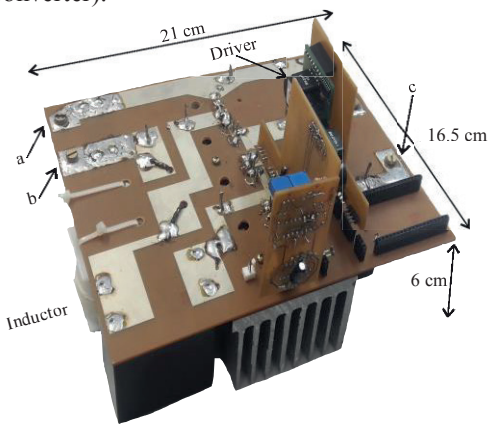


Fig. 9 . 1 kW prototype used to verify experimentally the proposed converters.

TABLE IV
Specifications of the Test Setup

Parameters	Values
Input Voltage	V_{IN} = 600 V
Output Voltage	V_o = 150 V
Output Power	P_o = 1 kW
Switching Frequency	f_s = 70 kHz
Nominal Duty Cycle	D = 0.5
Number of Cells	M=1

TABLE V
Components Used in the Prototype

Components	
Inductor L	535 µH Core: EPCOS N87–55/28/21 Number of turns: 59 Wire: 24 AWG
Switches S_1, S_2 and S_3	IPx60R099C6 – r_{on}=0.099 Ω 600 V / 24 A
Diode D_1	C3D10060A 600 V / 10 A
Capacitors C_1, C_2 and C_3	100 µF, r_c=4.7 mΩ EZPE50107MTA 500 V / 10 A

C. Buck Topology

The prototype shown in Figure 9 was developed for the hybrid buck topology. Thus, full tests were conducted in this configuration, which was designed for 1 kW rated power.

To verify the theoretical gain obtained from the steady-state analysis described in this paper, the buck topology was tested at three different operation points (D=0.3, D=0.5, D=0.7) and the experimental results are shown in Figures 12.a, 12.b and 12.c. On setting the duty cycle at D=0.3, the output voltage was 92 V, as seen in Figure 12.a [theoretical value from (9) was 90 V]. When the duty cycle was set at D=0.5, the output voltage was 154 V, as shown in Figure 12.b [theoretical value was 150 V]. Finally, on setting the duty cycle at D=0.7, the output voltage was 210 V, as seen in Figure 12.c (theoretical value was 210 V). In all cases the voltage on the switches and capacitors are independent of the duty cycle and equal to half of the input voltage, as can be seen from the measured V_{S1} and V_{C1} values. The voltages across these components are clamped by the switched capacitor C_3. The self-balance voltages provided by the switched capacitor on V_{C1} and V_{C2} are shown in Figure 13.

For the nominal duty cycle (D=0.5), load steps were performed to evaluate the regulation of the circuit from 50 W to 1.150 kW, as shown in Figure 14. As expected, since the converter operates in open-loop, the output voltage drops as the output power increases. Nevertheless, the curve presents a flat drop, which means the proposed HACC does not have high losses, even when using more components compared with the conventional commutation cell.

The efficiency was also measured for the entire power range and the result is shown in Figure 15. The efficiency curve shows a flat behavior at around 95%, above 700 W, and it reaches a peak value of 95.5% at rated power, which enables the proposed converter to step-down voltages with high efficiency.

Figure 16.a, 16.b and 16.c show how the theoretical losses are distributed among the inductor, capacitors, diode and switches in the buck, boost and buck-boost topologies, respectively. In this analysis, the resistance in the current path (r_{on} and r_c) is considered. The largest losses occurs in the buck-boost topology, which provided a theoretical efficiency of 87.74% at rated power. The inductor and diode are responsible for 40% of the total losses. The boost topology presented the greater theoretical efficiency among the three studied structures (98.77%). In the buck topology, the largest loss occurs in the diode and switches, of which 25% are commutation losses and 49% are conduction losses (theoretical values).

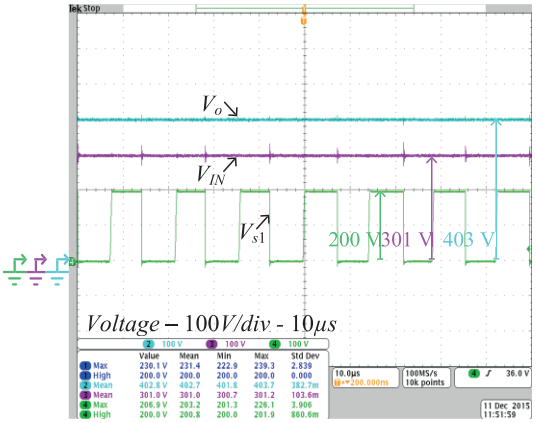


Fig. 10. Experimental results for the boost converter derived from the HACC: input voltage (V_{IN}), output voltage (V_o) and voltage stress on switch S_1 (V_{S1}).

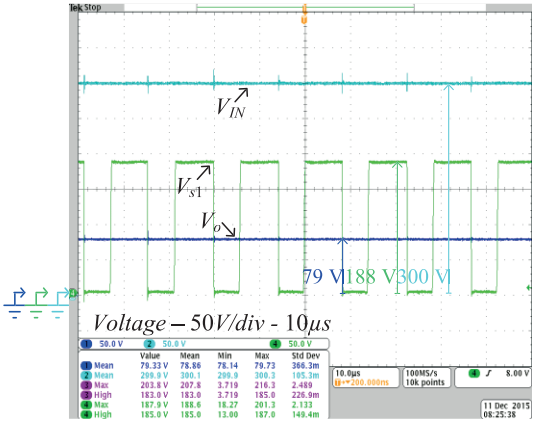
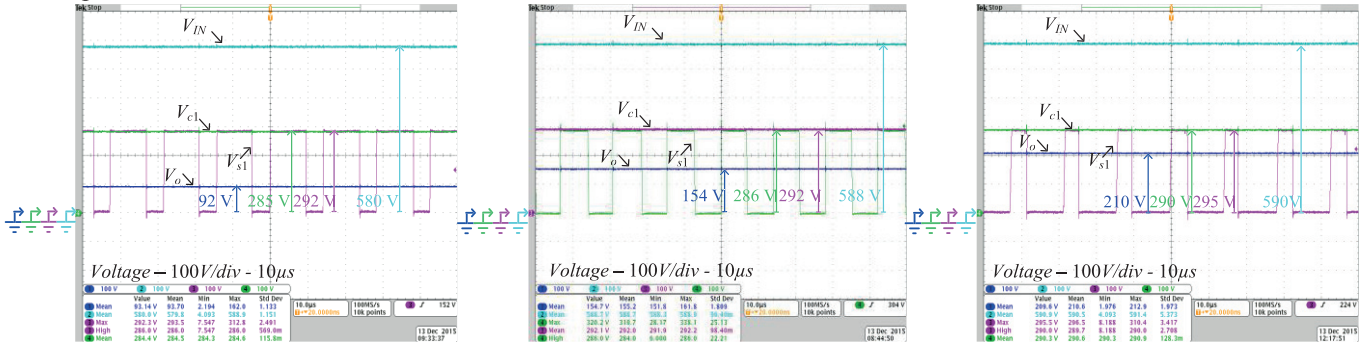


Fig. 11. Experimental results for the buck-boost converter derived from the HACC: input voltage (V_{IN}), output voltage (V_o) and voltage stress on switch S_1 (V_{S1}).



(a) (b) (c)

Fig. 12. Experimental results for the buck converter derived from the HACC: input voltage (V_{IN}), output voltage (V_o), voltage stress on switch S_1 (V_{S1}) and voltage stress on capacitor C_1 (V_{C1}). (a) for D=0.3, (b) for D=0.5 and (c) for D=0.7.

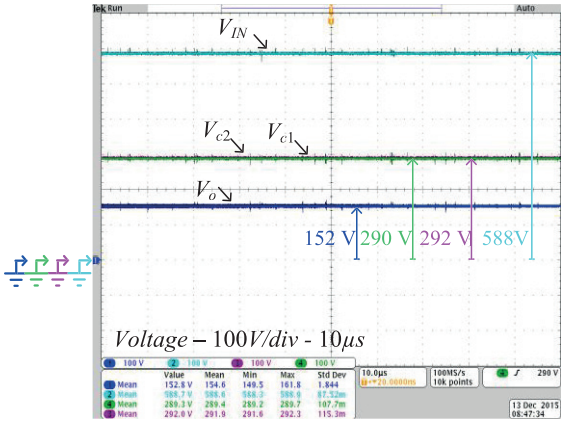


Fig. 13. Experimental results for the buck converter derived from the HACC: test to verify the self-balancing provided by the SC on capacitors C_1 and C_2.

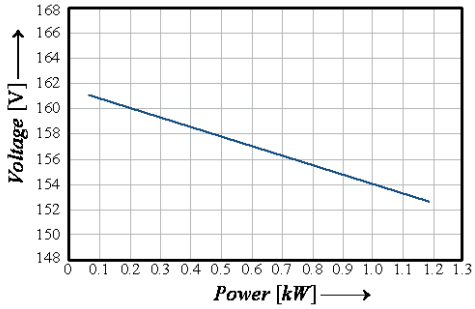


Fig. 14. Regulation of the converter for a duty cycle of D=0.5. Measurements for the entire power range.

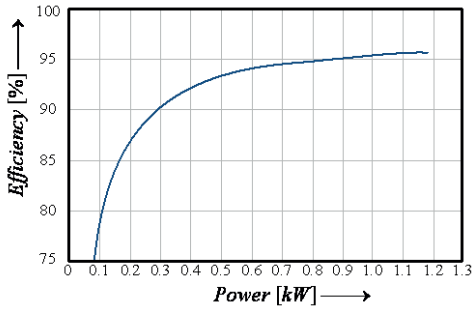


Fig. 15. Efficiency measurements for the buck converter derived from proposed HACC.

VI. CONCLUSIONS

A new hybrid dc-dc commutation cell is proposed in this paper, which is obtained through the integration of the ASCC and the CCC. The hybrid cell can generate a new family composed by three converters: a hybrid buck, a hybrid boost and a hybrid buck-boost. By changing only the input and output connections, the step-up/step-down characteristic could be achieved from the commutation cell. A bidirectional structure can be obtained by substituting the power diode D_1 for an extra active switch, as proposed in [34].

The buck, boost and buck-boost topologies provide a high resolution of output voltage adjustment in relation to the duty cycle, since they have a small range of gain for a large range of duty cycles. This feature could be beneficial for certain applications, especially for high gain converters operating in closed loop. However, as a drawback, the limited gain reduces the applications of the converters, and also they have a higher number of components in comparison with conventional topologies. Hence, the converters proposed herein show good performance for application in systems that require either step-up or step-down conversion, higher accuracy between the static gain versus duty cycle, reduced voltage stress on the components, and rated power up to 700 W. In addition, the notable features of the buck converter include the static gain, voltage stress, generalization and simplicity. These features make it suitable for high step-down converters, in which a high rate of conversion is required (e.g., in auxiliary power supplies and DC-DC distribution systems).

The results of the theoretical studies were corroborated in tests with a 1 kW prototype, which was used for the experimental verification of the three topologies proposed herein. For the buck topology, an efficiency of 95% was obtained at rated power. A comparison between the hybrid structures and conventional converters highlights the advantages and disadvantages of these structures in relation to the static gain, the voltage stress and the number of components.

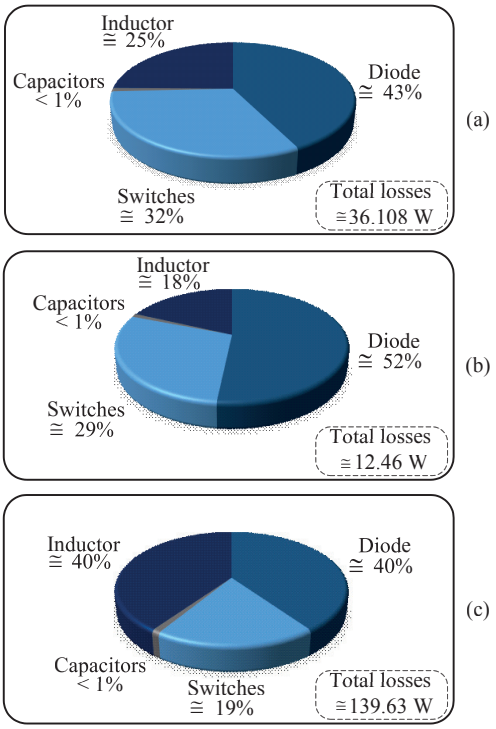


Fig. 16 –Theoretical distribution of losses at rated power (1kW): (a) buck topology, efficiency ≅ 96.51%; (b) boost topology, efficiency ≅ 98.77% and (c) buck-boost topology, efficiency ≅ 87.74%.

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