IMPACT OF COMMON MODE SIGNAL INJECTION ON THE LEAKAGE CURRENT OF A GRID-CONNECTED TRANSFORMERLESS PV INVERTER

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***Abstract* – Leakage current is one of the most relevant problems in grid-connected transformerless photovoltaic (PV) inverters due to parasitic capacitance of the PV modules. This problem is directly related to the common mode voltage generated by inverter modulation. Therefore, this paper presents an analysis of the impact of the common mode signal usually injected in carrier based modulation approaches, aiming the reduction of the leakage current in three-phase grid-connected transformerless PV inverter. The resulting leakage current is analyzed for an inverter topology with a modified LCL filter, which is utilized to attenuate the high frequency components of the voltage on the PV parasitic capacitance. Experimental results are given to evaluate the performance of a 10 kW transformerless PV inverter.**

***Keywords* – Geometric Approach, Leakage Current, Transformerless PV Inverter.**

I. INTRODUCTION

Transformerless photovoltaic (PV) systems have high efficiency, low cost and reduced size/weight due to the lack of galvanic isolation [1]–[3]. However, the leakage current circulation between the parasitic capacitances of the grounded PV arrays and the grid is a concern in these systems [4], [5]. This is mainly because the leakage current circulation results in electromagnetic interference, safety issues, waveform distortion of the grid currents and higher losses [6]. Consequently, there are safety requirements defined in some standards to protect against excessive leakage current values. The standards DIN VDE V 0-126-1-1 and IEC62109-2 require that the inverter must disconnect from the grid within a predefined time when a continuous residual current exceeds 300 mA_{rms} [7], [8].

It is well-known that the leakage current in three-phase grid connected inverters is directly related to the common mode voltage generated by inverter [9]. In this way, the techniques used for leakage current reduction can be classified according to topology modifications, modulation techniques and passive filters [10]. Several authors propose modified modulation techniques to change the behavior of the common mode voltage of the three-phase inverter [11]–[13]. However, these techniques penalize the inverter modulation index and may increase the switching losses and the magnetic core losses. Modified inverter topologies are also proposed to reduce the high frequency components of the voltage on the parasitic capacitance, such as the full-bridge three-phase zero voltage rectifier and the DCM-232 Converter [14], [15]. These topological modifications are made together with specific modulation strategies. Nevertheless, the increased number of components usually increases the complexity and cost as well as reduces the overall efficiency. In [16], a space vector modulation technique was proposed, using two medium vectors with an adaptive neutral point voltage to allow the inverter operation with unitary modulation index and constant common mode voltage. However, this technique requires the use of a bidirectional half-bridge dc-dc converter to generate the adaptive neutral point voltage, increasing the complexity of the converter.

On the other hand, modified LCL (MLCL) filter in the grid connection is a reliable and simple alternative for leakage current reduction [17], [18]. In the MLCL filter, the common point of the output filter capacitors is connected directly to the dc bus central point. This solution attenuates the high frequency components of the voltage on the PV parasitic capacitance, whereas maintaining the modulation index range. Additionally, the remaining low frequency components of the voltage on the parasitic capacitance can be reduced using an active control loop [10]. However, the leakage current reduction still depends on modulation strategy, since the voltage on the parasitic capacitance is affected by it.

To maximize the attainable output voltage amplitude of the inverter, carrier-based modulation based on geometric approach can be used [19], [20]. In this modulation technique, the inverter modulation signals are obtained from the definition of the desirable reference line voltages and using an adequate common mode signal. This common mode signal can be defined to reach some objective, such as harmonic distortion reduction or efficiency improvement. Furthermore, this modulation presents easy implementation provided by carrier-based modulation concept. Several works discuss the impact of the common mode signal on the neutral point voltage balancing, losses and waveform quality of multilevel inverters [21]–[25]. Nevertheless, so far, none addresses its impact on the leakage current of grid-connected transformerless PV inverters. Although the high-frequency components produced by commutations are usually the main concern from the leakage current point of view, the low frequency components of the common mode signal directly affects the leakage current since the MLCL filter is not able to reduce the low frequency harmonics. As a consequence, a careful analysis of the common mode signal choice is required. Therefore, this paper proposes a new analysis of the classical carrier-based modulation from the point of view of the leakage current of transformerless PV inverters. The resulting leakage current is analyzed in a three-phase three-level grid-connected transformerless PV inverter with a

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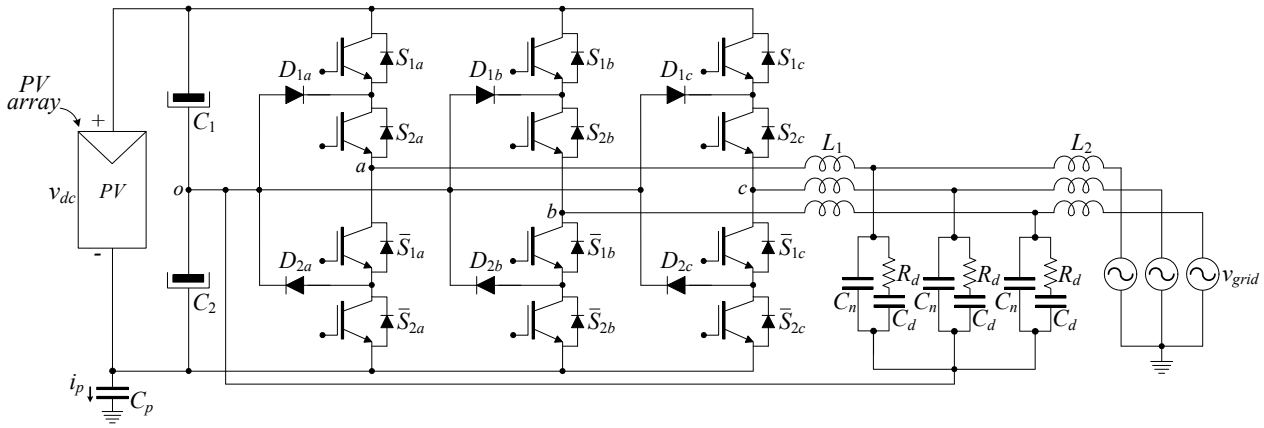

Fig. 1. Three-level inverter connected to the grid through an MLCL filter.

MLCL filter, by injecting distinct common mode signals in the modulation waveforms obtained from the geometric approach. The main purpose is to show the influence of these different modulation approaches on the leakage current, mainly on the low-frequency components, and to provide an additional requirement for the common mode choice besides the classical requirements.

The inverter topology and the modulation strategy are addressed in Section II to define some typical common mode signals. Section III presents the common mode circuit of the inverter and the relationship between the leakage current and the inverter common mode voltage. Experimental results are included to evaluate the performance of a 10 kW transformerless PV inverter with a MLCL filter in Section IV.

II. TOPOLOGY DESCRIPTION AND MODULATION

A schematic of a transformerless three-phase neutral point clamped (NPC) PV inverter is shown in Figure 1. The NPC topology generates up to five levels in the line-to-line voltages, improving the waveforms quality. Moreover, the semiconductors are submitted to a blocking voltage equal to half of the dc bus, allowing a high voltage in the PV array. The capacitor C_p was included at the negative terminal of the dc bus to model the parasitic capacitance of the PV system. The common point of the MLCL filter capacitors is connected directly to the dc bus central point, reducing the leakage current of the PV system [26]. This reduction can be explained by the fact that the capacitive branch of the MLCL filter offers a low impedance path for the high frequency leakage current components.

In this paper, a low-loss series RC passive damping branch is considered, as presented in Figure 1. This damping scheme maintains the high frequency attenuation of the filter even by increasing the damping resistance R_d [27]. The design of the damping resistance can be made based on grid current loop stability margin and leakage current requirements, since leakage current behavior is affected by the resistance value [28]. Additionally, the other filter parameters can be designed using classical techniques applied to the LCL filters [29].

The modulation technique adopted in this paper for the PV inverter shown in Figure 1 is the phase disposition pulsewidth modulation (PWM) based on geometric approach [18], [19]. In this technique, a transformation matrix is used to relate the modulation signals (v_{an}^*, v_{bn}^*, v_{cn}^*) with the reference line voltages (v_{ab}^*, v_{bc}^*):

$$\begin{bmatrix} v_{an}^*(t) \\ v_{bn}^*(t) \\ v_{cn}^*(t) \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & 1 & 1 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix}\begin{bmatrix} v_{ab}^*(t) \\ v_{bc}^*(t) \\ v_o(t) \end{bmatrix}. \quad (1)$$

Consequently, the modulating signals can be obtained from the definition of the reference line voltages and using an adequate common mode signal v_o. The definition of the common mode signal is a degree of freedom to determine v_{an}^*, v_{bn}^* and v_{cn}^*. Generally, v_o can be used to maximize the attainable output voltage amplitude of the converter in the linear operating region. However, it also affects other inverter quantities, such as neutral point voltage balance and losses [21].

Therefore, it is necessary to define some restrictions for v_o, obtaining its limits for the converter operation in the PWM linear region. In this sense, the modulating signals for phase x ($x = a, b, c$) must be in the interval $0 \le v_{xn}^* \le 1$. Applying this restriction to (1), the limits for v_o can be found:

$$v_{o,\min}(t) \le v_o(t) \le v_{o,\max}(t) \quad (2)$$

where, as demonstrated in Appendix:

$$\begin{cases} v_{o,\min}(t) = \max\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right) \\ v_{o,\max}(t) = 3 + \min\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right) \end{cases}. \quad (3)$$

From (2), the set of all possible v_o values are defined to ensure the inverter operation in the linear region [30]. To simplify the choice of v_o, the variable α can be defined as a linear combination of $v_{o,\min}$ and $v_{o,\max}$:

$$v_o(t) = \alpha(t)\, v_{o,\min}(t) + (1 - \alpha(t))\, v_{o,\max}(t) \quad (4)$$

where $0 \le \alpha(t) \le 1$. From definition of $\alpha(t)$ is possible to use a common mode signal that is within the range defined in (2). Furthermore, $\alpha(t)$ is also related to the distribution ratio

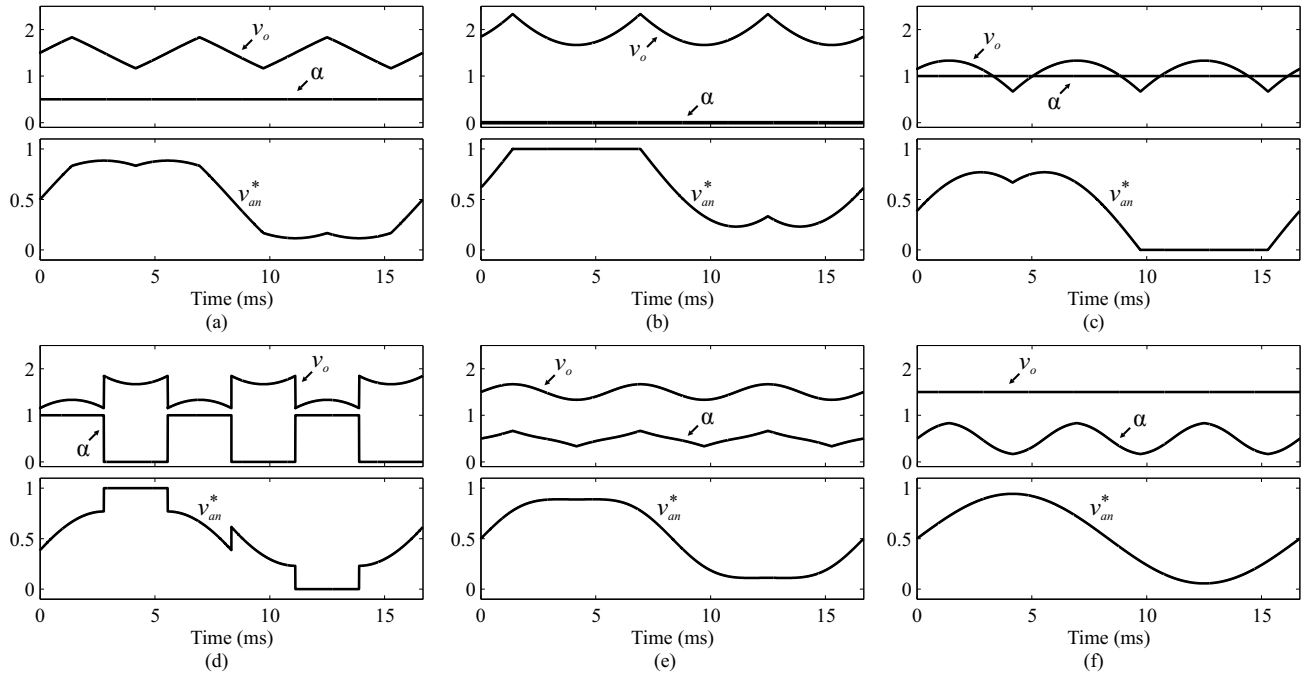

Fig. 2. Common mode signal choice. (a) $\alpha(t) = 0.5$. (b) $\alpha(t) = 0$. (c) $\alpha(t) = 1$. (d) DPWM1. (e) Sinusoidal v_o. (f) Constant v_o.

TABLE I
Common Mode Functions

α function	v_o function	Fig.
$\alpha(t) = 0.5$	$v_o(t) = \frac{v_{o,\min}(t) + v_{o,\max}(t)}{2}$	2(a)
$\alpha(t) = 0$	$v_o(t) = v_{o,\max}(t)$	2(b)
$\alpha(t) = 1$	$v_o(t) = v_{o,\min}(t)$	2(c)
$\alpha(t) = \begin{cases} 1, & 0 \le t_1 < \frac{T_1}{6} \\ 0, & \frac{T_1}{6} \le t_1 < \frac{T_1}{3} \end{cases}$, $T_1 = 16.67$ ms	$v_o(t) = \begin{cases} v_{o,\min}(t), & 0 \le t_1 < \frac{T_1}{6} \\ v_{o,\max}(t), & \frac{T_1}{6} \le t_1 < \frac{T_1}{3} \end{cases}$	2(d)
$\alpha(t) = \frac{\frac{\sqrt{3}}{6} m_a \sin(3\omega t) + 1.5 - v_{o,\max}(t)}{v_{o,\min}(t) - v_{o,\max}(t)}$	$v_o(t) = \frac{\sqrt{3}}{6} m_a \sin(3\omega t) + 1.5$	2(e)
$\alpha(t) = \frac{1.5 - v_{o,\max}(t)}{v_{o,\min}(t) - v_{o,\max}(t)}$	$v_o(t) = 1.5$	2(f)

of the redundant states during a switching period for the NPC inverter [21], [31]. For example, the three-level NPC inverter has six small vectors where each one has two redundant states that generate the same line-to-line voltages. The use of $\alpha(t) = 0.5$ results in the conventional space vector PWM, where the time application of each redundant state during a switching period is the same. Similarly, the use of $\alpha(t) = 0$ or $\alpha(t) = 1$ implies that only one redundant state is used during a switching period over all fundamental cycle.

A typical choice for $\alpha(t)$ is a constant value, such as $\alpha(t) = 0.5$, as shown in Figure 2(a). However, there are distinct possibilities for $\alpha(t)$, as depicted in Figure 2 and in Table I. By using $\alpha(t) = 0$ (Figure 2(b)) or $\alpha(t) = 1$ (Figure 2(c)) the modulating signals remain clamped on one or zero, respectively, during 120º at each fundamental period, resulting in discontinuous modulation [21]. Nevertheless, these solutions cause voltage imbalance in the dc bus capacitors of the NPC inverter, since a dc current level is generated in the central point. Similarly, other discontinuous modulation is the called DPWM1 (Discontinuous PWM 1), which is achieved by alternating the value of $\alpha(t)$ between zero and one at each 60º, as shown in Figure 2(d). Other variations of this modulation, as DPWM2, DPWM3 and DPWM4 can be obtained by shifting the phase of the $\alpha(t)$ square waveform [31]. These discontinuous solutions can be used to reduce the number of commutations, improving the converter efficiency. A proper choice for $\alpha(t)$ can also result in a sinusoidal or a constant common mode signal, as presented in Figure 2(e) and Figure 2(f), respectively. However, for a constant common mode signal the maximum value of the output line voltages generated by inverter is only 86.6% of the total dc bus voltage. The sinusoidal v_o adopted in this situation was obtained similarly to the technique where an one-sixth of third harmonic is added to the modulating waveform [32].

The impact of $\alpha(t)$ in the switching losses and waveform quality is addressed in several papers [22]–[25]. The harmonic distortion factor (HDF) can be used to compare the waveform quality for different modulation strategies [23]–[25]. As expected, the DPWM1 presents an inferior performance (highest HDF) with relation to the continuous solutions ($\alpha(t) = 0.5$, constant v_o, and sinusoidal v_o) for all range of modulation index and considering the same switching frequency [24], [25]. The cases $\alpha(t) = 0.5$ and sinusoidal v_o present a similar behavior in terms of HDF. Although the constant v_o presents better performance than DPWM1, its HDF is higher than the HDF of $\alpha(t) = 0.5$ and sinusoidal v_o. Considering the switching losses, they are significantly influenced by the load power factor for DPWM1. If the output current during the clamping intervals reaches the maximum values in module (unitary power factor), the switching losses are minimized. In this case, the switching losses are reduced by half for DPWM1 in relation

to the continuous modulations considering unitary power factor [23]. Even for zero power factor the DPWM1 represents a reduction of 13.4% in the switching losses in relation to the continuous modulations [23].

III. IMPACT OF THE COMMON MODE SIGNAL ON THE LEAKAGE CURRENT

Figure 3 presents the common mode equivalent circuit of the inverter with MLCL filter, where i_p is the leakage current of the PV system. This model considers that inductances and capacitances of the output filter are equal for all phases and the dc bus capacitors (C_1 and C_2) are replaced by two equivalent constant voltage sources $v_{dc}/2$. In addition, the grid voltages are considered sinusoidal and balanced, so that they do not contribute to the leakage current. The grounding impedance and the resistance of the filter elements were not included in this case, representing the worst case from the point of view of leakage current magnitude. The source v_{cmv} is called common mode voltage, which is usually defined as:

$$v_{cmv}(t) = \frac{v_{an}(t) + v_{bn}(t) + v_{cn}(t)}{3}. \tag{5}$$

The leg-voltages v_{an}, v_{bn} and v_{cn} are generated by comparing the modulating signals v_{an}^*, v_{bn}^* and v_{cn}^* with the phase disposition triangular carries. Consequently, the source v_{cmv} includes both high switching frequency components and low frequency components due to the common mode signal v_o. In other words, from (1) and (5), the relationship between v_{cmv} and v_o, considering the average values in a switching period T_s, is given by:

$$\left\langle v_{cmv}(t) \right\rangle_{T_s} = \frac{v_o(t)}{3}. \tag{6}$$

One can observe from Figure 3 that the leakage current generation is directly related to the frequency and amplitude of the voltage source v_{cmv}. Thus, the resulting leakage current spectrum is obtained from the common mode voltage and the common mode circuit transfer function G_{cm}, such as:

$$i_p(s) = v_{cmv}(s) G_{cm}(s) \tag{7}$$

where G_{cm} is given by:

$$G_{cm}(s) = \frac{sC_p(sC_dR_d + 1)}{s^5k_5 + s^4k_4 + s^3k_3 + s^2k_2 + sk_1 + 1} \tag{8}$$

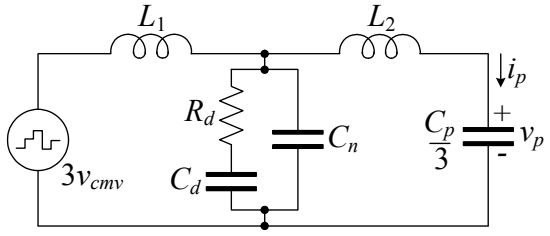

Fig. 3. Commom mode equivalent circuit.

and the coefficients k_1 to k_5 are:

$$\begin{aligned}
k_1 &= C_dR_d \\
k_2 &= L_1\left(C_d + C_n + \frac{C_p}{3}\right) + L_2\frac{C_p}{3} \\
k_3 &= C_dR_d\left(C_nL_1 + \frac{C_p(L_1 + L_2)}{3}\right) \\
k_4 &= C_pL_1L_2\left(\frac{C_d + C_n}{3}\right) \\
k_5 &= \frac{C_dC_pC_nL_1L_2R_d}{3}.
\end{aligned} \tag{9}$$

From (6), note that resulting low frequency components of the common mode voltage synthetized by the inverter are directly proportional to the common mode signal defined in the geometric approach. As a consequence, low frequency components of the leakage current will depend on choice of the common mode signal. Moreover, only the high frequency portion of the leakage current is filtered by the capacitive branch (composed of C_n and C_d) of the MLCL filter.

Figure 4 shows the low frequency spectrum of the v_{cmv} ($h \leq 27$), considering different solutions and $v_{dc} = 700$ V, where h is the harmonic order related to the fundamental frequency. As expected, the resulting low frequency components of the DPWM1 are high due to the $\alpha(t)$ square waveform. The low frequency content is gradually reduced for $\alpha(t) = 0.5$ and for sinusoidal v_o. In an ideal case, none low frequency leakage current is generated using a constant v_o. To better illustrate this fact, Figure 5 shows the contribution of the low frequency components of v_{cmv} ($h \leq 27$) in the leakage current. In this case, a total parasitic capacitance $C_p = 1.25$ µF has been considered as a typical value for crystalline silicon PV modules [6]. The other parameters employed are shown in Table II. One can observe that the low frequency current is responsible for 6% to 25% of the total leakage current for a sinusoidal v_o and 24% to 68% for $\alpha(t) = 0.5$, according to the dc bus voltage level. For the DPWM1 this percentage comes near to 98% for high dc bus

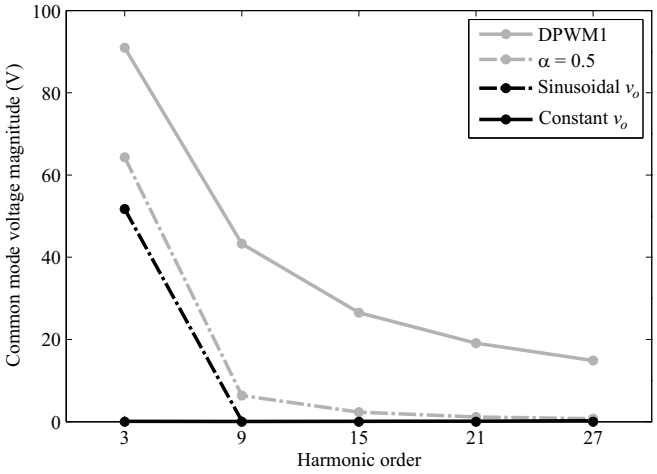

Fig. 4. Magnitude of the low frequency components of v_{cmv} for $v_{dc} = 700$ V.

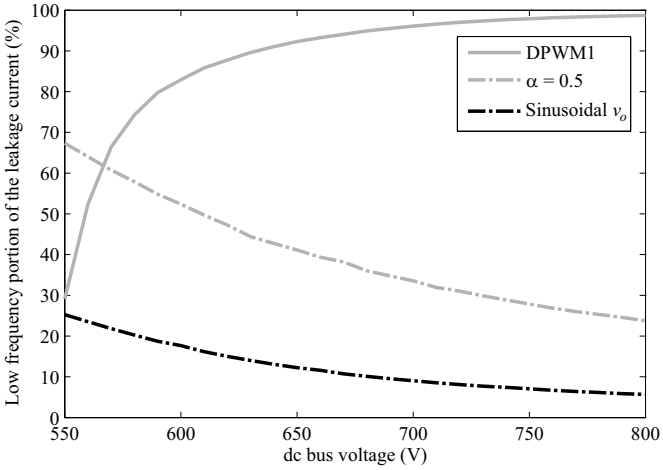

Fig. 5. Contribution of the low frequency components in the total leakage current.

TABLE II
Inverter and Filter Parameters

Parameter	Value
Power	10 kW
Grid voltage/frequency	380 V/60 Hz
Switching frequency f_s	7.68 kHz
Inductor L_1	1100 µH
Inductor L_2	200 µH
Capacitor C_n	10 µF
Capacitor C_d	15 µF
Resistance R_d	1 Ω

voltage levels. These theoretical results show that a significantly portion of the leakage current is composed of low frequency components. This occurs because the common mode signal v_o inserts low frequency components in the source v_{cmv} and the common mode circuit transfer function G_{cm} is not able to attenuate it.

It is also important to highlight that the common mode circuit of Figure 3 is a fifth order system, and its frequency response has two resonance peaks. Neglecting the influence of the damping resistance, the first resonance frequency can be defined as essentially dependent on L_1, C_d and C_n, and it is given by (in Hertz):

$$f_1 = \frac{1}{2\pi\sqrt{L_1\left(C_d + C_n\right)}}. \tag{10}$$

Similarly, neglecting the influence of the damping resistance, the second resonance peak depends on inductance L_2 and parasitic capacitance C_p, and it can be approximated as (in Hertz):

$$f_2 = \frac{1}{2\pi\sqrt{\frac{L_2}{3}C_p}}. \tag{11}$$

Since $(C_d + C_n) >> C_p$, the first resonance peak is located at lower frequency than second one. This behavior is shown in Figure 6, which shows the gain frequency response of the transfer function G_{cm}, considering the parameters of Table II.

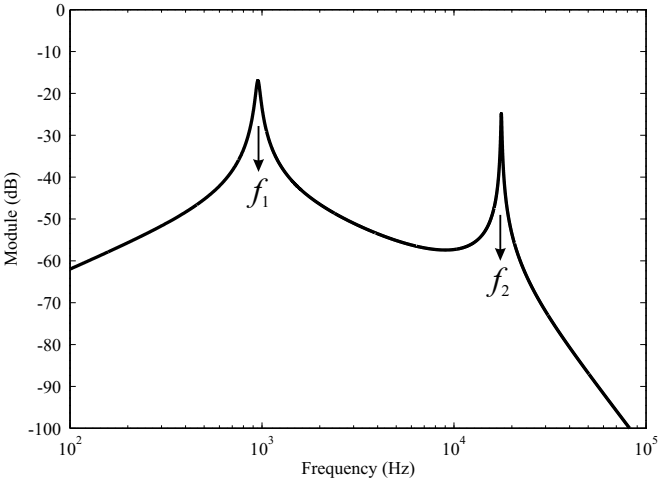

Fig. 6. Gain frequency response of G_{cm}.

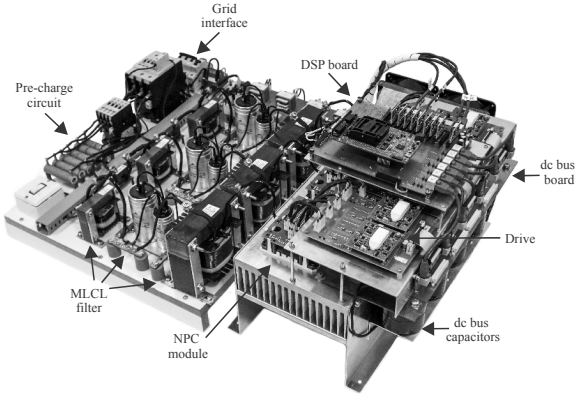

Fig. 7. Prototype of the PV inverter.

Note that f_2 can change substantially in practice, since parasitic capacitance is an uncertain quantity. If the value of the parasitic capacitance becomes high, the switching frequency components of v_{cmv} can excite the resonance in f_2, resulting in high leakage current. In this situation, the inverter must disconnect from the grid within the time intervals defined in the applicable standards if the leakage current exceeds the permissible limit [7], [8]. Moreover, care should be taken to avoid resonance excitation of f_1 due to low frequencies included in v_{cmv}. As mentioned, these low frequencies are resulting from the common mode signal v_o injected in the modulating signals. Thus, the frequency f_1 should be designed to avoid a match with these low frequency components. Nevertheless, the design of the MLCL filter is out of scope of this paper.

IV. RESULTS

Experimental results were obtained considering the parameters presented in Table II. The prototype picture of the 10 kW PV inverter is shown in Figure 7 and the block diagram of the control system in Figure 8. To obtain the experimental results, the PV system was emulated with a dc controlled source and a polypropylene capacitor was used for the parasitic capacitance. The control system consists in a classical digital PI (Proportional-Integral) based-control implemented in a synchronous reference frame (*dq*) for the grid current control. The solutions with $\alpha(t) = 0$ or $\alpha(t) = 1$

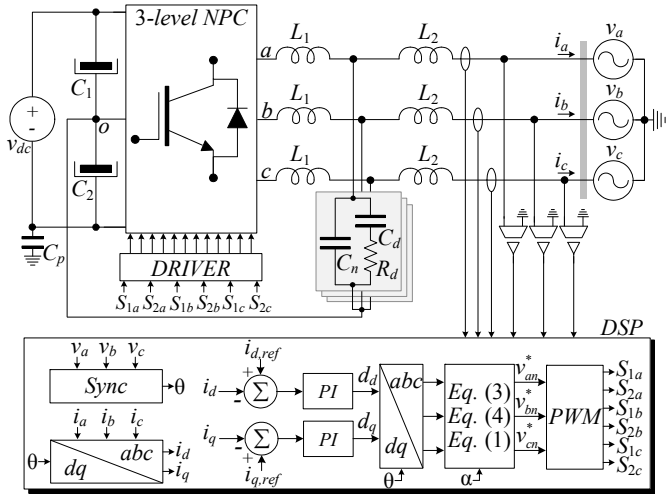

Fig. 8. Block diagram of the inverter control system.

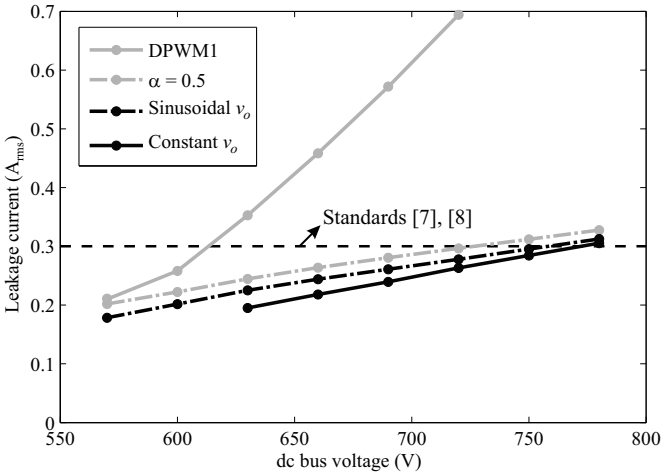

Fig. 9. Experimental rms leakage current for different solutions.

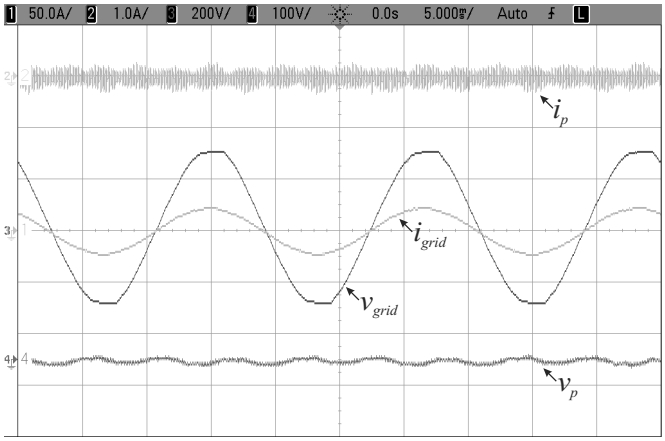

Fig. 10. Experimental result for constant v_o using v_{dc} = 700 V.

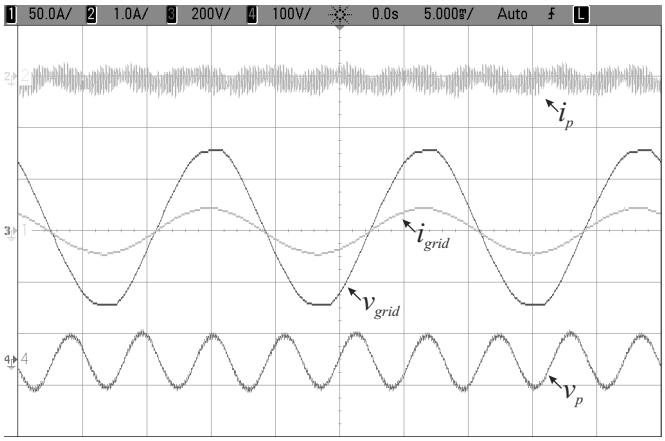

Fig. 11. Experimental result for sinusoidal v_o using v_{dc} = 700 V.

were not tested in practice, since the balance of the dc bus capacitor voltages is not feasible.

Figure 9 presents the experimental rms leakage current behavior for distinct dc bus voltage levels and different solutions for v_o. Note that the leakage current is high for DPWM1 modulation and remains above the standard limit for $v_{dc} > 610$ V. This is caused by $\alpha(t)$ square waveform, which produces a resonance excitation due to low frequencies components presented in v_o. Due to their similar characteristics, one can conclude that DPWM2, DPWM3 and DPWM4 result in similar behavior for the leakage current.

The smallest leakage current levels were obtained employing a constant v_o, since none low frequency component is injected with this solution. On the other hand, a constant v_o limits the voltage synthesis capability of the inverter, and this solution cannot be used for $v_{dc} < 620$ V. In this case, the sinusoidal v_o can be used for $v_{dc} < 620$ V, since the leakage current is smaller than other solutions. In addition, the curve for sinusoidal v_o is also lower than the curve for $\alpha(t) = 0.5$. For higher values of the dc bus voltage ($v_{dc} > 760$ V), the leakage current is above the standard limit independent of v_o waveform. In this situation, the inverter must be disconnected from the grid for safety reasons. Another possibility is to redesign the MLCL filter to reduce the high frequency leakage current or to employ active methods to reduce the low frequency components [10], [28].

To illustrate this analysis, some waveforms are included for a dc bus voltage equal to 700 V. Figure 10 shows experimental waveforms for leakage current (i_p), grid voltage (v_{grid}), grid current (i_{grid}) and voltage on the parasitic capacitance (v_p) considering a constant v_o. The rms leakage current obtained in this case was 247.3 mA, which complies with standards. Some low frequency ripple is still verified in the v_p due to the imbalance in the grid voltages. If a sinusoidal v_o is used, the leakage current tends to be higher for this dc bus voltage level. This can be confirmed through the results presented in Figure 11, where a rms leakage current equal to 268.3 mA was obtained. On the other hand, considering $\alpha(t) = 0.5$, the leakage current level is higher than the previous cases, resulting in a leakage current equal to 287.6 mA, as demonstrated in Figure 12. Finally, experimental result for DPWM1 is shown in Figure 13. As expected, a dangerous leakage current equal to 622 mA was verified.

V. CONCLUSIONS

This paper presented an analysis about the impact of the common mode signal choice on the leakage current of a three-phase three-level grid-connected transformerless PV inverter using a MLCL filter. The MLCL filter offers a low impedance

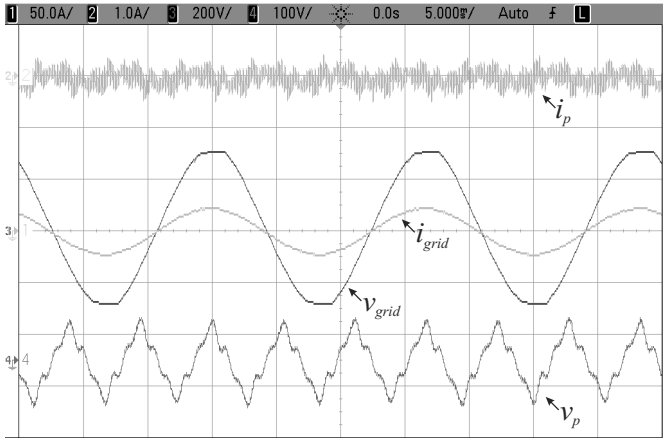

Fig. 12. Experimental result for $\alpha(t) = 0.5$ using $v_{dc} = 700$ V.

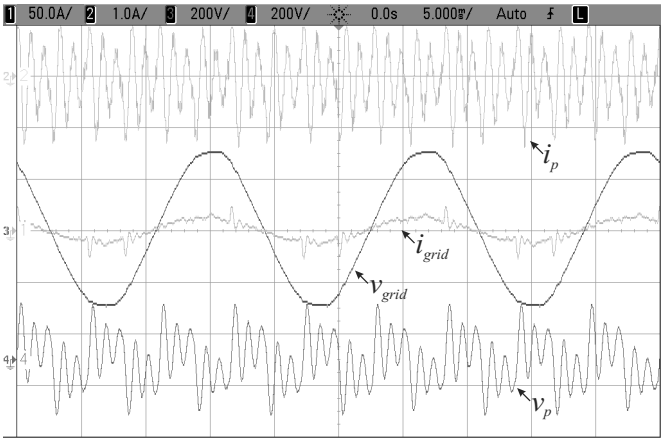

Fig. 13. Experimental result for DPWM1 using $v_{dc} = 700$ V.

path for high frequency leakage current components, reducing its circulation to the grid. On the other hand, a low frequency leakage current is generated from the use of the common mode signal in the modulation signals. Therefore, the leakage current levels were analyzed for typical common mode signals employed in the modulation using geometric approach. It was verified that these low frequency components are responsible for a significant portion of the total leakage current. From the analysis, one can conclude that the degree of freedom represented by common mode signal can be adjusted based on leakage current level in addition to other classical requirements. Furthermore, it was shown that the solution adopted for v_o in geometric approach is critical and the leakage current can be optimized according to PV array voltage level.

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APPENDIX

This section was included to clarify the achievement of expression (3), which defines the limits for $v_o(t)$ in the linear region. As explained previously, the modulating signal of each phase must be in the interval $0 \le v_{xn}^* \le 1$ for operation in the linear region. Applying this restriction to (1) results in:

$$0 \le \frac{1}{3}\begin{bmatrix} 2 & 1 & 1 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix}\begin{bmatrix} v_{ab}^*(t) \\ v_{bc}^*(t) \\ v_o(t) \end{bmatrix} \le 1. \quad (12)$$

Considering the lower limit ($0 \le v_{xn}^*$) in (12), the following expressions can be obtained:

$$\begin{cases} 0 \le \frac{2}{3}v_{ab}^*(t) + \frac{1}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \\ 0 \le -\frac{1}{3}v_{ab}^*(t) + \frac{1}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \\ 0 \le -\frac{1}{3}v_{ab}^*(t) - \frac{2}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \end{cases}. \quad (13)$$

Isolating $v_o(t)$ in (13):

$$\begin{cases} v_o(t) \ge -2v_{ab}^*(t) - v_{bc}^*(t) \\ v_o(t) \ge v_{ab}^*(t) - v_{bc}^*(t) \\ v_o(t) \ge v_{ab}^*(t) + 2v_{bc}^*(t) \end{cases}. \quad (14)$$

Since all restrictions described in (14) must be respected, $v_o(t)$ must be equal or greater than the maximum instantaneous value among all sentences:

$$v_o(t) \ge \max\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right). \quad (15)$$

Consequently, since $v_o(t)$ must satisfy (15), the minimum value of $v_o(t)$ is given by:

$$v_{o,\min}(t) = \max\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right). \quad (16)$$

Similarly, considering the upper limit ($v_{xn}^* \le 1$) in (12), the following conditions are obtained:

$$\begin{cases} \frac{2}{3}v_{ab}^*(t) + \frac{1}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \le 1 \\ -\frac{1}{3}v_{ab}^*(t) + \frac{1}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \le 1 \\ -\frac{1}{3}v_{ab}^*(t) - \frac{2}{3}v_{bc}^*(t) + \frac{1}{3}v_o(t) \le 1 \end{cases}. \quad (17)$$

Again, isolating $v_o(t)$ in (17):

$$\begin{cases} v_o(t) \le -2v_{ab}^*(t) - v_{bc}^*(t) + 3 \\ v_o(t) \le v_{ab}^*(t) - v_{bc}^*(t) + 3 \\ v_o(t) \le v_{ab}^*(t) + 2v_{bc}^*(t) + 3 \end{cases}. \quad (18)$$

Since all restrictions shown in (18) must be respected, $v_o(t)$ must be equal or lower than the minimum instantaneous value among all sentences:

$$v_o(t) \le 3 + \min\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right). \quad (19)$$

Consequently, since $v_o(t)$ must satisfy (19), the maximum value of $v_o(t)$ is given by:

$$v_{o,\max}(t) = 3 + \min\left(-2v_{ab}^* - v_{bc}^*, v_{ab}^* - v_{bc}^*, v_{ab}^* + 2v_{bc}^*\right). \quad (20)$$

From (16) and (20) the limits for $v_o(t)$ are established:

$$v_{o,\min}(t) \le v_o(t) \le v_{o,\max}(t). \quad (21)$$

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