THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER FED BY A PHOTOVOLTAIC SYSTEM UNDER PARTIAL SHADING

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***Abstract* – This paper deals with a system composed of a three-level Neutral-Point-Clamped inverter fed by photovoltaic panels. The system is able to operate adequately even under partial shading operation by controlling the dc-link neutral point injected current. System model, pulse width modulation strategy, maximum power point tracking, and control logic for balancing the dc-link capacitors voltages are presented. Analysis of harmonic distortion, thermal stress, limits of control, and power losses are included. Experimental results validate the proposed system.**

***Keywords* – NPC Inverter, Partial Shading, Photovoltaic System, Unbalanced DC-link.**

I. INTRODUCTION

The energy generation from renewable sources has drastically increased in recent years and a larger expansion is expected in the future. Nowadays, the photovoltaic (PV) power generation is very desirable since it demands low maintenance, the system can be adapted to either distributed or centralized generation and the sun is available most part of the year.

Different topologies have been conceived for handling photovoltaic energy generation. Their choice depends on different criteria such as the number of available PV panels, output signal quality (voltage and current), system efficiency, and managing complexity [1]-[4]. In one of the possible solutions, two power conversion stages are provided, each one using one dc-to-dc boost converter between the PV module and the dc-bus. Since multilevel inverters can handle higher voltages this scheme becomes attractive because the boost converter can be used not only for boosting the voltage but also for obtaining the maximum power point tracking (MPPT) [5].

Even though there are many advantages in the use of a photovoltaic system, challenges such as shadow influence and ac-side power quality continue to defy researchers [6]. Shading effects can be attenuated through photovoltaic generator configuration, system architecture, use of inverter topologies, and system modulation.

One problem with the tree-level Neutral-Point-Clamped (NPC) topology is the natural unbalance of their dc-link capacitor voltages [7], [8]. As a consequence, when the PV output voltage is stable, the use of the NPC inverter is attractive [9], [10]. However, when there is partial shading the capacitor voltage balance is not anymore guaranteed and provokes loss of quality in the output signals [1]. A dc-link control to overcome that problem was introduced in [11]. In that paper, the system model, the pulsewidth modulation (PWM) strategy and the control strategy have been studied.

This paper evaluates the capacitors balance in the same stand alone system as in [11] operating under partial shading. Harmonic distortion (THD, WTHD), thermal stress, power losses, inclusive the dc-link high-frequency power losses, are compared for the panel with and without shading. The limits of control under shading are also investigated. The validity of the proposed system is confirmed by simulation and experimental results. Although not considered the main focus of the paper, comments on the grid connected three-level NPC inverter are given.

II. PROPOSED SYSTEM

The proposed system is constituted of two PV panels, two boost converters and a three-level NPC inverter, as shown in Figure 1. The boost converters are used with the objective of both extracting the maximum power from the PV panel and feeding the NPC inverter at a wished dc-link voltage level. The NPC inverter output is connected to a RL load. The capacitors voltage control is obtained with the help of the modulation strategy.

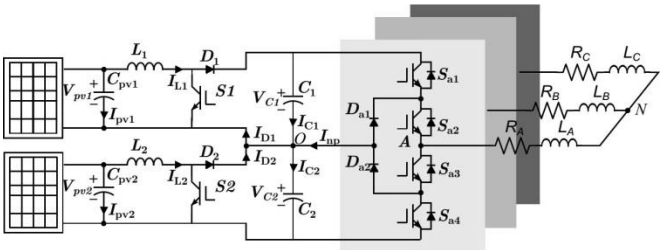

Fig. 1. Proposed scheme with two power stages.

A. System Modelling

Figure 2 presents the equivalent circuit for the proposed system. The *NPC* inverter switches S_{j1}, S_{j2}, S_{j3}, and S_{j4} are represented by the switching states q_{j1}, q_{j2}, q_{j3} and q_{j4}, respectively. The switching states q_{j3} and q_{j1} are complementary and so are q_{j4} and q_{j2}. Switches S_1 and S_2 of the boost converters are represented by the switching states $q_1$and q_2, respectively.

Manuscript received 19/03/2016; first revision 07/05/2016; accepted for publication 04/07/2016, by recommendation of Editor Marcelo Cabral Cavalcanti.

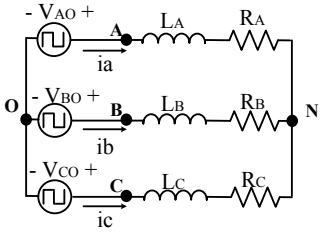

Fig. 2. Equivalent circuit.

The load is star-connected so that the inverter model is given by:

$$v_{jo} - R_1 i_j - L_1 \frac{di_j}{dt} - v_{on} = 0 \qquad (1)$$

where j = a, b, c. In case the load is balanced, voltage v_{on} is given by:

$$v_{on} = \frac{(v_{ao} + v_{bo} + v_{co})}{3}. \qquad (2)$$

The pole voltages, v_{jo}, can be defined as functions of the switching states, that is,

$$v_{jo} = (q_{j1} + q_{j2} - 1)(v_{c1} + v_{c2})/2. \qquad (3)$$

Figure 3 presents the modes of operation of the boost dc converter fed by the PV voltage V_{pvk}.

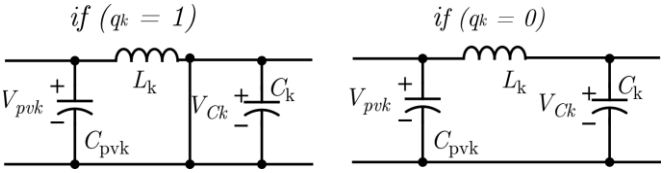

Fig. 3. Boost converter: modes of operation.

From that figure, the dc-bus capacitor voltages can be written, as a function of the panels voltages:

$$v_{ck} = (1 - q_k)\left(v_{pvk} - L_k \frac{di_{Lk}}{dt}\right) \qquad (4)$$

where:

k = 1, 2;

v_{pvk} - panel voltage;

i_{Lk} - current flowing in the boost converter inductor;

L_k - boost converter inductors.

B. MPPT Control

The *PV* voltage, V_{pvk}, is determined by the boost converter switching state, that is,

when $q_k = 1$, $v_{pvk} = L_k \dfrac{di_{Lk}}{dt}$

when $q_k = 0$, $v_{pvk} = L_k \dfrac{di_{Lk}}{dt} + v_{ck}$.

Then,

$$\frac{di_{Lk}}{dt} = \frac{v_{pvk}}{L_k}, \text{ for } q_k = 1 \qquad (5)$$

$$\frac{di_{Lk}}{dt} = \frac{v_{pvk} - v_{ck}}{L_k} \text{ for } q_k = 0. \qquad (6)$$

From (5) and considering that v_{pvk} is always positive, there is always a current increment since $di_{Lk}/dt > 0$. On the other hand, from (6) there is a decrement since $di_{Lk}/dt < 0$. This way, the inductor current is used to control the voltage v_{pvk}. The voltage reference for extracting the maximum power from the PV panels comes from the MPPT algorithm.

A complete control scheme for the boost converter is shown in Figure 4. For the MPPT, it is used the method of incremental conductance that results in the panel reference voltage.

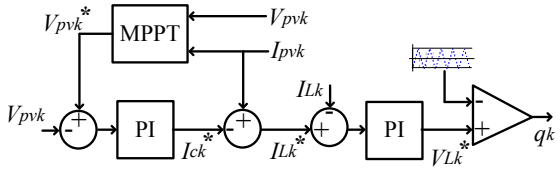

Fig. 4. MPPT control.

The PV voltage error is measured and controlled with the help of a PI controller. One can note that the PV output capacitor voltage can be controlled through current i_{ck}. That means that the PI controller output is the current reference i_{ck}*. The inductor current reference can be found by using the Kirchhoff's Law, that is, $i_{Lk*} = i_{pvk} - i_{ck}$*. Finally, the inductor current error is applied to a second PI controller of which the output is the PWM reference voltage.

C. PWM Strategy and Dc-Link Control

Figure 5 shows the control diagram for the PWM approach proposed which is used to control the dc-link voltage and to balance in the capacitors in order to have v_{C1}=v_{C2}.

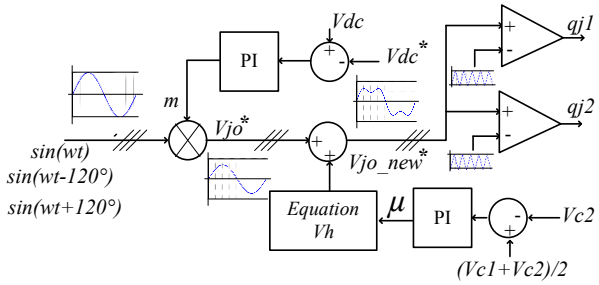

Fig. 5. DC-link control.

The dc-link voltage (V_{dc}) level control is obtained by regulation of the amplitude index m through *PI*. m is the ratio between modulating signal and the carrier amplitude and determines the current value to be injected in the dc-link so that its required level is maintained. Multiplication of m by the three unitary sinusoidal signals phase-shifted of 120 degrees results in the three reference voltages v_{ao}*, v_{bo}* and v_{co}*. With the objective of balancing the voltages of the

individual capacitors, a zero-sequence signal v_h is added to the three reference voltages. The zero sequence signal is defined in [12], so that

$$v_h = (1-2\mu)\frac{V_{DC}}{2} + \mu v_{\max} + (1-\mu)v_{\min}, \qquad (7)$$

where:

v_{max}=V_{dc}/2 – max(v_{ao}*, v_{bo}*, v_{co}*);
v_{min}= - V_{dc}/2 – min(v_{ao}*, v_{bo}*, v_{co}*);
μ is the distribution ratio.

The distribution ratio μ establishes the ratio between the duration of application of the vectors applied at the extremities of the modulation period. In three-level inverters these vectors can be either zero vectors or small vectors [12], [13]. The distribution ratio is employed to control the dc-bus voltages balance [11], [14]. The new reference voltages then become $v_{jo\_new}^* = v_{jo}^* + v_h$ that are compared with the two triangle carriers of the carrier-based PWM Level-Shift [15] technique. This defines the NPC inverter switching signals.

III. CAPACITOR VOLTAGE UNBALANCE CONTROL

In the NPC structure, the control of μ allows for making zero the average of the current flowing in and out of the central point. With that the voltages of the dc-link capacitor can be made equal [8].

In the scheme proposed in this paper, the two boost converters output currents, i_{D1} and i_{D2}, together with current i_{np} flow in and out of the central point. Therefore,

$$i_{C1} = i_{C2} + (i_{D1} - i_{D2}) - i_{np}. \qquad (8)$$

From (7) i_{C1} = i_{C2} when i_{D1} =i_{D2} and i_{np} =0. When both panels are identical and are submitted to same irradiation, then the first condition is satisfied. The value of μ is made 0.5 to satisfy the second condition. This seems to be a good solution. One of the investigations that deal with the voltage balancing across the dc-link capacitors of the NPC is reported in [2]. Authors use a similar technique to that proposed here in the sense they introduce a zero sequence signal which corresponds to μ = 0.5, but do not consider shading occurrence. Under shading condition i_{D1} is different from i_{D2}, provoking the dc-link unbalance. This problem can be overcome when μ is adjusted so that $i_{D2} - i_{D1} + i_{np} = 0$.

IV.SIMULATION RESULTS

Simulation results have been obtained with the help of MATLAB and PSIM programs. Table I presents the data used in the simulation.

Each panel module has 36 photovoltaic cells with fixed temperature of 25°C.

A. Open- Loop Analysis

Figure 6 shows the current, the voltage and the solar panel power, respectively. It is show that for $t < 0.95$, when the identical panels are submitted to an irradiation of 1000W/m^2, current, voltage and power do not change. That is, each PV panel provides the same power quantity.

TABLE I
System Parameters Used in the Simulation

Parameter	Symbol	Value
Boost Indutor	L_k	3 mH
PV Capacitor	C_{pvk}	1,100 μF
Boost Capacitor	C_k	2,200 μF
Boost Carrier Frequeny	f_b	10 kHz
Load Inductor	L_o	7 mH
Load Resistance	R_o	50 Ω
Dc-Link Voltage	V_{dc}	120 V
Carrier Frequency	f_s	10 kHz

In order to emulate partial shading, at instant $t = 0.92$ the irradiation of the second panel, PV_2, is changed to 900W/m^2. Since the MPPT control is independent for each panel, tracking the maximum power is guaranteed even under shading conditions, as shown in Figure 6(c). In that figure, P_{m1} and P_{m2} are the maximum power, and P_{O1} e P_{O2} are the instantaneous Power in panels *PV1* and *PV2*, respectively. It can be observed from Figure 6(b) that the voltage reference variation is not as significant as for the current.

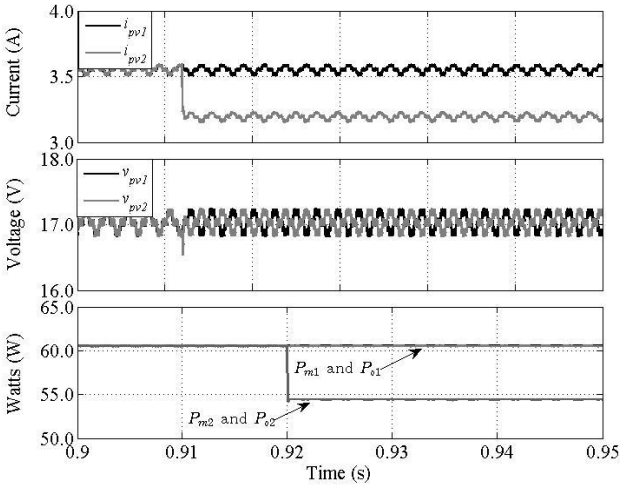

Fig. 6. PV's current, voltage and power.

Because this is an open loop operation, the current variation affects the operation point thus modifying the current in the diodes of the boost converters. Since currents i_{D1} and i_{D2} are unequal, i_{C1} differs from i_{C2}, with consequent unbalance of the capacitor voltages, as shown in Figure 7. To overcome this problem, a closed-loop control is introduced.

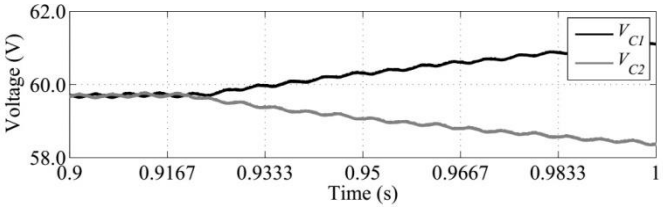

Fig. 7. Open-loop: output current and voltages V_{C1} and V_{C2}.

B. Closed-Loop Analysis

Figure 8 indicates the two control variables. From $t=0.95$ on, the modulation index reduces in order to adjust the lacking of current due to shadows. On the other hand, μ is not anymore regulated around 0.5 but around 0.75. The reason is that the value of μ is adjusted taking into account

the boost converters current error. This way, the voltage equilibrium in the capacitors is re-established, as shown in Figure 9. From that figure, one can see that the voltage error control is adequately controlled after the irradiation step.

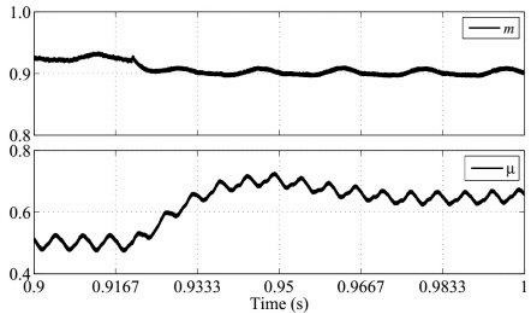

Fig. 8. Control variables: modulation index (m) and distribution ratio (μ).

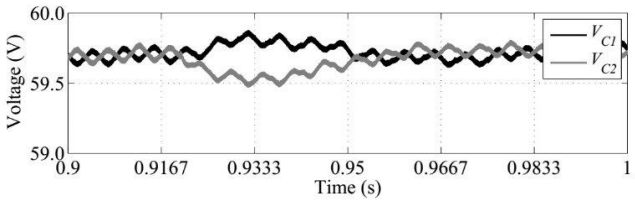

Fig. 9. Closed-loop: balance of the dc-link voltages, V_{C1} and V_{C2}.

C. Current THD and Voltage WTHD

Figure 10 presents the three-phase currents i_a, i_b and i_c, the pole voltage V_{ao}, and the line voltage V_{ab}. It is not visually possible to identify the shading influence in the system.

Since the control variables are directly associated to the power processing, it is necessary to analyze the impact of such control on the current THD and the voltage WTHD.

The variation of μ implies in a change of the switching

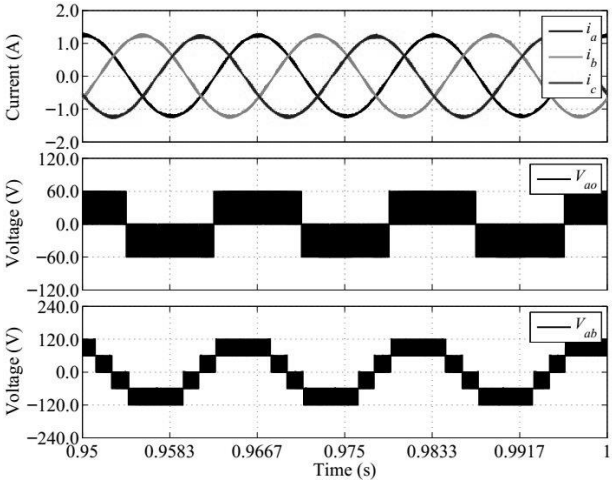

Fig. 10. Simulation results: Output current (top), pole voltage (middle) and line voltage (bottom).

pattern, since its value is directly associated to the time of application of the small vectors inside one switching period. Table II presents the current THD and voltage WTHD before and after shading.

TABLE II
Current THD and Voltage WTHD

Distortion	Situation	Value
Current THD	Without shading	1.89
	With shading	2.08
Voltage WTHD	Without shading	0.10
	With shading	0.13

D. Losses

Conduction and switching losses for both NPC inverter and boost converter as well as the boost converter inductor winding losses have been calculated. The switching and conduction losses have been calculated with the regression method introduced in [16]. The switches used in the experimental set-up have been modeled by using the PSIM9.0 "Thermal Module" tool in order to calculate the losses.

It has been shown that the behavior of both boost converters is similar when there is no shading. This is because both converters deliver the same power into the NPC inverter. When the panel that feeds the Boost converter 02 is under shading, there is a reduction in the power delivered by the panel, that is the current in Boost 01 is larger than that in Boost 02 causing this last one to produce losses there are smaller than Boost 01 [11].

Figure 11 compares the total losses for panels out of shading and under shading. Note that there are not significant changes in NPC and Boost 01. However, the difference between the two situations is of 0.95 W. Total losses without and with shading are 22.69 W and 21.73 W, respectively, what means a difference of de 0.96 W. Losses reduction basically occurs in the boost converter dealing with shading situation.

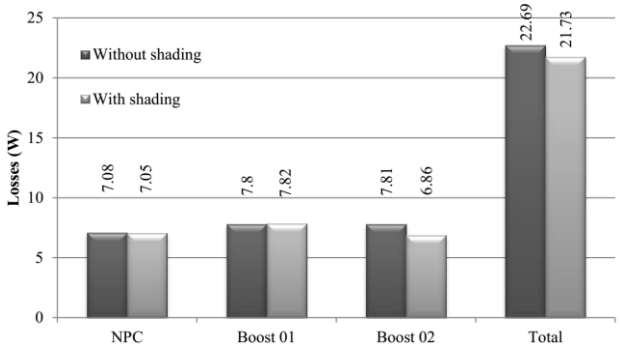

Fig. 11. Total losses for the NPC converter: Boost 01 and Boost 02.

E. Dc-Link High-Frequency Power Losses

A comparative study of dc-link power losses estimation will be done in the following. The dc-link high-frequency power loss is calculated by:

$$P_{loss}^{HO} = N(0.45)ESR_{(100Hz)}(I_{c(RMS)}^{HO})^2 \qquad (9)$$

where N is the number of capacitors used in dc-link, $I_{c(RMS)}^{HO}$ is the high-order component of root-mean-square (RMS) current on the dc-link (with h > 50), and $ESR_{(100Hz)}$ corresponds to the equivalent series resistance with frequency at 100 Hz. The ESR can be considered constant

for frequencies higher than 3 kHz. It has been chosen as equal to 0.45 times the ESR value for 100 Hz [17]. This means that P_{loss}^{HO} loss only depends on $I_{c(RMS)}^{HO}$.

Table III presents the RMS current normalized in relation to the RMS current without shading. Notice that the high-frequency dc-link RMS current, in the case of shading, presents a reduction of 6% when compared with the case in which there is no shading.

TABLE III
High-Frequency RMS Currents in the Dc-Link

Normalized RMS Current	Without shading	With shading
$I_{c(RMS)}^{HO}$ $/I_{c(RMS)}^{HO}(\boldsymbol{without\ shading})$	1.0	0.94

F. Thermal Stress

The thermal model for power switches indicates in thermal terms how the temperature energy loss is transferred toward different locals in the power semiconductors (junction, case, or heat-sink, for instance). Normally, the thermal behavior of a given material is represented by the thermal impedance, composed of thermal resistances (R_{th}) and thermal capacitances (C_{th}). The power switch total thermal impedance from the junction toward the ambient temperature can be modeled as a net of cascaded thermal impedances that represent each different material layer, as can be seen in Figure 12.

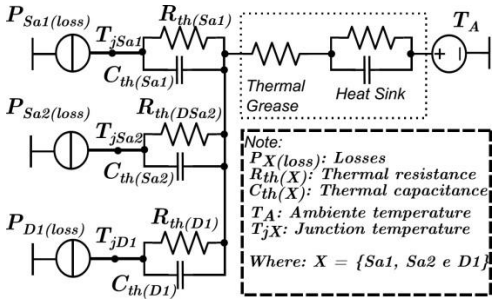

Fig. 12. Thermal Model

Figure 13 presents the junction temperatures for the active switches S_{a1} and S_{a2} and for the clamping diode D_{a1}. As it can be seen from that figure presents the maximum junction temperature for switch S_{a1}, switch S_{a2} and diode D_{a1} is 42.3°C, 42.05°C and 41.8°C, respectively. The use of the thermal model shows that partial shading does not affect the thermal behavior of the switches and diode.

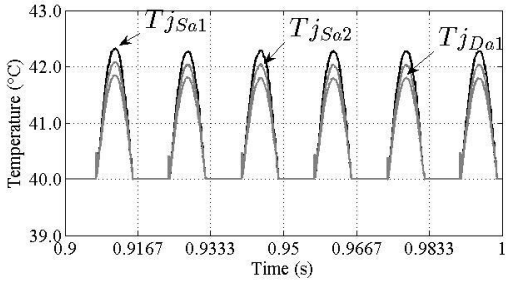

Fig. 13. Thermal stress on the different devices.

G. Shading versus Dc-Link Voltage Balance.

As it has already been shown, the dc-link voltage control is obtained through control of the variable μ, so that:

$$\text{If } I_{rad}PV1 = I_{rad}PV2, \quad \mu = 0.5$$

$$\text{If } I_{rad}PV1 > I_{rad}PV2, \ 0.5 < \mu < 1.0$$

$$\text{If } I_{rad}PV1 < I_{rad}PV2, \quad 0 < \mu < 0.5.$$

Or, the control variable "*m*" varies from 0 to 1.0. In order to estimate the limit of the control operation, as a function of shading, the modulation index was first fixed. Next panel PV1 was submitted to shading until the control variable m reaches 0, while panel PV2 was kept at the reference value. In the following, panel PV2 was put under shading till the moment in which *m* =1.0, while PV1was kept at the reference value. Figure 14 depicts the control action region for *m* between 0.5 and 1.0. High modulation index indicates less shading variation in panels. For instance, with *m* = 1.0 the change in radiation can be of 14.3% at maximum. Instead, with *m* = 0.5 such variation can reach 92%.

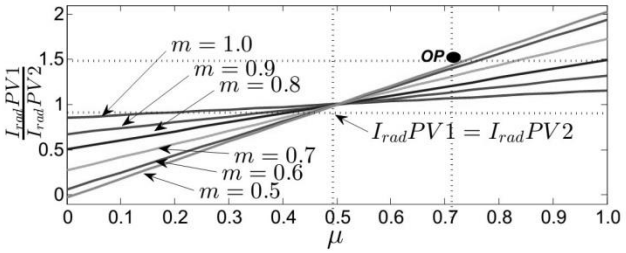

Fig. 14. Shading limit for dc-link voltage balance.

Figure 15 shows the behavior of the control variables m and m when during the system operation does occur a 50% shading event at t = 0.92s in panel PV2. It may be observed that in this condition variable μ converges toward 0.72 while the modulation index converges toward 0.51. This operation point is indicated in Fig. 14 as "OP".

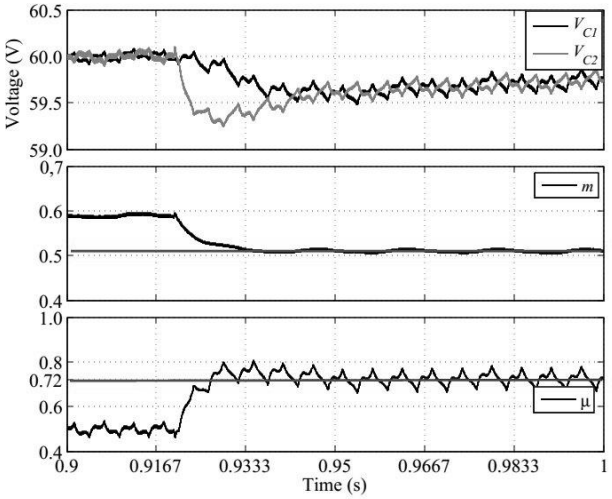

Fig. 15. Simulation results: shading of 50% in PV2.

V. EXPERIMENTAL RESULTS

The inverter employed for obtaining the experimental results is composed of IGBTs controlled by dedicated drives. The generation of control signals was done with the help of the DSP TMS320F28335. For emulation of the solar panels a two channels source E4360A was used. The source was adjusted so that one channel provided 1000 W/m^2 while the other one provided 900 W/m^2, under same temperature. Each source channel was connected to a boost converter with an input inductance of 2,2mH and an output capacitance of 2,200 μF. The inverter output load was composed of R = 50Ω and L=7,2mH.

Figure 16(a) presents the three-phase currents i_a, i_b and i_c. These currents are equilibrated and with acceptable distortion. In Figure 16(b) is shown the voltages obtained with the experimental set-up. As it can be seen it was obtained the capacitor voltages equilibrium even under partial shading. Both pole and line voltages have their levels well defined thus allowing ideal conditions operation. Finally, Figure 16(c) presents the output diode current for each boost converter. Since the panels do not provide equal irradiation, the currents have different values. In this case control compensated the central point current injection for obtaining the dc-link voltage control.

VI. CONSIDERATIONS ON GRID CONNECTION

Although the grid connected inverter is not the focus of this paper the proposed control was adapted to this case. Main difference consists in the dc-link total voltage control loop, since the dc-link capacitor voltages control loop can be the same as in Figure 5. Although the results are not shown, the case voltage drops of 10% and 20% occurred in phase A and phase C, respectively, while one panel was submitted to an irradiation of 1000W/m^2 and the other one was submitted to 900W/m^2.The control action was satisfactory. Additional parameters used: voltage grid of 60 V; filter inductance of 7 mH ; dc-link voltage of V_{DC}=120 V.

VII. CONCLUSIONS

This paper proposed a NPC three-level inverter fed by two photovoltaic modules in which the maximum power point tracking is realized with the help of two boost converters. Under a possible shading of the PV modules it was necessary to adjust the control in order to maintain balance in the dc-link voltages. The proposed control scheme has been verified by applying a 10% change in the irradiance of one of the panels with balance of the dc-link voltages. It was verified that current *THD* and voltage *WTHD* presented low values even under shadow occurrence. In addition, the behavior of the system as a function of switches losses, dc-link high frequency losses and thermal stress have been investigated. In addition the shading limits for having capacitors voltages balance have been established. The dc-link control is also satisfactory when the inverter is grid connected.

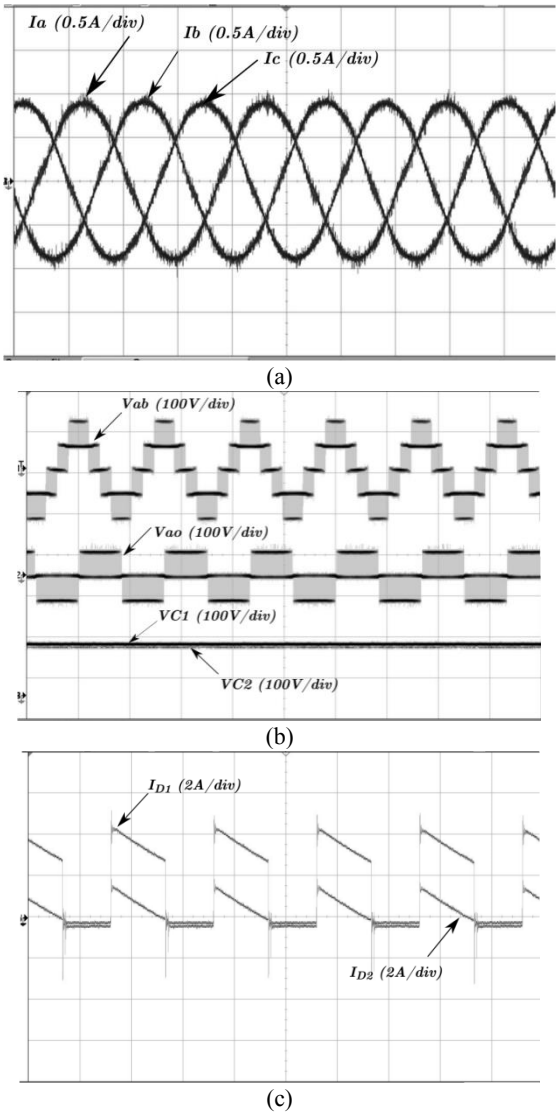

Fig. 16. Experimental results: (a) three-phase output currents; (b) line voltage (top), pole voltage (middle) and dc-link voltages (v_{C1} and v_{C2}, bottom); (c) diode currents.

APPENDIX

The methodology used for controllers design is given in the following [18], [19]. Considering the values of v_{max} and v_{min} as constants, and renamed as k_1 and k_2, respectively, (7) can be rewritten as

$$v_h = (1-2\mu)\frac{V_{DC}}{2} + \mu(k_2 - k_1) - k_2\,, \qquad (10)$$

so that the reference voltage is given by:

$$v_{jo}\_new^* = v_{jo} + (1-2\mu)\frac{V_{DC}}{2} + \mu(k_2 - k_1) - k_2\,. \qquad (11)$$

Since the control objective is not voltage v_{jo},, this term together with $-k_2$ can be considered as perturbations. Therefore,

$$v_{jo}\_new^{*} = -\frac{V_{DC}}{2} + \mu(k_2 - k_1 + V_{DC}) . \quad (12)$$

In frequency domain, taking into account the PI gain, it can be written:

$$v_{jo}\_new(s) = -\frac{V_{DC}}{2s} + \mu(s)k . \quad (13)$$

On the other hand, the reference voltage cannot be considered as an ideal source since it is a function of the bus voltage, which is given by [19]:

$$v_c(s) = v_c^{"}(s)\frac{V_{DC}}{s\tau + 1}\frac{1}{sC} . \quad (14)$$

For $v_{jo}\_new^{*}(s)=v_c(s)$, it comes:

$$v_c^{"}(s)\frac{V_{DC}}{s\tau + 1}\frac{1}{sC} = -\frac{V_{DC}}{2s} + \mu(s)k . \quad (15)$$

This way, the transfer function is given by:

$$G_{mf}(s) = \frac{\frac{k_i V_{DC}}{k\tau C}}{s^2 + s\frac{1}{\tau} + \frac{k_i V_{DC}}{k\tau C}} . \quad (16)$$

Controller parameters can be calculated from

$$k_i = \frac{Ck}{4V_{DC}\tau} \quad (17)$$

and

$$k_p = \frac{Ck_i}{r_{res}} \quad (18)$$

where r_{res} is the series capacitor resistance.

ACKNOWLEDGEMENTS

This Project was financially supported by CNPq, CAPES and FAPESP-PB.

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