PULSE-WIDTH-MODULATION FOR A MODIFIED HYBRID 2/3-LEVEL CONVERTER

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***Abstract* – This paper proposes a modification in both topology and operation algorithm for the existent 2/3 level converter. The modified strategy is of simple implementation. In addition, the modified topology reduces the switching losses and the command complexity. The harmonic distortion and losses of the two-level converter, the three-level Neutral-Point-Clamped (NPC) converter and the 2/3-level converter are compared. Also the limitation of the modified topology operation is investigated. Simulated and experimental results demonstrate the validity of the proposed topology and pulsewidth modulation method.**

***Keywords* – Multilevel Converters, Pulsewidth Modulation, 2/3-Level Converter.**

I. INTRODUCTION

Multi-level converters were first conceived for high-voltage and high-power applications. The neutral-point-clamped (NPC) inverter was first proposed in [1] and [2]. Since then, many configurations have been considered [3], [4], with the objective of establishing highly desirable characteristics for high-power applications, such as reduced waveform distortion and low blocking voltage by switching devices [5]. Besides the NPC, the other well-known configurations are the flying capacitor, the cascaded H-bridge, and the modular multilevel inverters [6], [7]. In special the NPC can be obtained from stacking two basic cells as shown in Figure 1(a), where the symbol (\) represents semiconductor switches. The scheme of Figure 1(b) is obtained by connecting terminals A and B with an additional basic cell. Its practical realization can be seen in Figures 1(c), for a three-level NPC inverter leg, and Figure 1(d), for a three-level active NPC (ANPC) inverter leg [8].

For this kind of inverter leg, the three-phase version is achieved by connecting three legs in parallel, with only one DC-bus voltage as shown in the scheme of Figure 2(a). This means additional components and more elaborated control strategies. Nevertheless, the three-level NPC converters can be economically competitive at the low voltage range (less than 575 V) as in low-voltage drives application [9]. An alternative three-phase scheme does exist, which combines two- and three-level legs resulting in a reduced number of components: the hybrid 2/3-level converter proposed in [10] and shown in Figure 2(b). The same principle has been exploited in [11] and [12] but directed to other structures. An important aspect to be considered in multilevel converters is the modulation techniques used to synthesize the output voltage. First concepts of those techniques were introduced in [2], [13] and [14] and, since then, many modulation strategies have been developed [15]–[20].

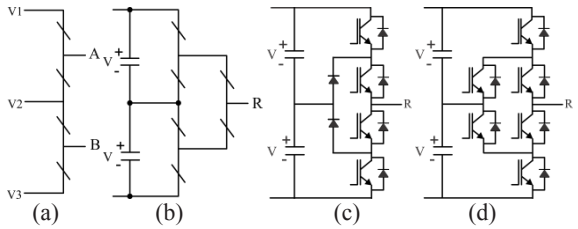

Fig. 1. Stacking of cells to form NPC and ANPC inverters.

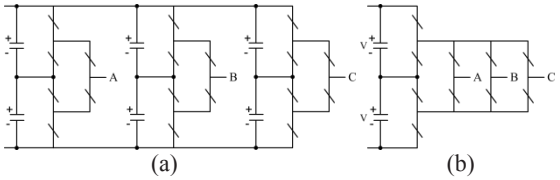

Fig. 2. Three-phase topology schemes.

Figure 3 shows the hybrid 2/3-level converter proposed in [10]. Such converter is constituted by a three-phase bridge, S_{x1}-S_{x2} (x = a, b, c), and four auxiliary switches, S_1-S_4. Auxiliary switches S_1 and S_2 (S_3 and S_4) enable the positive (negative) side of the three-phase bridge to be connected to the positive (negative) dc-link or to the central point O, respectively. Since one of the legs in the topology of Figure 3 can be seen as a three-level ANPC leg, the converter is also referred in this paper as hybrid 2/3-level ANPC inverter.

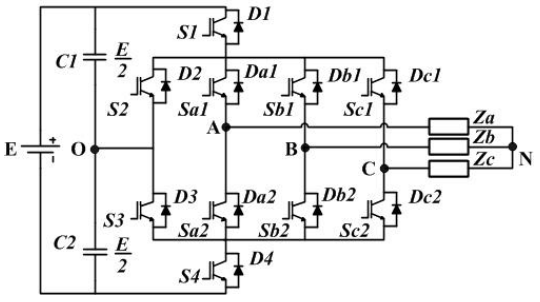

Fig. 3. Hybrid 2/3 level ANPC inverter [13].

In particular, Mihalache proposed an algorithm for the pulsewidth modulation (PWM) control of the hybrid 2/3-level converter of Figure 3 in [10]. That paper details the

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PWM technique, proposes its simplification and also the simplification of that topology. The new strategy reduces the effort of the algorithm implementation. In addition, the simplified topology reduces the switching losses and the command complexity. Total Harmonic Distortion (THD) and losses of the two level (2L) inverter, the NPC three level (3L) inverter and the 2/3-level modified inverter are compared against each other. Simulated and experimental results validate the proposed topology and PWM strategy.

II. MIHALACHE MODULATION STRATEGY

Considering that the three-phase sinusoidal reference voltages are divided into six 60 degrees sectors, from I to VI, as in Figure 4, maximum, middle and minimum voltages can be defined inside each sector, that is, v_{max}=max(v_a,v_b,v_c), v_{mid}=mid (v_a,v_b,v_c), and v_{min}=min(v_a,v_b,v_c).

The basic idea of the method exposed in [10] is to reproduce, when possible, the maximum voltage (v_{max}) with the help of levels zero (0) and +E/2 (P) and the minimum voltage (v_{min}) with the help of levels zero and –E/2 (N). This modulation was referred to as 3L-modulation. Reproduction of the middle voltage (v_{mid}) is achieved with the help of levels +E/2 and –E/2, referred to as 2L-modulation. In case 3L-modulation is not possible to reproduce v_{max} and v_{min} then the 2L-modulation is used for the corresponding phase(s). The modulation strategy proposed in [10] uses two level-shifted triangular waveforms, v_{t1} and v_{t2}, for 3L operation; 2L operation is obtained with the help of the triangular waveform v_{t3}, as shown in Figure 5. Such waveforms are compared with the reference waveforms (v_a,v_b,v_c) to define the switching states.

For understanding the selection of either 2L- or 3L-modulation, Sector I ($v_a > v_b > v_c$) will be initially analyzed and then results will be extended to the other sectors.

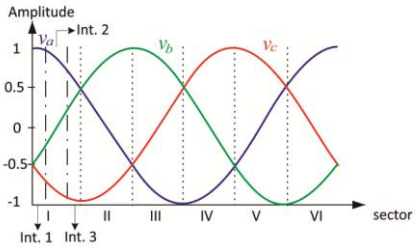


Fig. 4. Sectors and intervals in Sector I.

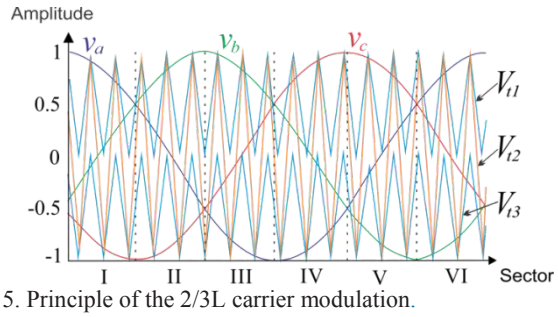


Fig. 5. Principle of the 2/3L carrier modulation.

At the beginning of Sector I, referred as *Interval 1* in Figure 4, the reference voltage v_a is much larger than v_b and v_c. Therefore, it is possible to employ the three-level modulation to reproduce the maximum voltage v_a and the two-level modulation to reproduce the middle voltage v_b, inside a switching period. Since the difference between v_b and the minimum voltage v_c is small, the two-level modulation can be also employed to reproduce the reference voltage v_c. The pulse generated by v_a inside the switching period is larger than the pulses generated by v_b and v_c, as shown in Figure 6. The required condition for this operation is that the pulse for S_1 (phase A under 3L-modulation, with S_{a1} kept on) is bigger than the pulse for S_{b1} (phase B in 2L-modulation). This condition can be described by considering the similarity of the triangles formed by the carriers v_{t1} and v_{t2} and the respective reference voltages as depicted in Figures 7(a) and 7(b). From those triangles, it can be written:

$$\frac{1-v_a}{y}=\frac{1}{x}\rightarrow y=x(1-v_a) \quad (1)$$

$$\frac{1-v_b}{z}=\frac{2}{x}\rightarrow z=\frac{x}{2}(1-v_b) \quad (2)$$

in which y is the level O application time in phase A, z is the level –E/2 application time in phase B, and x is the modulation period.

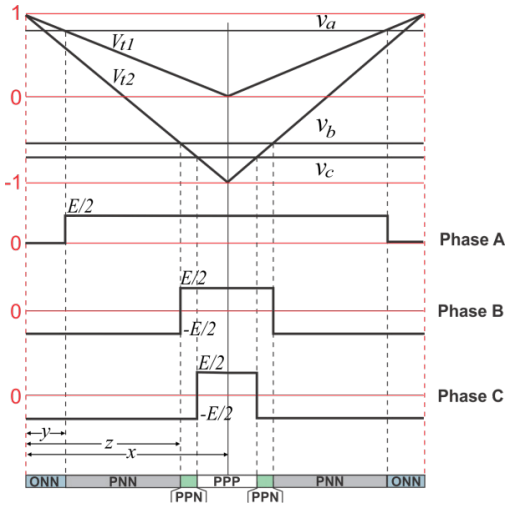


Fig. 6. Sector 1: Interval 1 commutation waveforms.

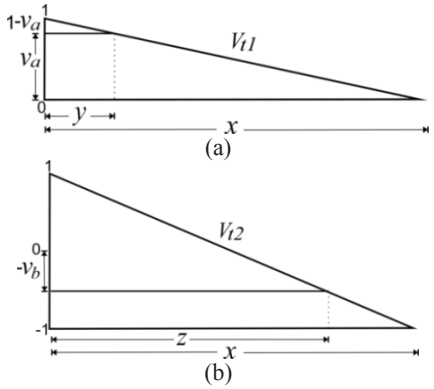


Fig. 7. Triangles formed by carriers and voltages v_a and v_b during Interval 1.

Since the pulse for S_1 must be bigger than the pulse for S_{b1}, $y < z$, then,

$$x(1 - v_a) < \frac{x}{2}(1 - v_b)$$

or

$$v_a > \frac{1}{2} + \frac{v_b}{2}. \quad (3)$$

As v_b increases and v_c decreases along Sector I, the difference between these two phases becomes large enough at a certain point to enable the use of 3L-modulation for reproducing v_c. 2L-modulation is kept for v_b. Such region is indicated as *Interval 2* in Figure 4. In other words, the pulse generated by v_b inside the switching period becomes larger than the one generated by reference v_c, as shown in Figure 8. This condition is satisfied while the pulse for S_{b1} (phase B under 2L-modulation), is bigger than the pulse for S_3 (phase C in 3L-modulation with S_{c2} kept on). From Figure 8, the triangles formed by the carriers v_{t1} and v_{t2} and the reference voltages v_a and v_b, as shown in Figures 9(a) and 9(b), can be obtained. Considering the similarity of the triangles, and x, y and z as defined in the figures, it can be written:

$$\frac{1 - v_b}{y} = \frac{2}{x} \rightarrow y = \frac{x}{2}(1 - v_b) \quad (4)$$

$$-\frac{v_c}{z} = \frac{1}{x} \rightarrow z = -xv_c \quad (5)$$

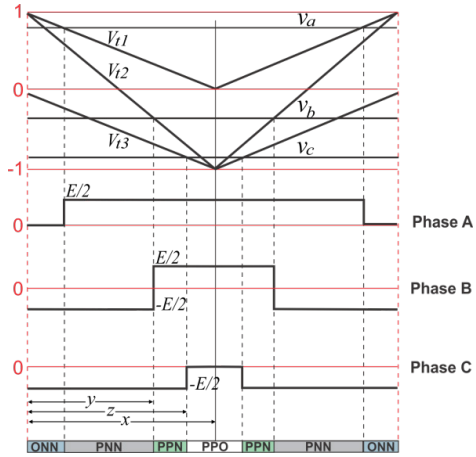


Fig. 8. Sector 1: Interval 2 commutation waveforms.

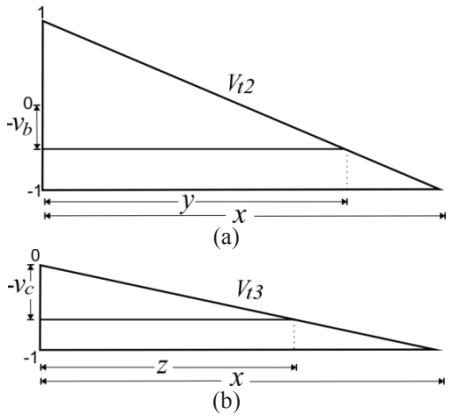


Fig. 9. Triangles formed by carriers and voltages v_a and v_b during Interval 2.

in which y is the level –E/2 application time in phase B, z is the level –E/2 application time in phase C, and x is the modulation period.

Since the pulse for S_{b1} must be bigger than the pulse for S_3, that is, $y < z$, then

$$\frac{x}{2}(1 - v_b) < -xv_c$$

$$\frac{1}{2}v_b > \frac{1}{2} + v_c. \quad (6)$$

Yet, while v_a and v_c decrease during Interval 2, v_b increases so that the difference between the pulses in phase A and phase B becomes smaller and smaller. At a certain point, (3) cannot be satisfied anymore. That is the beginning of an interval at the end of the sector, referred as *Interval 3* in Figure 4, in which the difference between v_a and v_b is small while the difference between these two and v_c is a big one. It is then possible to employ the 3L modulation for v_c and the 2L modulation for reference voltages v_a and v_b, as shown in Figure 10.

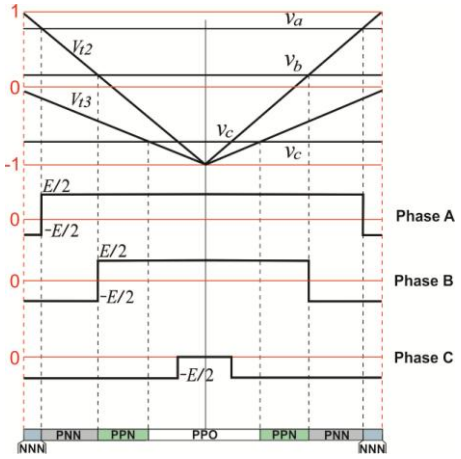


Fig. 10. Sector 1: Interval 3 commutation waveforms.

Therefore, during Interval 1 only (3) is satisfied while (6) is not satisfied; during Interval 2 both (3) and (6) are satisfied; finally, during Interval 3 only (6) is satisfied while (3) is not satisfied. Consider that the fact of (3) and (6) are not satisfied can be respectively described by

$$v_a < \frac{1}{2} + \frac{v_b}{2} \quad and$$

$$\frac{1}{2}v_b > \frac{1}{2} + v_c. \quad (7)$$

Then, the equations that represent Intervals 1, 2, and 3 can be written respectively as:

$$v_a > \frac{1}{2} + \frac{v_b}{2} \text{ and } \frac{1}{2}v_b < \frac{1}{2} + v_c \quad (8)$$

$$v_a > \frac{1}{2} + \frac{v_b}{2} \text{ and } \frac{1}{2}v_b > \frac{1}{2} + v_c \quad (9)$$

$$v_a < \frac{1}{2} + \frac{v_b}{2} \text{ and } \frac{1}{2}v_b > \frac{1}{2} + v_c. \quad (10)$$

As already mentioned, v_a has the largest voltage value, v_{max}, v_b has the medium voltage value, v_{mid}, and v_c has the smallest voltage value, v_{min}, when compared to each other, in Sector I. Taking into account that v_{max}=max(v_a,v_b,v_c), v_{mid}= mid(v_a,v_b,v_c), and v_{min}=min(v_a,v_b,v_c), (8) to (10) can be written in a generalized form and can be applied to any of the six sectors. That is,

$$v_{max} > \frac{1}{2} + \frac{1}{2}v_{mid} \text{ and } \frac{1}{2}v_{mid} < \frac{1}{2} + v_{min} \quad (11)$$

$$v_{max} > \frac{1}{2} + \frac{1}{2}v_{mid} \text{ and } \frac{1}{2}v_{mid} > \frac{1}{2} + v_{min} \quad (12)$$

$$v_{max} < \frac{1}{2} + \frac{1}{2}v_{mid} \text{ and } \frac{1}{2}v_{mid} > \frac{1}{2} + v_{min}. \quad (13)$$

For practical implementation, Intervals 1, 2, and 3 do not need to be calculated for establishing which modulation type, 3L or 2L, is adequate for each phase. In fact the method consists in only evaluating if (11) to (13) are true or false, with v_{mid} calculated by

$$v_{mid} = -\frac{v_{max} + v_{min}}{2}. \quad (14)$$

Based on those decisions the modulation types, 3L or 2L, are chosen to be applied to the phases identified as v_{max}, v_{mid} and v_{min} for each sector, as show in the flowcharts of Figure 11. It can be noticed from those flowcharts that in the case in which (11) to (13) are not satisfied all phases are 2L-modulated. This occurs when the modulation index is below 0.5. In this case, the pulses generated by v_{max} are not sufficiently larger than the pulses generated by v_{mid}, which, in turn, are not sufficiently larger than the pulses generated by $v_{min.}$ This way, it is impossible to employ 3L-modulation for any of the three phases.

The procedure for application of the strategy proposed in [10] consists then in:

- Defining the reference voltages v_a, v_b and v_c;
- Determining v_{mid};
- Determining the six 60 degrees sectors;
- Evaluating for each sector if (11), (12) and (13) are true or false, as in the flowchart of Figure 11.
- Employing the adequate type of modulation, 3L or 2L.

One interesting point of this strategy is that three-phase operation does not produce *medium vectors*, as defined in Space Vector Modulation, making easier the control of the capacitors voltage balance.

III. MODIFIED TOPOLOGY AND MODIFIED MODULATION STRATEGY

The strategy implementation with the use of (11) to (13), as proposed in [10], needs the identification of six sectors that are divided in three intervals each, thus resulting in a total of eighteen intervals, as shown in Figure 12. In addition, for each interval, it is necessary to determine which one, 2L or 3L, should be applied to each phase. This approach results in 54 operations. A modified technique is introduced next to reduce this time operation.

Rearranging (8), (9) and (10) leads to [21]:

$$v_a > \frac{1}{2} + \frac{1}{2}v_b \text{ and } -\frac{1}{2} + \frac{1}{2}v_b < v_c \quad (15)$$

$$v_a > \frac{1}{2} + \frac{1}{2}v_b \text{ and } -\frac{1}{2} + \frac{1}{2}v_b > v_c \quad (16)$$

$$v_a < \frac{1}{2} + \frac{1}{2}v_b \text{ and } -\frac{1}{2} + \frac{1}{2}v_b > v_c. \quad (17)$$

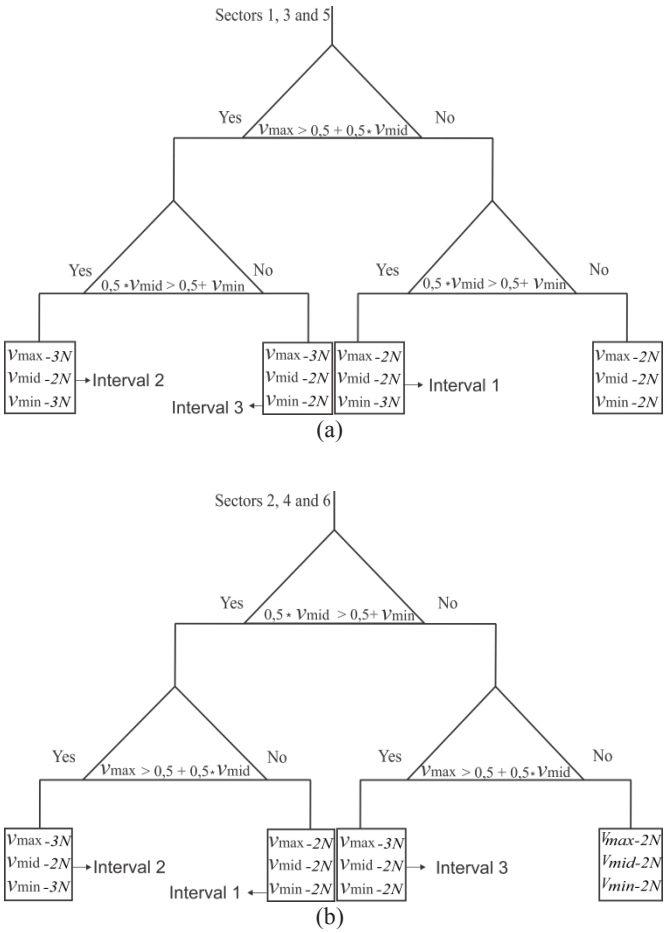


Fig. 11. PWM modulator flowchart as in [10]: (a) for sectors 1, 3 and 5; (b) for sectors 2,4 and 6.

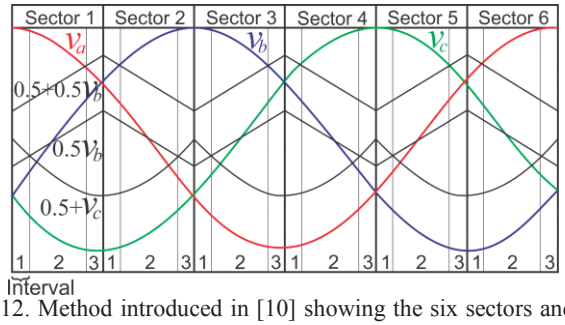


Fig. 12. Method introduced in [10] showing the six sectors and the eighteen intervals to be determined.

It has been shown that during Interval 1, v_a is switched with 3L-modulation while v_b and v_c are switched with 2L-modulation; that during Interval 2, v_a and v_c are switched with 3L-modulation and v_b with 2L-modulation; and that during Interval 3, v_a and v_b is switched with 2L-modulation and v_c with 3L-modulation.

The conditions from (15) to (17) can be written in the general form as

$$\text{If } v_{ref} > \frac{1}{2} + \frac{1}{2}v_{mid} \text{ or } v_{ref} < -\frac{1}{2} + \frac{1}{2}v_{mid} \qquad (18)$$

v_{ref} is modulated in 3 levels;

$$\text{If } \frac{1}{2} + \frac{1}{2}v_{mid} < v_{ref} < -\frac{1}{2} + \frac{1}{2}v_{mid} \qquad (19)$$

v_{ref} is modulated in two levels, for $v_{ref} = \{v_a, v_b, v_c\}$ and $v_{mid} = mid\{v_a, v_b, v_c\}$.

In summary, satisfaction of the conditions in (18) and (19) by one of the references v_a, v_b or v_c clearly defines the type of modulation to be employed. As shown in Figure 13, the division in sectors is no longer necessary. In this modified method the comparison of the references voltages with the expression of v_{mid} allows for determining which type of modulation, two or three-level, will be applied to each phase in only 9 operations, instead of 54 ones.

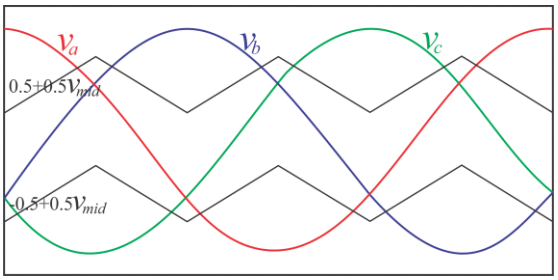


Fig. 13. Proposed method: realization of (17) and (18).

The procedure for using the new strategy consists in:

- Defining the reference voltages v_a, v_b and v_c;
- Determining v_{mid};
- Comparing the reference voltages via (18) and (19);
- Employing the adequate type of modulation, 3L or 2L.

The corresponding flowchart is presented in Figure 14.

The proposed method also accepts the injection of zero-sequence-signals to the three reference voltages in order to extend linearity till a modulation index of 1.15. The zero-sequence-signal injected to the three-level modulation can be the same as that added to each phase reference of a two-level carrier-based modulator leading to similar results as the conventional Space Vector Modulation [10], [16], [17]. For instance, with the addition of the term $v_h = v_{mid}$, (18) and (19) become

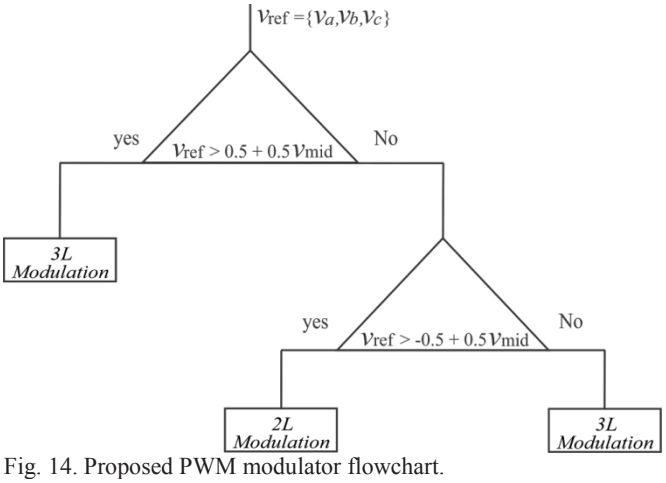


Fig. 14. Proposed PWM modulator flowchart.

$$\text{If } v_{ref} > \frac{1}{2} + \frac{1}{4}v_{mid} \text{ or } v_{ref} < -\frac{1}{2} + \frac{1}{4}v_{mid} \qquad (20)$$

$$\text{If } \frac{1}{2} + \frac{1}{4}v_{mid} < v_{ref} < -\frac{1}{2} + \frac{1}{4}v_{mid}. \qquad (21)$$

Alternative zero-sequence-signals can be also added so that the different modulated waveforms can be obtained.

An alternative to the circuit in Figure 3 is the topology shown in Figure 15 in which the three-level NPC leg is replaced by a three-level NPC leg [21]. In other words, switches S_2 and S_3 are eliminated from Figure 2 thus simplifying the inverter topology. Figure 16 shows the equivalent configurations or the modified topology for Sector I and Interval 1. All states for the three intervals are presented in Table I. Elimination of switches S_2 and S_3 is possible because those switches are allowed to not conduct until the load power factor forces it. By simulation, this limit was found to be around 0.66. For power factors smaller than that limit the current direction interferes on the O level application. For instance, if the converter is operating with the three-level modulation in the positive half-cycle with the current flowing from the load toward the dc-bus, and levels P and O are to be applied, the level O cannot be applied until the current becomes positive. This is due to the fact that at least one phase is operating with 2L modulation, what obliges S_4 to be in conduction. The alternative of turning S_2 off and turning S_3 on connects then the output to N instead of O. However, the simplified topology can be applied to the market of low voltage applications with power factor superior to 0.66.

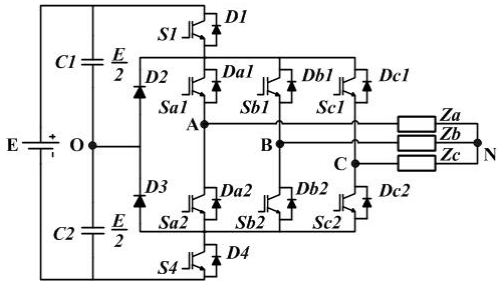
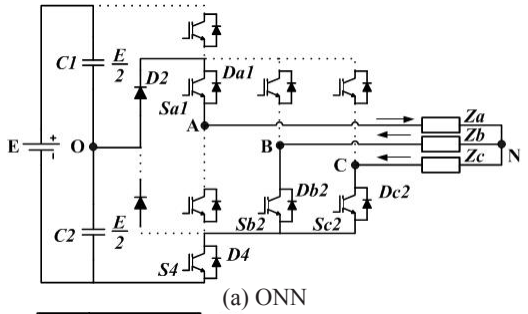
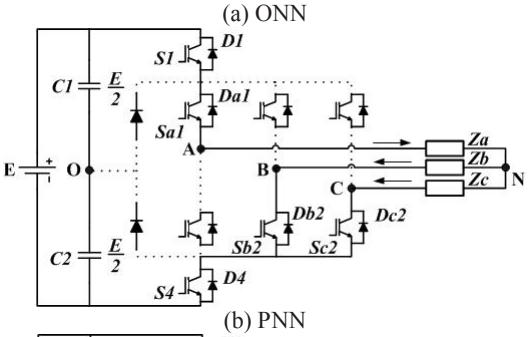


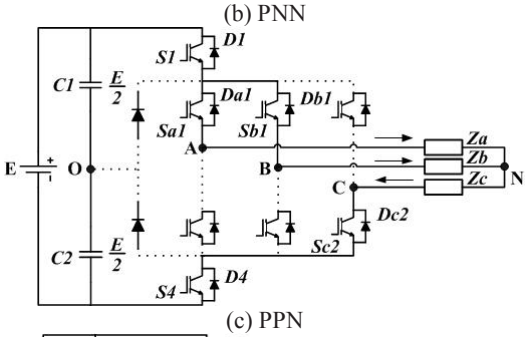
Fig. 15. Hybrid 2/3-level NPC converter.



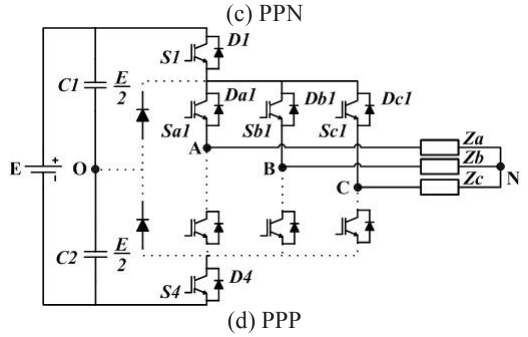
(a) ONN



(b) PNN



(c) PPN



(d) PPP

Fig. 16. Modes of operation for Interval 1 in Sector I.

TABLE I
Sequence of States Inside the Three Intervals

Interval 1	PNN	PPN	PPP	PPN	PNN	ONN
Interval 2	PNN	PPN	PPO	PPN	PNN	ONN
Interval 3	PNN	PPN	PPO	PPN	PNN	NNN

IV. SIMULATED RESULTS

Figures 17 to 20 show simulated results of the proposed converter in Figure 15 by using the proposed algorithm. Figures 17(a), 17(b) and 17(c) show respectively: (a) pole voltage, (b) line voltage, (c) currents in the three-phase load. Detail of the pole is given in Figure 18, in which the Intervals of Sector I are indicated and the switching frequency has been lowered in order to facilitate the visualization of the three operation regions.

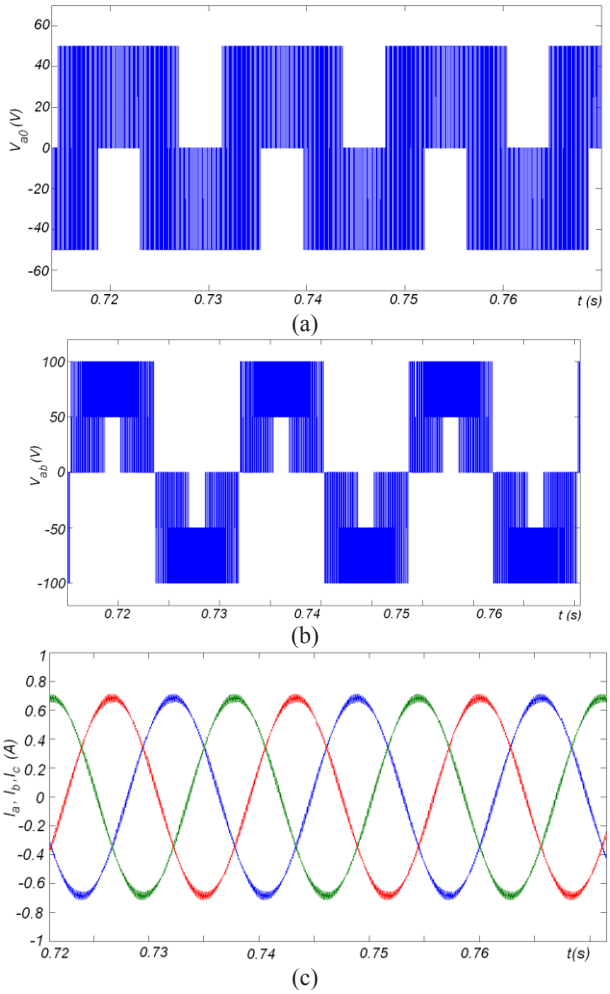


Fig. 17. Simulated results: (a) pole voltage; (b) line voltage; (c) currents in the three-phase load.

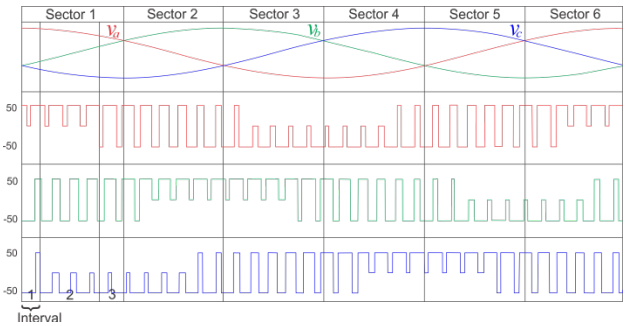


Fig. 18. Details of the pole voltage.

Note from Figure 18 that, for Interval 1, phase A is 3L-modulated while phases B and C are 2L-modulated. At

Interval 2, phase C switches from 2L- to 3L-modulation, while phases A and B keep the previous modulation, that is 3L and 2L, respectively. Finally, it can be seen that at Interval 3 phase A changes to 2L modulation while phases B and C keep the modulation as in Interval 2, that is, 2L and 3L, respectively.

In Figure 19 the current THD of the 2-, 2/3- and 3-level converters are compared against each other as a function of the modulation index, *m*. The parameters are: dc-bus voltage equal to 100 V; C1 = C2 = 2200 μF; load composed of R = 65 Ohms and L = 7 mH; switching frequency = 10 kHz. Note that the line voltage for the 3L-NPC modulator is composed of two phases that use 3L-modulation; in the new hybrid 2/3-level modulator one phase uses 3L-modulation and other one uses 2L-modulation; in the regular two-level modulator both phases use 2L-modulation. As expected, the THD of the 2/3-level converter presents better results than the 2 level converter and worse results than the 3-level converter.

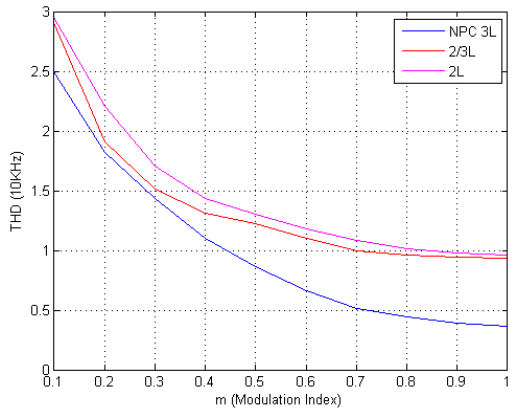


Fig. 19. THD comparison among 2-, 2/-3 and 3-level converters.

Similar behavior occurs with the Weighted THD (WTHD). Figure 20 compares the line voltage Distortion Factor, DF1, of the 2-, 2/-3 and 3-level converters. For m < 0.4, the 2/3 level and the 2-level topologies have the same number of levels and consequently same DF1. The 3-level operation of the 2/3-level topology that occurs for higher values of m, improves its performance although its DF1 continues to be higher than the 3-level topology.

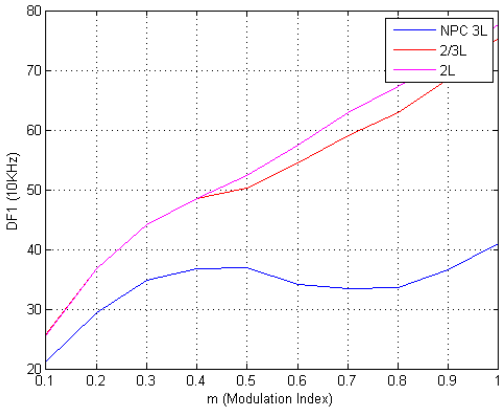


Fig. 20. Comparison of DF1 among 2-, 2/-3 and 3-level converters.

Also the losses have been calculated for the three topologies operating with frequencies of 750 Hz, 2 kHz 5 kHz, and 10 kHz and dc-bus values of 150 V, 300 V, and 600 V. It was observed that in the range from 750 Hz/150 V to 5 kHz/300 V the 2-level topology has less total losses than the those of 3-level and hybrid 2/3-level ones, although the values of the losses produced by these two are close to each other. From 5 kHz/600 V on, the total losses of both 3-L and 2/3-L topologies are smaller than that of the 2-L converter, favoring the 3-L topology for both higher frequency and higher dc-bus voltage, as shown in Figure 21.

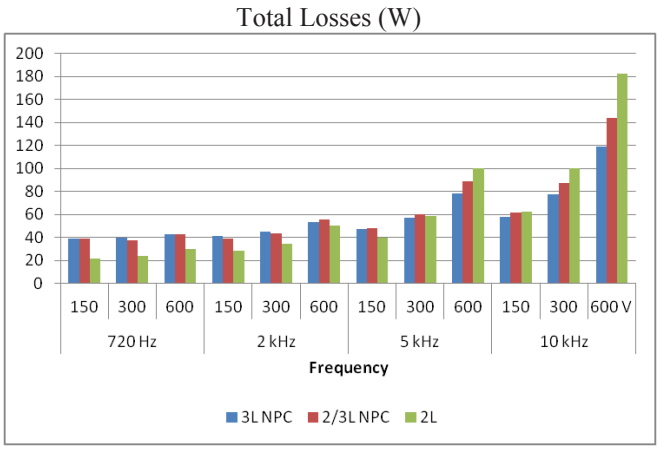


Fig. 21. Comparison of total losses versus frequency and dc-bus.

As expected, the performance of the proposed topology is between that of the 2- and 3-level converters. However, the 2/3-L topology is reduced of four active switches and four diodes when compared to the 3-L NPC topology. Also, in terms of total losses the proposed topology becomes competitive, for the conditions examined, for low-voltage (150 V) from 5 to 10 kHz and for higher voltage (600 V) from 2 to 5 kHz. Since, for higher voltage at the frequency range from 5 to 10 kHz, losses highly favor the 3-L NPC inverter, the proposed inverter seems adequate for low-voltage motor drives.

V. EXPERIMENTAL RESULTS

Tests have been made with the experimental set-up shown in Figure 22.

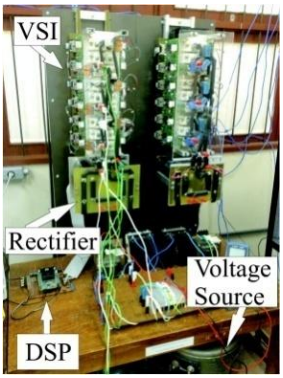


Fig. 22. Experimental setup.

Results in Figure 23(a) were obtained for the three pole voltages and the load current in one of the phases. In Figure 23(b), it is shown the three line voltages together with one of

the phases load current, while in Figure 23(c) the line voltage is shown together with the three-phase load current. Parameters are the same as used in Figure 17. Although the topology has been tested with low power it can be used in the 15 kVA range.

It can be seen that simulated and experimental results agree and 2L and 3L-modulation can be seen in both results.

An important aspect is that in DSPs, the triangle waveforms can be only positive since they are implemented

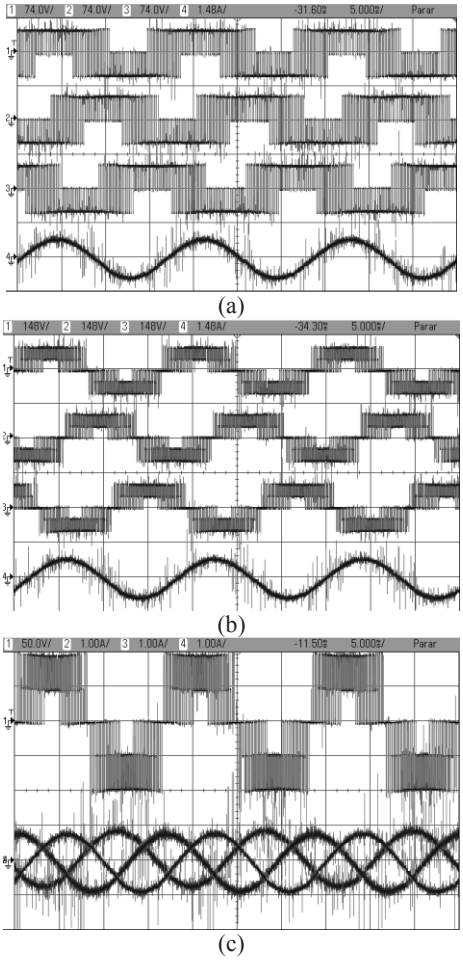


Fig. 23. Experimental results: (a) pole voltages, 74 V/div., and load current, 1.0 A/div; (b) line voltages, 74 V/div., and load current, 1.0 A/div ; (c) line voltage , 50 V/div., three phase load current, 1.0 A/div.

via counters. Or, the implementation of the three-level modulation needs two counters for emulating the carrier signal and only one counter is available in the DSP. In order to overcome such problem, a set formed by one counter to emulate the carrier, one sinusoidal reference for the two-level operation and one modified reference (inverted at the end of the positive half-cycle) for the three-level operation, as shown in Figure 24. It should be mentioned that this set of signals is equivalent to that in Figure 5.

VI. CONCLUSIONS

In this paper it is proposed a 2/3-level converter modulation much simpler than that found in [10] for the 2/3-level converter operation. The new PWM strategy simplifies

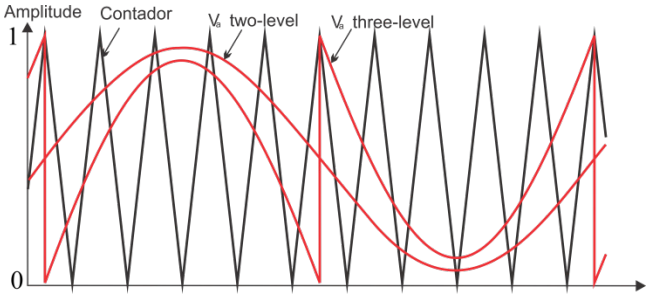


Fig. 24. Equivalent principle used for DSP implementation.

the algorithm implementation, needing only 9 operations, instead of the 54 ones needed by its counterpart, for generating the same results. A comparative study among the two-level converter, NPC three level converter and the modified 2/3-level converter (reduced of two switches when compared to its counterpart) shows that that the last one has a THD in between the two other. Experimental results verify the proposed modulation and modified topology. Although the modified topology can only operate with load power factors larger than 0.66, there is a large range of low-voltage industrial applications in which the power factor is superior to that value that allows its usage. In case of loads with a smaller power factor, however, the ANPC version is necessary for operation.

ACKNOWLEDGEMENTS

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REFERENCES

[1] R. H. Baker “Bridge converter circuit”, US Patent 4270163, May 26, 1981.

[2] A. Nabae, I. Takahashi, H. Akagi, “A new neutral-point-clamped pwm inverter”, *IEEE Transactions on Industry Applications*, vol. 17, n. 5, pp. 518 –523, Sept. 1981.

[3] S. Mariethoz, A. Rufer, “New configurations for the three-phase asymmetrical multilevel inverter”, *in Proc. of IEEE IAS Annual Meeting*, vol. 2, pp. 828 – 835, 2004.

[4] H. Weng, K. Chen, J. Zhang, R. Datta, X. Huang, L. Garces, R. Wagoner, A. Ritter, P. Rotondo, “A four-level converter with optimized switching patterns for high-speed electric drives”, *in Proc. of IEEE PESC,* pp. 1585 –1591, 2007.

[5] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, J. Leon, “Recent advances and industrial applications of multilevel converters”, *IEEE Transactions on Industrial Electronics,* vol. 57, n. 8, pp. 2553 –2580, Aug. 2010.

[6] P. Chan, H.-H. Chung, S. Hui, “A generalized theory of boundary control for a single-phase multilevel inverter using second-order switching surface”, *IEEE Transactions on Power Electronics,* vol. 24, n. 10, pp. 2298 –2313, Oct. 2009.

[7] A. Boora, A. Nami, F. Zare, A. Ghosh, F. Blaabjerg, "Voltage-sharing converter to supply single-phase asymmetrical four-level diode-clamped inverter with high power factor loads", *Transactions on Power Electronics,* vol. 25, n. 10, pp. 2507 –2520, Oct. 2010.

[8] T. Brückner, S. Bernet, H. Güldner, "The Active NPC Converter and Its Loss-Balancing Control", *IEEE Transactions on Industrial Electronics*, vol. 52, n. 3, pp. 855-868, June 2005.

[9] R. Teichmann, S. Bernet, "A comparison of three-level converters versus two-level converters for low voltage drives, traction and utility applications", *IEEE Transactions on Industry Applications,* vol. 41, n. 3, pp. 855-865. May/June 2005.

[10] L. Mihalache, "A Hybrid 2/3 Level Converter with the minimum Switch Count", *in Proc. of IEEE IAS,* vol. 2, pp. 611-618, 2006.

[11] D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S.A. Mussa, M. L. Heldwein, "Symmetrical Hybrid Multilevel DC-AC Converters with Reduced Number of Insulated DC Supplies," *IEEE Transactions on Industrial Electronics*, vol. 57, n.7, pp. 2307-2314, July 2010.

[12] D. Floricau, E. Floricau, G. Gateau, "New Multilevel Converters with Coupled Inductors: Properties and Control", *IEEE Transactions on Industrial Electronics*, vol. 58, n. 12, pp. 5344-5351, Feb. 2011.

[13] R. H. Baker, "Synthesizer circuit for generating three-tier waveforms", U.S. Patent 4,135,235, Jan. 16, 1979.

[14] M.Mazzucchelli, L. Puglisi, Giuseppe Sciutto, "PWM systems in power converters: an extension of the "subharmonic"' method", *IEEE Transactions on Industrial Electronics and Control Instrumentation*, vol. 28, n. 4, pp. 315-322, Nov. 1981.

[15] P. M. Bhagwat, V. R. Stefanovic, "Generalized structure of a multilevel pwm inverter", *IEEE Transactions on Industry Applications,* vol. 19, n. 6, pp. 1057–1069, Nov. 1983.

[16] R. N. C. Alves, A. M. N. Lima, E. R. C. da Silva, C. B. Jacobina, "A new approach to the problem of synthesizing non-sinusoidal waveforms for analog and digital implementations of space vector PWM strategies", *in Proc. of COBEP*, pp. 228-333, 1991.

[17] V. Blasko. "A hybrid PWM strategy combining modified space vector and triangle comparison method", *in Proc. of IEEE PESC'96*, pp. 1872-1878, 1996.

[18] A. S. Oliveira, E. R. da Silva, C. B. Jacobina. A Hybrid PWM Strategy for Multilevel Voltage Source Inverters, *in Proc. IEEE PESC*, pp. 4220-4225, 2004.

[19] J. Rodriguez, P. Correa, and L. Moran, "A vector control technique for medium voltage multilevel inverters", *in Proc. of IEEE APEC*, vol. 01, pp. 173–178, 2001.

[20] F. M. Carnielutti, H. Pinheiro, "Estratégia de Modulação para Conversores Multiníveis em Cascata Simétricos sob Condições de Faltas", *Revista Eletrônica de Potência*, v. 17, n. 2, pp. 555-564, Maio 2012.

[21] J. H. Muniz, E. R. C da Silva, R. B. da Nóbrega, E.C. dos Santos, "An improved pulse-width-modulation for the modified hybrid 2/3-level converter", *in Brazilian Power Electronics Conference* (COBEP), 2013. pp. 248-253.

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