

# BIDIRECTIONAL DUAL ACTIVE CLAMPING PUSH-PULL DC-DC CONVERTER

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**Abstract** – In this paper is presented a bidirectional dual active clamping push-pull dc-dc converter, to be used in applications requiring isolated bidirectional interface between two dc ports with low-voltage/low-current ripple. The main characteristics of the proposed converter are the non necessity of input and output filters in both ports, galvanic isolation, reduced number of magnetic components and high efficiency operation. The paper presents a theoretical analysis of the proposed converter and experimental analysis for a 600 W prototype, with 50 kHz switching frequency, and dc power supplies of 14 and 42 volts, at the input and output ports, respectively. The measured performance agreed well with the theoretical predictions.

**Keywords** – Bidirectional Isolated Dc-Dc Converter, Low Current Stress, Low Input/Output Current Ripple, Phase-Shift, Push-Pull Converter.

## NOMENCLATURE

$\alpha$	Subscript indicating transformer side, $p$ for primary and $s$ for secondary
$\theta_n$	Switching angle
$\eta\%$	Converter efficiency
$a$	Secondary-Primary winding turns ratio
$C_{g\alpha}$	Clamping capacitor of $\alpha$ side
$D_{\alpha k}$	Anti-parallel diode of main transistor $k$ of $\alpha$ side
$D_{\alpha k a}$	Anti-parallel diode of auxiliar transistor $k$ of $\alpha$ side
$E_\alpha$	Voltage Source of $\alpha$ side
$f_s$	Switching frequency
$g_{\alpha k}$	Transistor $T_{\alpha k}$ gating signal
$i_\alpha$	Current through $E_\alpha$ source
$i_{\alpha k}$	Current through $k$ winding of $\alpha$ side
$i_{C_{g\alpha}}$	Current through $\alpha$ side clamping capacitor
$i_{\alpha d}$	Differential mode current of $\alpha$ side
$k$	Numeric subscript
$l_{\alpha k}$	Leakage inductance of $\alpha$ side transformer winding
$p$	Power processed by the converter
$q$	Static gain
$T_{\alpha k}$	Main transistor $k$ of $\alpha$ side
$T_{\alpha k a}$	Auxiliar transistor $k$ of $\alpha$ side
$x_{(n)}$	Value of $x$ during stage $n$
$\langle x \rangle$	Average value of $x$ over half-switching period
$\bar{X}$	Normalized value of $X$
$X^{ref}$	Value of $X$ referred to secondary side
$\delta$	Phase-shift angle
$V_{g\alpha}$	Voltage over $\alpha$ side clamping capacitor

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## I. INTRODUCTION

Many applications related to dual voltage systems [1]–[3], such as telecommunications power supplies, computer power system [4]–[6], electric vehicles [7]–[9] and renewable energy systems [10]–[12] employ bidirectional dc-dc converters.

Several isolated bidirectional converters were proposed in the last years and are available for practical applications. The dual active bridge (DAB) [13]–[16], the dual half-bridge (DHB) and their topological variations [17]–[21] are very attractive options since they present soft switching, high efficiency and high power density. However, they are not appropriate for low voltage and high current applications, due to the large amount of reactive power circulating inside the converter and the presence of large current ripple in the input/output filter capacitor or DC voltage source. This contributes to reduce the efficiency and power density. Modulation strategies [22]–[24] and design methodologies [25], [26] were proposed to minimize reactive power at the cost of increasing operation principle complexity. The LLC resonant converter [27], [28] presents high efficiency but its input/output currents also exhibit large ripple, furthermore, since it is an assymetrical topology, the operation principle differs depending of power flow direction.

In order to reduce this input/output current ripple, the full-bridge and half-bridge topologies [29]–[31] were proposed. Nevertheless, they need a voltage source on one side, through which the high current ripple is going to circulate.

In this research, a novel isolated bidirectional dual active clamped push-pull dc-dc converter topology (DPP) is proposed. Thereby, it has some desirable advantages as compared with the solutions mentioned above, namely lower conduction loss and input and output current ripple. As the proposed circuit belongs to the push-pull family, the theoretical voltage across the power switches is approximately the double of the DC voltage of the related voltage source; therefore, it is not appropriate for high voltage applications. Thus, as it will be demonstrated hereafter, it is suitable for low voltage and high current applications.

Two viable applications for the proposed converter are automotive powernet [32] and telecommunications system [33]. In the first case, a converter interfaces two batteries, a 14 V battery and a 42 V battery. The 14 V battery provides energy to the conventional low voltage automotive loads, such as lighting, ventilation and accessories, and the 42 V battery is responsible for higher power loads, e.g., air conditioning and heating. Galvanic isolation can be employed to decrease short circuit risk between batteries [34]. In the second case, a converter interfaces a low voltage battery and a 42 V bus. In this case, isolation between the two buses can be used for

safety purposes. In both cited papers, the chosen topology is the bidirectional Ćuk converter. Besides galvanic isolation possibility, this topology presents low input and output current ripple which prolongs useful life of batteries and dc-link capacitors. For higher current specifications, this topology becomes infeasible due to the current transistor conduction losses. Therefore, the proposed converter is an interesting option because it has lower current stress among switches.

## II. PROPOSED CONVERTER AND OPERATION PRINCIPLE

Figure 1 shows the power stage diagram of the proposed dual-push-pull converter topology and Figure 2 depicts the modulator circuit and its typical gate signals.

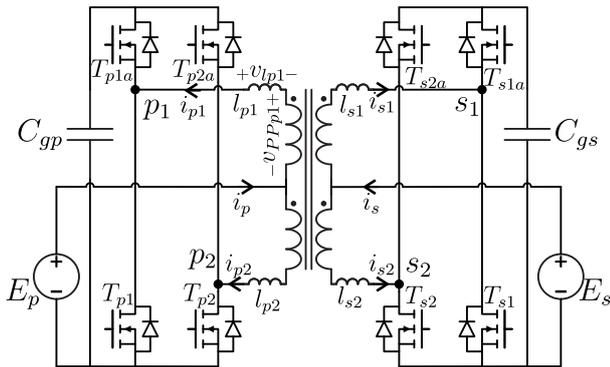
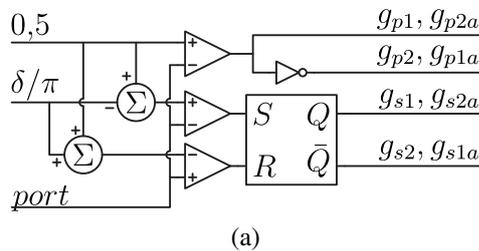
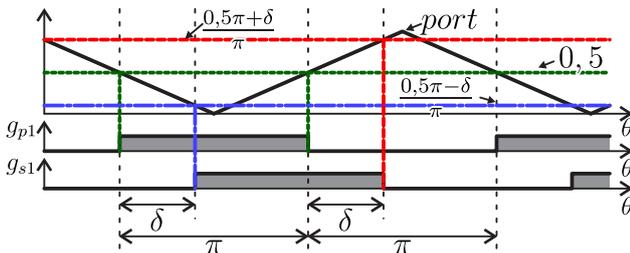


Fig. 1. Power stage diagram of the proposed isolated bidirectional dc-dc converter.



(a)



(b)

Fig. 2. (a) Modulator circuit and (b) typical modulator waveforms.

The modulation strategy consists of gating the primary bridge transistors  $T_{p1}$  and  $T_{p2a}$  with  $g_{p1}$  signal with duty cycle of 50 % and frequency,  $f_s$ . The other primary bridge transistors are gated by the complementary signal of  $g_{p1}$ ,  $g_{p2}$ . The secondary bridge transistors are gated by similar signals with the difference that they are phase-shifted by the angle  $\delta$  from the primary bridge signals. The angle  $\delta$  defines the power flow direction. If it is positive, the power flow is from the primary to the secondary source. Otherwise, if it is

negative, the power is transferred from the secondary source to the primary source.

The operation principle of the converter are described just for  $\delta$  positive since the converter is symmetrical. In the topological state analysis, all components are referred to the secondary side and will be considered ideal. The referred values are represented by adding  $^{ref}$  in property name. In the description of the operation principle, the voltage of  $E_s$  are equal to  $aE_p$  and the voltage on the  $C_{gp}$  and  $C_{gs}$  capacitors is equal to twice the value of  $E_p$  and  $E_s$ , respectively. In this analysis, the transformer will be considered ideal and additional auxiliary inductor will be placed in series with its windings. The primary side auxiliary inductors,  $l_{p1}$  and  $l_{p2}$ , are considered to have the same inductance value,  $l_p$ , as well as the secondary side auxiliary inductors  $l_{s1}$  and  $l_{s2}$  but in this case, the inductance value is  $l_s$ . Although it is not necessary,  $l_s$  is considered equal to  $a^2 l_p$  for simplicity in the topological state analysis. In reality, what really matters is that auxiliary inductors of the same transformer side have the same inductance value. Along with the clamping capacitor voltage and transistor gating signals, these inductances determine the windings currents waveforms. If these parameters do not match, ac component cancellation resulting from the sum of winding currents will not occurs and the source current will present some ripple.

In the illustrations of the topological state, a circle at the transistor gate is used indicating it is enabled and the arrows presents the true circulating direction of the current through the circuit. Figure 3 shows the main converter waveforms.

Initially, before  $\theta = \theta_1$ , the  $g_{p1}$  and  $g_{s1}$  signals are set low. The  $T_{p1a}$ ,  $T_{p2}$ ,  $T_{s1a}$  and  $T_{s2}$  transistors are enabled.  $V_{gp}^{ref}$  voltage are applied between the points  $p_1$  and  $p_2$  and  $V_{gs}$  are applied between the points  $s_1$  and  $s_2$ . Since these voltages have the same value, the voltage on the auxiliary inductors are null and, hence, the current on the transformer windings does not vary. Therefore, the primary and secondary side sources current does not vary either.

*First topological state:* At  $\theta = \theta_1$ ,  $g_{p1}$  signal is set high,  $T_{p1a}$  and  $T_{p2}$  transistors are disabled and  $T_{p1}$  and  $T_{p2a}$  transistors are enabled. The  $C_{gp}$  voltage,  $V_{gp}^{ref}$ , are applied between the points  $p_2$  and  $p_1$ . The voltage  $V_{gp}^{ref} + V_{gs}$  are divided equally between the auxiliary inductors. The primary side winding currents increase with the same rate since the voltage over auxiliary inductors are equal but the source current,  $i_p$ , does not change for the same reason. On the other hand, the secondary side windings currents decrease with the same rate but still, the secondary side source current,  $i_s$ , does not vary. Figure 4(a) shows the converter circuit with the current direction indication immediately after the change in  $g_{p1}$  state.

*Second topological state:* At  $\theta = \theta_2$ ,  $g_{s1}$  signal is set high,  $T_{s1a}$  and  $T_{s2}$  transistors are disabled and  $T_{s1}$  and  $T_{s2a}$  transistors are enabled. The voltage  $V_{gs}$  are applied between the points  $s_2$  and  $s_1$ . The voltage  $V_{gp}^{ref} - V_{gs}$  are null, consequently, the voltage across the auxiliary inductors is also null. Therefore, primary and secondary windings currents do not vary, nor do the primary and secondary side sources current. Figure 4(b) depicts the converter circuit with the current direction

indication during this topological state.

*Third topological state:* At  $\theta = \theta_3$ ,  $g_{p1}$  signal is set low,  $T_{p2a}$  and  $T_{p1}$  transistors are disabled and  $T_{p2}$  and  $T_{p1a}$  transistors are enabled. The voltage  $V_{gp}^{ref}$  are applied between the points  $p_1$  and  $p_2$ . The voltage  $-V_{gp}^{ref} - V_{gs}$  are divided equally between the auxiliary inductors, similarly as in the first topological state. The primary side winding currents decrease with the same rate since the voltage over auxiliary inductors are equal but the source current,  $i_p$ , does not change for the same reason. On the other hand, the secondary side windings currents increase with the same rate but still, the secondary side source current does not vary. Figure 4(c) shows the converter circuit with the current direction indication immediately after the change in  $g_{p1}$  state.

*Fourth topological state:* At  $\theta = \theta_4$ ,  $g_{s1}$  signal is set low,  $T_{s2a}$  and  $T_{s1}$  transistors are disabled and  $T_{s2}$  and  $T_{s1a}$  transistors are enabled. The voltage  $V_{gs}$  are applied between the points  $s_1$  and  $s_2$ . The voltage  $-V_{gp}^{ref} + V_{gs}$  are null, consequently, the voltage across the auxiliary inductors also is null. Therefore, primary and secondary windings currents does not vary, nor do the primary and secondary side source currents. Figure 4(d) depicts the converter circuit with the current direction indication during this topological state. After this point,  $g_{p1}$  signal will be set high, ergo, a complete switching period has been described.

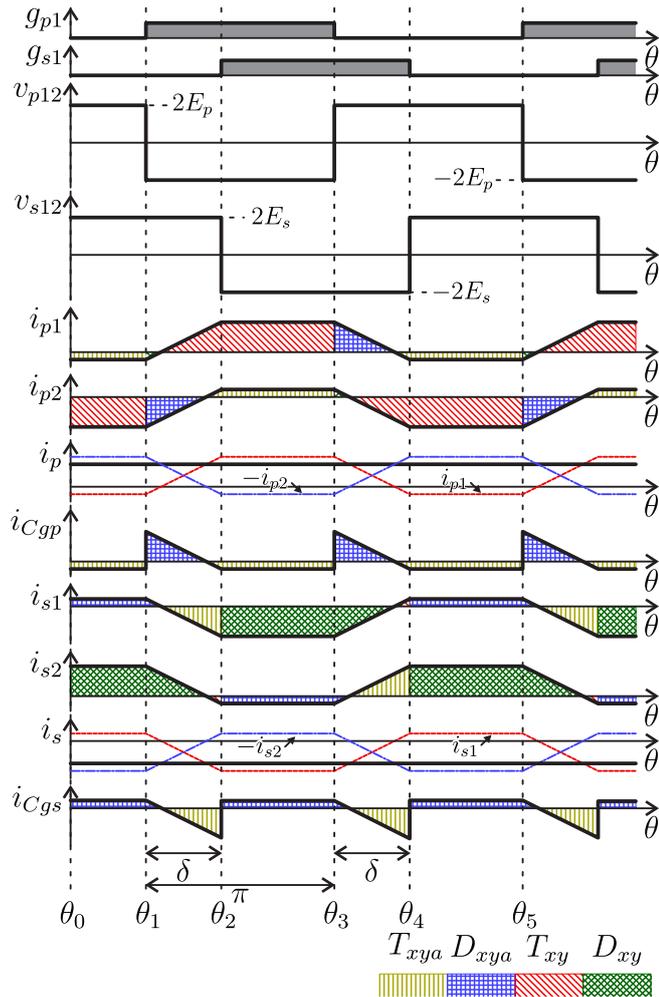


Fig. 3. Main theoretical waveforms of the converter.

### III. QUANTITATIVE ANALYSIS

In this section, the equation that determines the power transferred by the converter as function of the angle  $\delta$  is deduced. For this purpose, it is considered that all power delivered from the source  $E_p$  to the transformer will be transferred to the secondary side source  $E_s$ , hence, if this value is known, the power processed by converter is also known. The power transferred by the transformer depends on the voltages applied over its windings and the current that flows through them. The winding voltages and currents can be rewritten as a combination of two components: common mode and differential mode. The common mode components do not transfer energy through the transformer since the common mode current component in one winding cancels the magnetic flux created by the other. In addition, the common mode voltage across one winding nullifies the magnetomotive force produced by the other. Consequently, the power transferred by the transformer depends only on the differential mode components. The primary and secondary windings differential mode voltages components are equal to the voltages  $v_{p12}$  and  $v_{s12}$ , respectively. The differential mode equivalent circuit from transformer terminals pointview and its referred to the secondary side are presented in Figure 5. From this circuit, the following equation can be derived:

$$i_{sd}(\theta_n) = i_{sd}(\theta_{n-1}) + \frac{av_{p12} - v_{s12}}{4\omega_s l_s} (\theta_n - \theta_{n-1}). \quad (1)$$

The average value of  $i_{sd}$  current over one switching period can be calculated by:

$$\langle i_{sd} \rangle = \frac{1}{2\pi} \sum_{n=1}^4 \frac{(i_{sd}(\theta_n) + i_{sd}(\theta_{n-1})) (\theta_n - \theta_{n-1})}{2}. \quad (2)$$

Considering that  $i_{sd}(\theta_4)$  is equal to  $i_{sd}(\theta_0)$  and the average value of  $i_{sd}$  current null, (2) becomes:

$$\sum_{n=1}^4 i_{sd}(\theta_n) = 0. \quad (3)$$

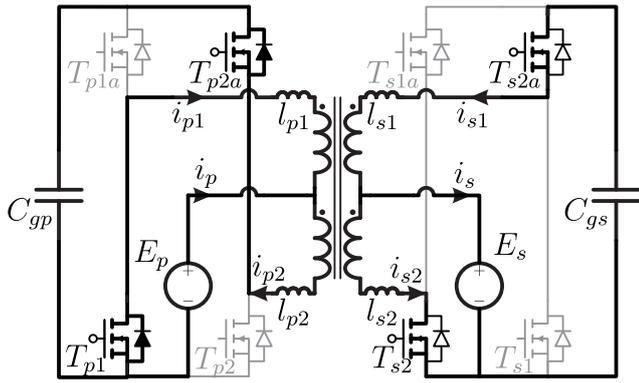
The linear system in (4) is obtained by associating (1) and (3). By solving it, the instantaneous value of the  $i_{sd}$  in each transistor switching instant is determined.

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{sd}(0) \\ i_{sd}(\delta) \\ i_{sd}(\pi) \\ i_{sd}(\pi+\delta) \end{bmatrix} = \begin{bmatrix} \frac{(-aE_p + E_s)\delta}{2l_s\omega_s} \\ \frac{(-aE_p - E_s)(\pi-\delta)}{2l_s\omega_s} \\ \frac{(aE_p - E_s)\delta}{2l_s\omega_s} \\ 0 \end{bmatrix} \quad (4)$$

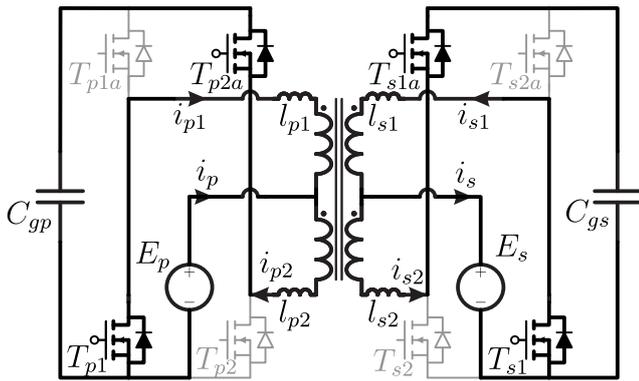
The average power of the converter over one switching period is calculated by:

$$\langle p \rangle = -\frac{1}{2\pi} \int_0^{2\pi} v_{s12} i_{sd} dt. \quad (5)$$

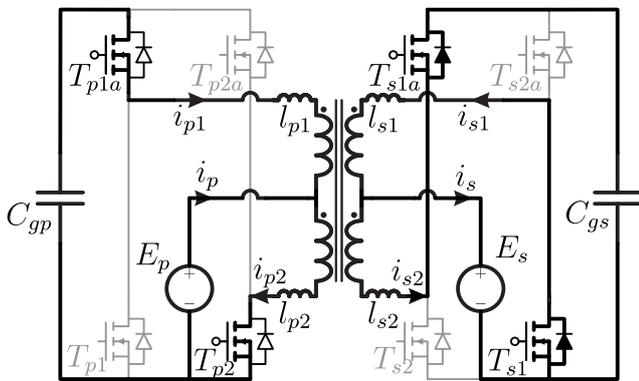
Considering the  $v_{s12}$  and  $i_{sd}$  waveforms, the integral in (5) is simplified to a summation and the result is:



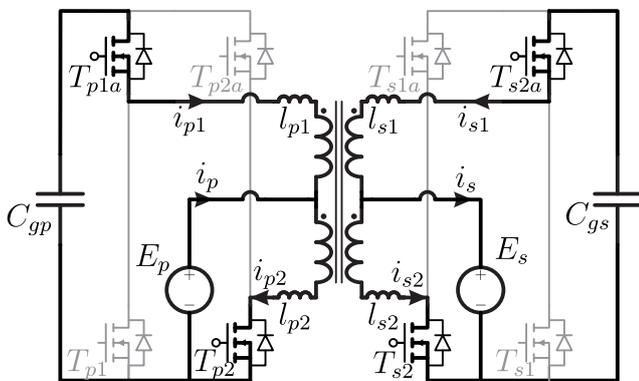
(a)



(b)



(c)



(d)

Fig. 4. (a) First topological state, (b) second topological state, (c) third topological state and (d) fourth topological state.

$$\langle p \rangle = -\frac{1}{2\pi} \sum_{n=1}^4 v_{s12(n)} \frac{i_{sd}(\theta_n) + i_{sd}(\theta_{n-1})}{2} \quad (6)$$

$$\langle p \rangle = \frac{aE_p E_s}{\omega_s l_s} \frac{\delta(\pi - \delta)}{\pi} \quad (7)$$

Equation (8) is obtained dividing both sides of (7) by  $E_s$ . This equation denotes that for a fixed value of  $E_p$ ,  $\langle i_s \rangle$  can be solely adjusted by the angle  $\delta$ , therefore, the converter equivalent circuit from the secondary side source terminals is a controlled current source.

$$\langle i_s \rangle = \frac{aE_p}{\omega_s l_s} \frac{\delta(\pi - \delta)}{\pi} \quad (8)$$

The normalized value of  $\langle i_s \rangle$  is determined by (9). This characteristic is plotted in Figure 6. It can be verified that for an angle between  $-45^\circ$  and  $45^\circ$ , the  $\langle i_s \rangle$  value varies almost linearly with  $\delta$  and for values outside of this range, the curve inclination drastically declines. In case of this converter being employed to interface two voltage sources, these features can be used to simplify the control of one of the source currents.

$$\langle \bar{i}_s \rangle = \frac{\delta(\pi - \delta)}{\pi} \quad (9)$$

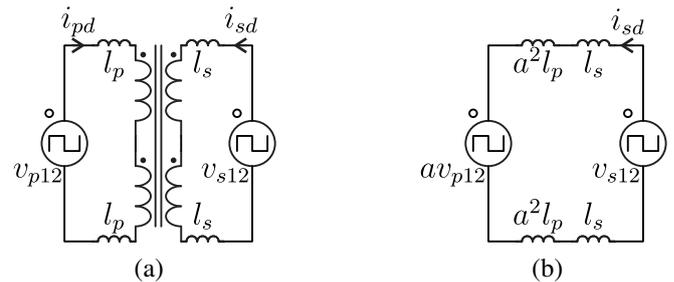


Fig. 5. Differential mode equivalent circuit (a) from transformer terminals pointview and (b) referred to the secondary side.

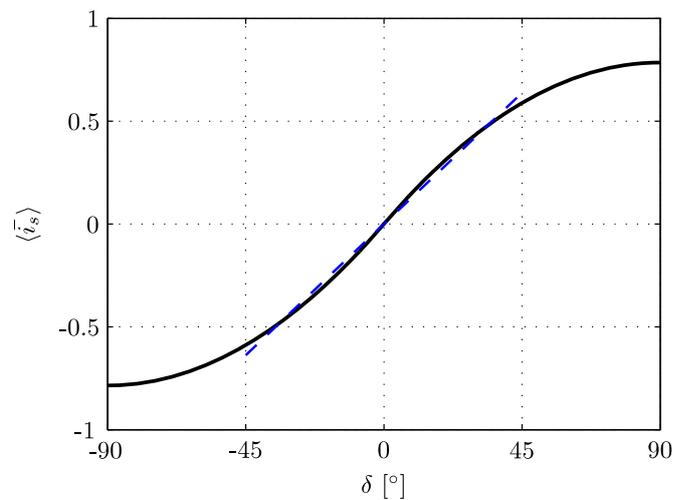


Fig. 6. Normalized secondary side source current versus phase-shift angle.

#### IV. SIMPLIFIED DESIGN EXAMPLE

A design example is demonstrated in this section. The specification of the converter is given by Table I.

**TABLE I**  
**Design Example Specifications**

Parameter	Symbol	Value
Maximum Output Power	$\langle p \rangle$	600 W
Primary Side Source Voltage	$E_p$	14 V
Secondary Side Source Voltage	$E_s$	42 V
Switching Frequency	$f_s$	50 kHz
Phase-Shift Angle	$\delta$	0.489 rad (28°)

The transformer secondary-primary turns ratio  $a$  is determined by:

$$a = \frac{E_s}{E_p} \quad (10)$$

$$a = \frac{42}{14} = 3.$$

The secondary-side auxiliary inductor inductance is obtained isolating  $l_s$  in (7) and replacing the specifications on Table I into it. The result is:

$$l_s = \frac{aE_pE_s}{\omega_s \langle p \rangle} \frac{\delta(\pi - \delta)}{\pi}$$

$$l_s = \frac{3 \cdot 14 \cdot 42}{2\pi \cdot 50 \cdot 10^3 \cdot 600} \frac{0.489(\pi - 0.489)}{\pi} = 3.86 \mu\text{H}. \quad (11)$$

The primary-side auxiliary inductor inductance is determined by:

$$l_p = \frac{l_s}{a^2} \quad (12)$$

$$l_p = \frac{3.86 \cdot 10^{-6}}{3^2} = 429 \text{ nH}.$$

The maximum voltage over one-side transistors are twice the value of the source voltage of this side, hence, the primary side transistors have to withstand, at least, 28 V and the secondary side ones have to sustain 84 V. The clamping capacitor minimum rated voltage also has to be these values.

In order to validate the design presented in this section and the theoretical waveforms shown at section II, a simulation of the designed converter operating at rated power was realized. The clamping capacitor capacitance was chosen to be 40  $\mu\text{F}$  for primary side and 10  $\mu\text{F}$  for secondary side. Figure 7 shows the source current and clamping capacitor voltage waveforms. The primary and secondary source currents waveforms show a ripple of 6.77 % and 3.13 %, respectively, opposing the expected results based on section II assumptions. This occurs due to the voltage over the clamping capacitor, which was considered ripple free in section II, have a considerable value, namely 3.41 % for the primary and 1.55 % for the secondary side voltage, due to the clamping capacitor capacitance value

is not sufficiently high. Nevertheless, the obtained current ripple is reasonable small.

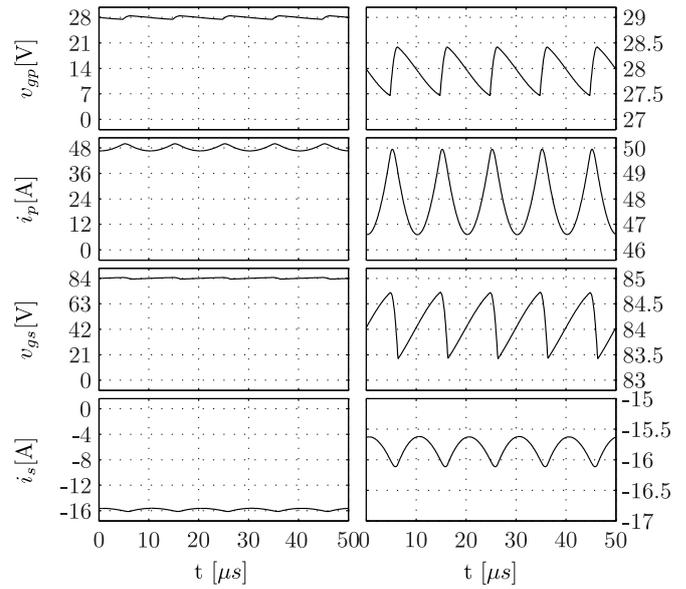


Fig. 7. Source current and clamping capacitor voltage waveforms obtained through simulation.

#### V. DESIGN EXAMPLE COMPARISON BETWEEN DPP AND DAB CONVERTER

A comparison between the proposed converter and the DAB converter are presented in this section regarding, especially, component current stress. Both converters are designed to meet the specifications given by Table I, e.g. same power, source voltage and switching frequency, hence, the example design presented in section IV is used.

The employed modulation strategy in the DAB case are the single phase-shift modulation and the expressions used to design it are presented in [35]. In practice, a capacitor could be sufficient to filter the DAB converter current but, in this case, the cable which connects the source to capacitor works as an inductor due its parasite inductance. In other words, indirectly, a LC filter is employed. Also, if this inductance is very low, a non-negligible portion of the current ripple may still circulate through the voltage source because of the capacitor impedance is not purely capacitive and may not be sufficiently low.

Hence, in order to account this effect, a LC filter for each side will be considered in addition to the DAB topology as shown in Figure 8. Therefore, in both cases, a capacitor is needed for each side. Filter capacitors for DAB and clamping capacitors for DPP. Theoretically, DPP  $i_p$  and  $i_s$  currents does not have current ripple and, therefore, it does not requires current filter.

These capacitors capacitance values are adjusted to store the same energy, although with different voltage and current specifications, theoretically, they will show the same size.

The filter resonance frequency is adjusted to one fifth of the switching frequency. Table II shows the component specification for each of the converter design. The current stress is obtained by means of simulation. Additionally, the semiconductors RMS current value normalized by the source

current average value are also displayed.

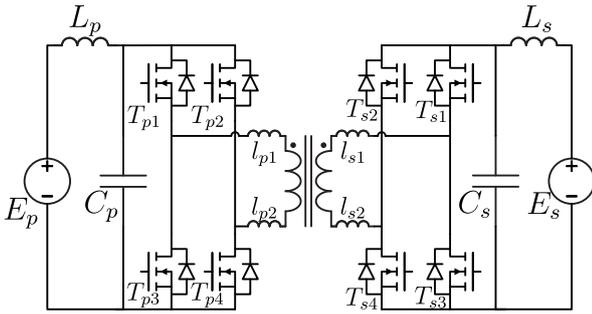


Fig. 8. Dual active bridge circuit.

**TABLE II**  
**Component Specifications Comparison Between Design**  
**Examples of A DAB And The Proposed Converter**

Sym.	Physical Quantity	DAB		DPP	
		$\alpha$	$\alpha$	$\alpha$	$\alpha$
		$p$	$s$	$p$	$s$
$E_\alpha$	Voltage (V)	14	42	14	42
	Current (A)	45	14.3	45.6	14.8
$C_{g\alpha}$	Rated Voltage (V)	14	42	28	84
	RMS current (A)	22.1	8.2	11.5	4.2
$C_\alpha$	Capacitance ( $\mu\text{F}$ )	160	40	40	10
	Accumulated Energy (mJ)	15.7	35.3	15.7	35.3
$L_\alpha$	Number of Inductors	1		-	
	Inductance ( $\mu\text{H}$ )	1.58	6.33	-	
	Maximum Current (A)	47.9	15.7	-	
	Accumulated Energy (mJ)	1.82	0.78	-	
$l_{\alpha k}$	Number of Inductors	4		-	
	Inductance ( $\mu\text{H}$ )	0.10	0.89	0.40	3.55
	Maximum Current (A)	57.5	19.2	53.4	17.6
	Accumulated Energy ( $\mu\text{J}$ )	163	163	562	551
$T_{\alpha k}$	Number of switches	4		2	
	Rated Voltage (V)	14	42	28	84
	RMS current (A)	37.5	12.5	35.0	11.5
	Normalized RMS current	0.79	0.80	0.73	0.73
	Turn On Current (A)	-43.5	-19.2	-4.3	-17.8
	Turn Off Current (A)	50.6	18.0	53.1	2.2
$T_{\alpha k a}$	Number of switches	-		2	
	Rated Voltage (V)	-		28	84
	RMS current (A)	-		6.9	2.8
	Normalized RMS current	-		0.19	0.17
	Turn On Current (A)	-		-53.1	-2.2
	Turn Off Current (A)	-		4.3	17.8

DAB and DPP main switches have to withstand about the same normalized RMS current and the DPP auxiliary switches have to sustain just a quarter of this value, however, DAB has a total of eight main switches while DPP has just four, hence, if the same transistors are employed in both designs, the proposed converter will present a lower conduction loss value than the DAB. Nonetheless, the maximum voltage across the proposed converter switches is twice that of the source voltage

while DAB switches have to sustain just the source voltage.

MOSFET on-state resistance is a composite by several terms related to material resistances. For higher rated voltage MOSFET, more than 100 V, this characteristic is predominantly influenced by a term that varies as a function with the breakdown voltage [36]. For lower rated voltage MOSFET, less than 100 V, this term is not that considerable and this property is majorly dependable on constant terms. For instance, considering the following International Rectifier MOSFETs with same package and similar current specifications: IRL3103, IRFZ44VZ, IRFB4227 and IRFB4510. The first two transistors have the same drain-source resistance, 12 m $\Omega$ , but its drain-to-source breakdown voltage are 30 V and 60 V, respectively. On the other hand, IRFB4510, a 100 V drain-to-source breakdown voltage MOSFET, has a drain-source resistance of 10.7 m $\Omega$  while IRFB4227, a 200 V drain-to-source breakdown voltage MOSFET, has a drain-source resistance of 19.7 m $\Omega$ . Therefore, for low voltage applications, the proposed converter will present a lower conduction loss even if higher rated voltage MOSFET is employed.

The total energy accumulated on inductors is 3.25  $\mu\text{J}$  for DAB and 2.23  $\mu\text{J}$  for the proposed converter. Considering that the magnetics size is proportional to the stored energy, overall DAB magnetics will be bulkier than the DPP. Also, although both converter circuits are shown with four auxiliary inductors, these inductances can be concentrated to one of the transformer sides and this number can be reduced to one in DAB case and two for the proposed converter. Therefore, including the two DAB filter inductors, DAB requires a total of three inductors and the proposed converter just two, thereby, DPP converter presents an inferior magnetic component count.

## VI. EXPERIMENTAL RESULTS

A prototype was built with specifications presented in section IV. The corresponding component parameters are given in Table III.

Auxiliary inductors were connected in series just to the secondary side winding and its inductance value was adjusted to be equal to twice the former calculated value minus half the transformer leakage inductance. Figure 9 presents a photograph of the laboratory prototype. In this figure is presented the auxiliary power supply, control circuit and power circuit stage, and components used in the setup are described in Table III.

Figure 10 shows the current and voltages waveforms of the primary and secondary sources for converter operating with  $\delta$  equal to 26.4°, that is, transferring power from primary side source to the secondary side one. Primary side source current waveform shows no ripple as operating principle analysis predicted. On the other hand, secondary source current does display some ripple. This occurs due to differences between the secondary side winding currents. If these current waveforms do not have the same shape, the perfect ripple cancellation at the composition of the source current does not succeed. These differences can be generated due to inaccurate gate signals and uneven winding inductance.

**TABLE III**  
**List of Prototype Component Parameters**

Component	Description
Secondary-primary turns ratio	$a = 3$
Transformer leakage inductance	$l_o^{ref} = 2.02\mu\text{H}$
Auxiliary secondary inductors	$l_{s1} = 4.95\mu\text{H}, l_{s2} = 5\mu\text{H}$
Transistors	$T_{p1}, T_{p2}, T_{p1a}, T_{p2a}$ : AUIRFB8409: 40V/197A $T_{s1}, T_{s2}, T_{s1a}, T_{s2a}$ : AUIRFB4410: 100V/75A
Clamping capacitors	Type: Polypropylene EPCOS: B32674, $C_c = 10\mu\text{F}$ $C_{gp} = 4 \cdot C_c, C_{gs} = C_c$

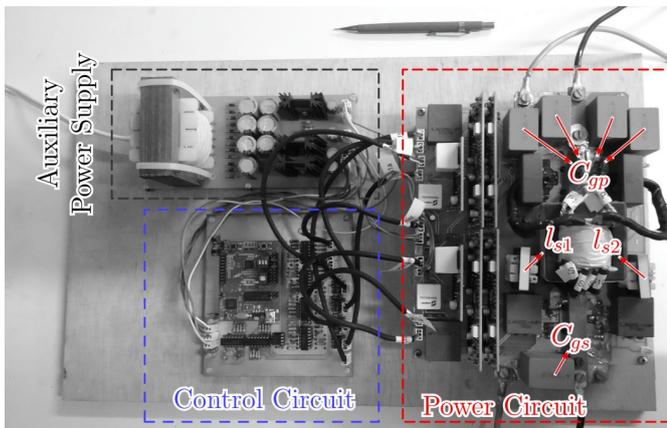


Fig. 9. Photograph of the laboratory prototype.

The primary and secondary side bridge voltages and the secondary winding currents AC component waveforms are shown in Figure 11. The  $v_{p12}$  and  $v_{s12}$  waveforms have similar shapes but  $v_{s12}$  is delayed in relation to  $v_{p12}$ . The secondary winding currents waveform shapes also are similar and agree well with the operation principle analysis presented in section II but its amplitudes differ, which, as mentioned before, generate ripple in the secondary source current.

Figure 12 shows the primary side source current transient to a trapezoidal shape phase-shift angle reference waveform. Initially,  $\delta$  and  $i_p$  are positive, hence, power is delivered from the primary side source to the secondary side one. At instant 0.6 ms,  $\delta$  starts to decrease down to  $-28^\circ$  and the  $i_p$  current follows a similar behavior. Nearly at instant 0.7 ms, both values are negative, hence, power is transferred from the secondary side source to the primary side one, i.e., the power processed by the converter changed its direction. Posteriorly,  $\delta$  starts to increase up to  $28^\circ$  and  $i_p$  current, as above, follows a resembling pattern. At instant 1.5 ms,  $i_p$  becomes positive, therefore, converter power direction is restored to its former state. The maximum current value in one direction of the power flow compared with to another one is slightly different, due to the experimental setup to test the reversible operation. The converter is supplied by a voltage source at the primary side but at secondary side a high value capacitive load associated with a resistor is used to emulate a voltage source. The load voltage when referred to primary side is lower due to the converters losses. Therefore, the primary current is lower

when power flow is reversed, as shown in Figure 12.

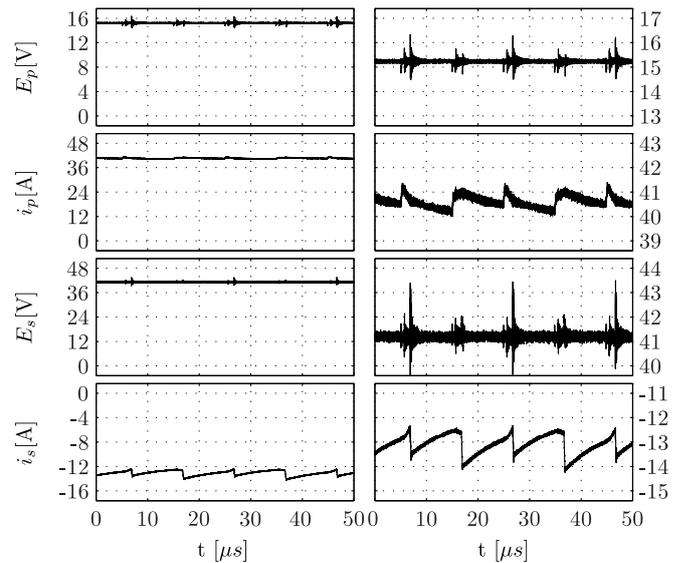


Fig. 10. Experimental voltages and currents waveforms of primary and secondary sources for  $\delta$  positive.

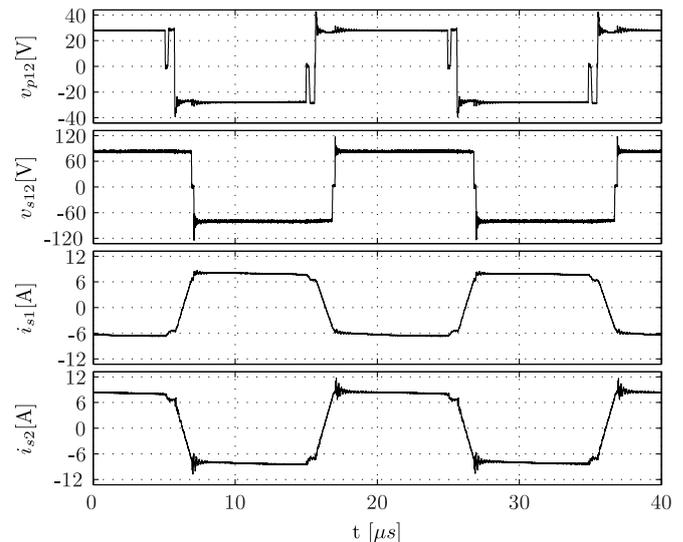


Fig. 11. Primary and secondary bridges voltage and secondary windings current AC component waveforms.

Figure 13 depicts the converter efficiency curve. Positive values of  $P$  denotes that power is delivered to the secondary side source and negative values represent that power is delivered to the primary side source. The maximum efficiency is 94.7 % and it occurs at 263 W when the converter delivers power from the primary side source to secondary side one. By observing this curves shape, it can be inferred that the converter shows a high conduction losses since the maximum efficiency occurs at less than half of the rated power. These experimental results were obtained in close looping control.

Figure 14 illustrates a comparison of the calculated losses, the estimated losses, based on the ratio between temperature rising value of the converter components and its thermal resistance, and the total losses experimentally measured when the converter processes 500 W from the primary side source to the secondary side source. Analytically obtained

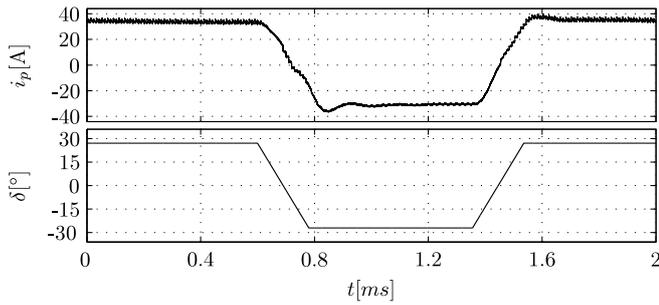


Fig. 12. Experimental result for the transient response of the converter to a trapezoidal phase-shift angle ( $\delta$ ), demonstrating the bidirectional power flow capability.

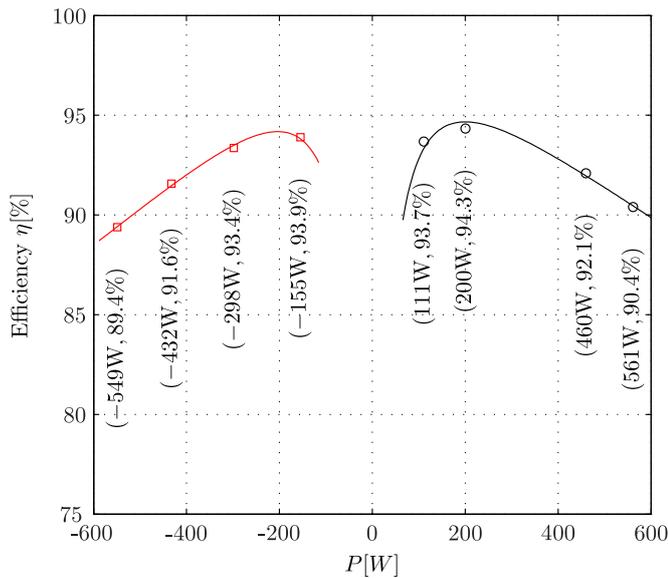


Fig. 13. Efficiency curves versus load power.

semiconductor losses shows that switching losses is about twice its conduction loss value. This high switching loss can be decreased by employing a more suited gate driver than the available used one. Calculated magnetics components losses agreed well with the estimated values. On the other hand, calculated semiconductor losses values are underestimated compared with the estimated transistor losses by a margin of about 10 W. Lastly, the estimated total loss is quite similar to the measured value and the discrepancy between the calculated and measured losses is actually lower than the presented since losses caused by parasitic resistances in PCB and connectors are not counted.

Figure 15 shows a comparison between the theoretical  $\langle \bar{i}_s \rangle$  versus  $\delta$  curve and experimental data. The experimental data differs from the theoretical curve by a considerable margin but if the converter efficiency is accounted into theoretical curve, this margin greatly diminishes, especially for larger phase-shift angle values.

## VII. CONCLUSION

The bidirectional dual active clamping Push-Pull dc-dc converter was addressed in this paper, with the intention to apply it in the control of the power flow between the sources of the dual low voltage systems. From the theoretical analysis

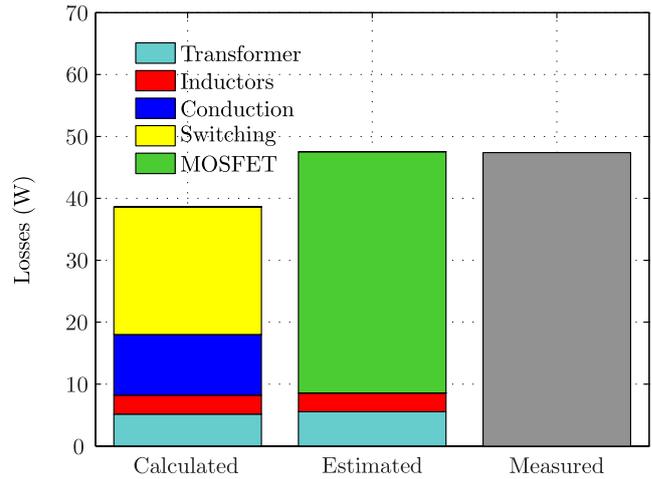


Fig. 14. Comparison between calculated and estimated losses and measured converter total loss.

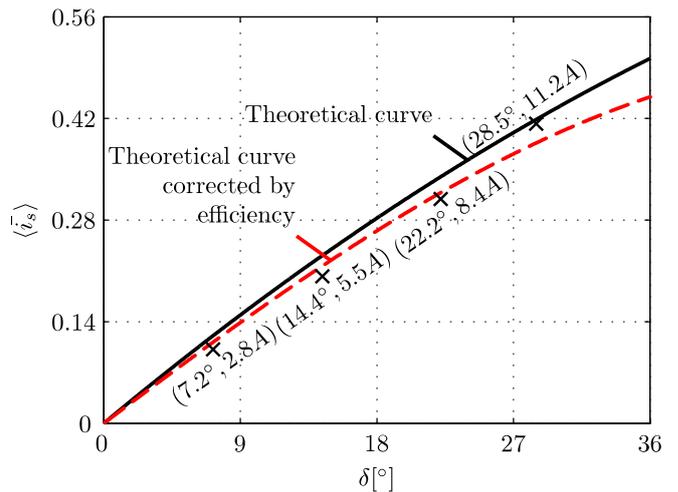


Fig. 15. Normalized  $i_s$  current versus  $\delta$  compared with experimental results.

and experimental studies conducted in the laboratory, it was possible to draw the following conclusions.

The experimental results agreed well with the results predicted in the analysis.

Both the input and output current ripple, which are severe problems in low voltage and high current applications, are lower in comparison with the conventional isolated bidirectional dc-dc converters, such as the DAB family.

It was demonstrated that even by employing higher rated voltage MOSFET, the proposed converter may present lower conduction loss than DAB converter for low voltage applications.

Compared with DAB filter and auxiliary inductors, the total size of the proposed converter auxiliary inductors can be smaller and a lower number of them is necessary.

The derived equations may be used to design a converter to comply with different specifications and applications.

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