A TRANSFORMERLESS COMMON-GROUND TWO-SWITCH SINGLE-PHASE INVERTER FOR BATTERY ENERGY STORAGE SYSTEM APPLICATIONS

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***Abstract* – This paper proposes a transformerless common-ground single-phase inverter for battery energy storage system (BESS) applications. With regard to conventional converters operating as a voltage source inverter (VSI), the proposed converter offers the advantage of a common connection between the battery bank negative terminal and the ground. Hence, the common-mode voltage becomes continuous while common-mode currents flowing through parasitic capacitances located between the battery bank and the grounded metallic frame are eliminated, allowing operation without a transformer. This new topology has only two power semiconductors, two inductors and one capacitor, without the need for a filter on the AC grid side. The converter operation is described and the relevant equations for sizing are presented along with the main characteristics. A 1 kW non-optimized prototype was dimensioned, built and tested to validate in practice the theoretical analysis, and a maximum efficiency of 95.25% was obtained. Due to the simplicity, low number of active components, no clamping circuit requirement and the common-ground, this topology is a very interesting option for the above-mentioned application.**

***Keywords* – Battery energy storage system, Common-ground inverter, Leakage current, Parasitic capacitance, Transformerless inverter.**

NOMENCLATURE

α	V_{opk} to V_1 ratio.
$\Delta i_{L1,2}$	Peak-to-peak current ripple in inductors L_1 and L_2.
$\overline{\Delta i_{L1,2max}}$	Maximum parameterized ripple in inductors L_1 and L_2.
$\Delta v_{C1,f}$	Peak-to-peak voltage ripple in capacitors C_1 and C_f.
ω_f	Filter cutoff angular frequency.
$C_{n,p}$	Parasitic capacitor between negative or positive DC source terminal and ground.
d	Duty cycle.
f_f	Filter cutoff frequency.
f_g	Grid frequency.
f_s	Switching frequency.
$i_{L1,2}$	Instantaneous current in inductors L_1 and L_2.
i_{L1pk}	Peak value of current in inductor L_1.
I_{L2}	Quasi-instantaneous mean current in inductor L_2.
I_{opk}	Peak value of the output current.
I_{orms}	Output current RMS value.
i_{Ro}	Current in the resistive load.
$I_{S1,2rms}$	Current in power switches S_1 and S_2 RMS values.
i_1	Instantaneous input current without LC filter.
L_{eq}	Equivalent inductance.
P_o	Output power.
$R_{L,DSon}$	Resistances in the inductors and the transistors.
$S_{1,2}$	Power switches.
T_s	Switching period.
v_{C1}	Voltage across capacitor C_1.
V_{C1max}	Maximum voltage across capacitor C_1.
v_o	Output voltage or grid voltage.
V_{opk}	Peak value of the output voltage.
V_{Smax}	Maximum voltage across the semiconductors.
V_1	Battery bank voltage.

I. INTRODUCTION

The development of renewable energy sources and storage systems is based on inverters connected to the electrical grid without galvanic isolation to reduce costs and increase system efficiency [1]-[6]. Conventional inverter topologies without a transformer are not suitable for this type of application due to common-mode voltages and leakage currents [1], [2].

The schematic in Figure 1 shows the voltage between the negative DC source terminal and the grid ground point is dependent on the voltage across the switches. The high switching frequency of semiconductors in a three-level modulation, for example, causes a high frequency common-mode voltage, which generates a significant leakage current through the parasitic capacitances. This current is proportional to the common-mode voltage variation, its frequency, and the parasitic capacitance values.

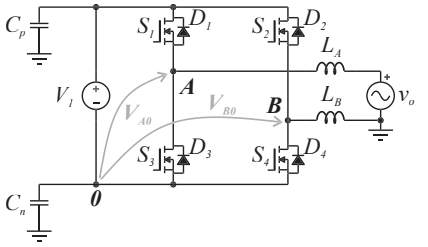

Fig. 1. Classic full-bridge inverter used to connect a DC power source to the grid.

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Topologies with galvanic isolation prevent the occurrence of this leakage current. However, they increase costs and reduce by over 2% the efficiency of the converter [2], [3]. Transformerless converters allow a cost reduction of around 25% [2]. Several non-isolated inverter topologies have been proposed to mitigate or reduce leakage currents in grid-tied applications [6]. The first converters were based on two known converter families: H-bridge and neutral point clamped (NPC) [3].

Basically, the new converter structures can be categorized as: common-mode voltage clamping, disconnection during the freewheeling modes or common-ground. Common-ground topologies have gained importance since other techniques do not eliminate the leakage current completely and the principle of these topologies is shown in Figure 2 [7]-[10].

The leakage current problem has generally been addressed with regard to photovoltaic systems [1]-[16]. In the photovoltaic modules, the parasitic capacitances are between the terminals and the grounded metal frame. These capacitances are charged and discharged with the common-mode voltage frequency, possibly causing significant leakage current.

A recurrent concern of the manufactures is that the leakage current can be extremely harmful, compromising the performance of photovoltaic distributed generation systems [11]. The modules are grounded through their metallic frame. This frame structure and other factors, such as the cell and panel manufacturing methods, cell surface area, distance between the cells and climatic conditions, affect the parasitic capacitance value [12].

Safety aspects are affected by the presence of a leakage current, generating unsafe operation conditions and the risk of electric shock, and additional negative factors include: a reduction in the quality of the electrical energy generated, the appearance of electromagnetic interference (EMI), increases in the total harmonic distortion (THD) and system losses, and the possible occurrence of a trip in the ground-fault protection devices [2], [7], [17].

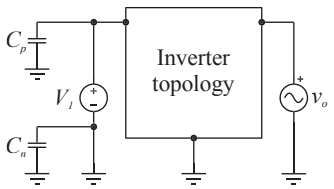


Fig. 2. Common-ground inverter principle.

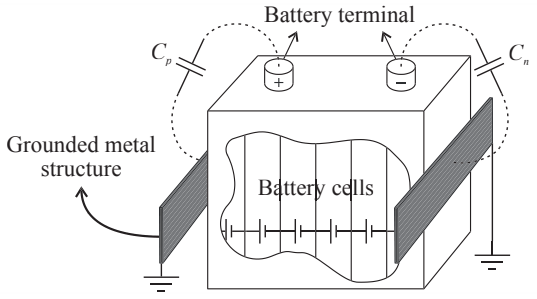
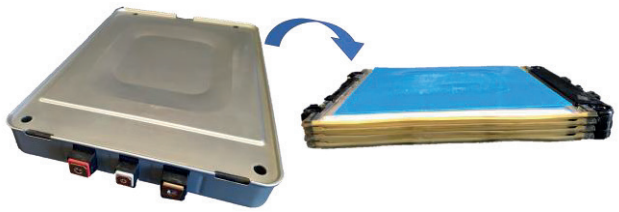


Fig. 3. Parasitic capacitances present in battery applications.



(a) (b)

Fig. 4. Nissan Leaf lithium ion battery module: (a) with the frame and (b) just the cells.

Similarly, but less frequently addressed in the literature, batteries also have parasitic capacitances between their terminals and the grounded frame, as seen in Figure 3.

A parasitic capacitance is created when part of the grounded metallic structure is overlapped and parallel to the electrodes that build the battery cells. So, for example, if the entire frame of a battery is metallic and the battery is grounded, the whole electrode area will form a parasitic capacitance with the frame.

According [18] and [19], capacitance is proportional to the area formed by two overlapped surfaces perpendicular to each other and inversely proportional to the distance between them. Consequently, a battery bank expansion leads to an increase in the parasitic capacitance value.

The parasitic capacitance present in a 10 MWh lead acid battery bank was estimated as 1.54 μF in [18]. Nonetheless, as mentioned in the same publication, $LiFePO_4$ batteries are ideal for BESS applications.

The lithium ion and nickel metal hydride technologies are the main chemical elements in electric or hybrid vehicle applications [20]. In addition, retired vehicle batteries do not need to be recycled directly, which involves a lot of effort and waste [21]. The reuse of these batteries is referred to as second life.

With a low cost compared to the first life, second life batteries tend to represent a large part of stationary battery applications. Therefore, to ascertain the parasitic capacitance of this type of battery, the value for this parameter was measured for retired lithium-ion batteries originating from a Nissan Leaf vehicle. Each module has a nominal voltage of 7.6 V, capacity of 64 Ah and total parasitic capacitance of approximately 1 nF. This module has a metallic casing and is formed by four cells, as shown in Figure 4.

Herein, a single-phase transformerless inverter topology to connect a stationary battery bank to the power grid is presented and analyzed. Its main attribute with respect to conventional topologies is the connection between the negative battery bank terminal and the grid neutral point, which is grounded, and it implies the elimination of the capacitive leakage currents.

II. PROPOSED INVERTER AND OPERATION PRINCIPLE

The proposed inverter power stage is presented in Figure 5, where the battery and the grid have a common ground. Thus, the voltage across the parasitic capacitor C_n is equal to zero while the voltage across the C_p parasitic capacitor is

equal to the battery bank voltage V_1. Accordingly, the common-mode voltage is set to zero and the common-mode currents are eliminated.

Conventional topologies are usually connecting to the grid through an inductor or an LCL filter. Note that the proposed inverter has an output inductor, which can be well designed to meet the requirements of grid connection standards. It is also possible to add an LC pair if the LCL filter is desired.

In order to understand the converter operation, it is initially observed that the grid frequency (f_g), 50 - 60 Hz, is much lower than the power semiconductor switching frequency (f_s), which is usually greater than 20 kHz. It is therefore considered that during a switching period the grid voltage remains constant, which allows it to be analyzed as a DC-DC converter. In a complete switching period, the converter has two topological states, which are illustrated in Figure 6. These are described below for positive output voltage v_o. To simplify the operation description, the case in which the fundamental component of the current i_{L2} is in phase with voltage v_o is analyzed.

Mode 1: According to Figure 6.a, during time interval $(0,d.T_s)$, switch S_1 is turned on while switch S_2 is turned off, since their command signals are complementary. In this topological state, the current in the L_2 inductor increases while the current in the L_1 inductor decreases. The main equations of this mode are given by:

$$L_1 \frac{di_{L1}}{dt}' = -v_{C1} \tag{1}$$

$$L_2 \frac{di_{L2}}{dt}' = V_1 - v_o \tag{2}$$

$$C_1 \frac{dv_{C1}}{dt}' = i_{L1}. \tag{3}$$

Mode 2: During time interval $(d.T_s,T_s)$, shown in Figure 6.), switch S_1 is turned off while switch S_2 is turned on. The .crrent in inductor L_2 decreases while the current in inductor L_1 increases as a function of time. The main equations of this topological state are:

$$L_1 \frac{di_{L1}}{dt}'' = V_1 \tag{4}$$

$$L_2 \frac{di_{L2}}{dt}'' = -v_{C1} - v_o \tag{5}$$

$$C_1 \frac{dv_{C1}}{dt}'' = i_{L2}. \tag{6}$$

Conventional pulse width modulation (PWM) is used, in which the inverter control variable is the duty cycle. It is represented by d in the schematic of the relevant waveforms in Figure 7.

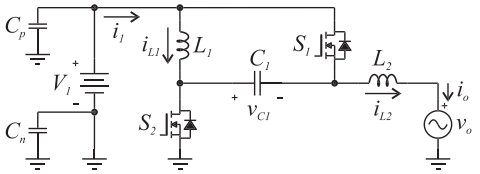


Fig. 5. Proposed converter topology.

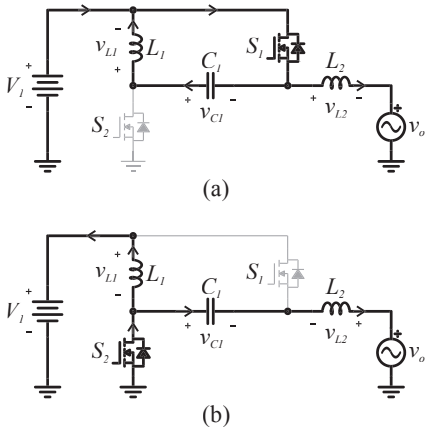


Fig. 6. Topological states for a switching period: (a) time interval $(0,d.T_s)$; and (b) time interval $(d.T_s,T_s)$.

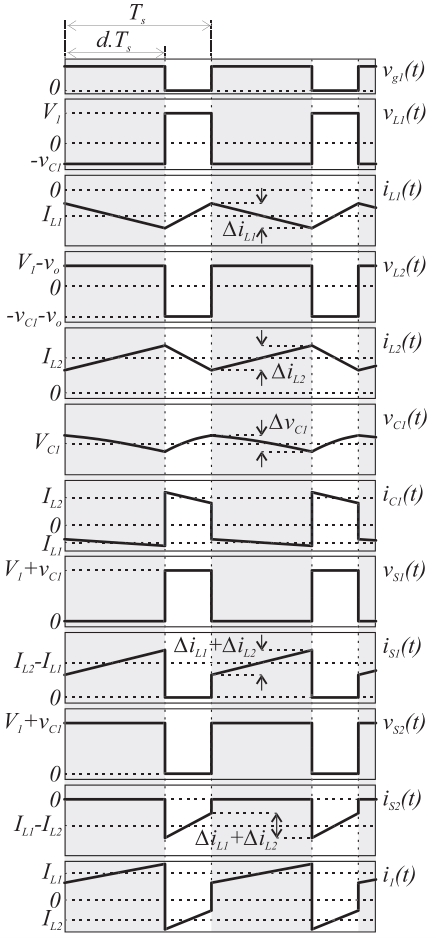


Fig. 7. Ideal waveforms of the proposed converter.

It can be seen that the input current i_1 has presented negative and positive values inside the switching period. Therefore, an input filter becomes necessary and will be discussed further in this article.

III. STEADY STATE ANALYSIS

A. Voltage Gain

The values for the quasi-instantaneous mean voltages in inductors L_1 and L_2 are null in a switching period and are given by (7) and (8), respectively, where $d(t)$ represents the duty cycle.

$$\left\langle v_{L1} \right\rangle_{T_s} = -v_{C1}(\mathrm{t})d(\mathrm{t}) + V_1(1-d(\mathrm{t})) = 0 \tag{7}$$

$$\left\langle v_{L2} \right\rangle_{T_s} = (V_1 - v_o(\mathrm{t}))d(\mathrm{t}) + (-v_{C1}(\mathrm{t}) - v_o(\mathrm{t}))(1-d(\mathrm{t})) = 0\,. \tag{8}$$

Isolating $v_{C1}(t)$ in (7) and substituting in (8), the quasi-instantaneous static gain of the converter is obtained as a duty cycle function. Considering the steady state, the voltage gain can be written as:

$$\frac{v_o}{V_1} = \frac{2d-1}{d}\,, \tag{9}$$

and its behavior can be seen in Figure 8. In this figure, the zero-voltage gain for a 0.5 duty cycle can be observed. This gain is positive for values of > 0.5, with a maximum unit value for d = 1. For values of < 0.5 the gain is negative, reaching unity when d is equal to 1/3. It can be observed that the voltage gain is a non-linear duty cycle function and thus differs from the case of conventional inverters, where this relationship is linear.

Considering a sinusoidal output voltage as follows:

$$v_o(\omega\mathrm{t}) = V_{opk}\sin(\omega\mathrm{t})\,, \tag{10}$$

and starting from (9), the duty cycle is obtained as a function of the output voltage, given by:

$$d(\omega\mathrm{t}) = \frac{V_1}{2V_1 - v_o(\omega\mathrm{t})}\,. \tag{11}$$

Substituting (10) in (11) gives:

$$d(\omega\mathrm{t}) = \frac{V_1}{2V_1 - V_{opk}\sin(\omega\mathrm{t})} = \frac{1}{2-\alpha\sin(\omega\mathrm{t})} \tag{12}$$

where:

$$\alpha = \frac{V_{opk}}{V_1}\,. \tag{13}$$

In Figure 9, the duty cycle is shown as a function of the ωt angle to generate a sinusoidal output voltage.

B. Passive Elements Design

During the second operating state, inductor L_1 is in parallel with input voltage V_1. Thus, the peak-to-peak current ripple is given by:

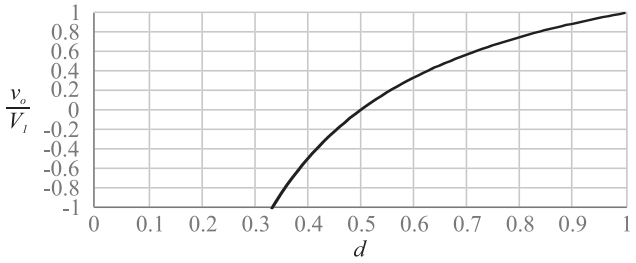


Fig. 8. Voltage gain of the proposed topology.

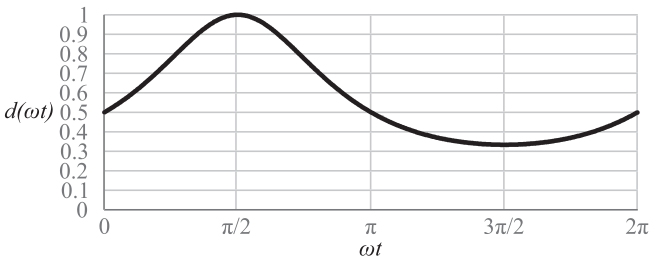


Fig. 9. Modulating signal for a unitary α.

$$\Delta i_{L1}(\mathrm{t}) = \frac{V_1(1-d(\mathrm{t}))T_s}{L_1}\,. \tag{14}$$

The parameterized current ripple is obtained from (14) as follows:

$$\overline{\Delta i_{L1}}(\omega\mathrm{t}) = \Delta i_{L1}(\omega\mathrm{t})\frac{L_1 f_s}{V_1} = 1 - d(\omega\mathrm{t})\,. \tag{15}$$

Similarly, the parameterized current ripple for inductor L_2 is obtained as:

$$\overline{\Delta i_{L2}}(\omega\mathrm{t}) = \Delta i_{L2}(\omega\mathrm{t})\frac{L_2 f_s}{V_1} = \left(1 - \frac{v_o(\omega\mathrm{t})}{V_1}\right)d(\omega\mathrm{t})\,. \tag{16}$$

Substituting (12) into (15) and (16) yields (17). The maximum parameterized ripple for both inductors occurs at $\omega t = 3\pi/2$, as shown in Figure 10, and can be calculated according to (18).

$$\overline{\Delta i_{L1}}(\omega\mathrm{t}) = \overline{\Delta i_{L2}}(\omega\mathrm{t}) = \frac{1-\alpha sin(\omega t)}{2-\alpha sin(\omega t)} \tag{17}$$

$$\overline{\Delta i_{L1max}} = \overline{\Delta i_{L2max}} = \left(\frac{1+\alpha}{2+\alpha}\right). \tag{18}$$

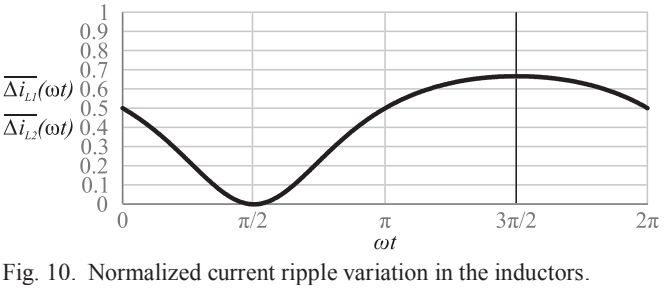


Fig. 10. Normalized current ripple variation in the inductors.

Therefore, the equations for calculating the two inductance values are:

$$L_1 = \frac{V_1}{\Delta i_{L1} f_s}\left(\frac{1+\alpha}{2+\alpha}\right) \tag{19}$$

$$L_2 = \frac{V_1}{\Delta i_{L2} f_s}\left(\frac{1+\alpha}{2+\alpha}\right). \tag{20}$$

The current in capacitor C_1 during the second state is the same as that for inductor L_2. Considering its quasi-instantaneous mean value, the following equation can be found:

$$I_{L2}(\omega t) = C_1 \frac{\Delta v_{C1}(\omega t)}{(1-d(\omega t))T_s}. \tag{21}$$

Rearranging (21), the parameterized voltage ripple is obtained by:

$$\overline{\Delta v_{C1}}(\omega t) = \Delta v_{C1}(\omega t)\frac{C_1 f_s}{I_{L2}(\omega t)} = 1 - d(\omega t). \tag{22}$$

With appropriate algebraic manipulation and considering that the output current i_o is equal to the current i_{L2} for the grid-tied case, the sizing equation for capacitor C_1 is established as:

$$C_1 = \frac{\sqrt{2} I_{orms}}{\Delta v_{C1} f_s}\left(\frac{1+\alpha}{2+\alpha}\right). \tag{23}$$

C. Voltage and Current Stress Analysis

From the expressions that describe the waveforms in Figure 7, the equations of the root mean square (RMS) value of the current in semiconductors of the inverter power stage are obtained. These can be written as (24) and (25), where L_{eq} is an equivalent inductance according to (26).

$$\overline{I_{S1rms}} = \frac{I_{S1rms} L_{eq} f_s}{V_1} = \sqrt{2\overline{I_{orms}}^2 + \frac{\alpha^4 - \frac{7}{2}\alpha^2 + 4}{12\sqrt{\left(4-\alpha^2\right)^5}}} \tag{24}$$

$$\overline{I_{S2rms}} = \frac{I_{S2rms} L_{eq} f_s}{V_1} = \sqrt{\overline{I_{orms}}^2\left(\frac{3}{4}\alpha^2 + 2\right) + \frac{1}{12} - \frac{3\alpha^4 - \frac{35}{2}\alpha^2 + 28}{12\sqrt{\left(4-\alpha^2\right)^5}}} \tag{25}$$

$$L_{Leq} = \frac{L_1 L_2}{L_1 + L_2} \tag{26}$$

The behavior of the parameterized RMS current in S_1 and S_2 as a function of the parameterized RMS output current is shown in Figure 11. It can be noted that the α value has a weak influence on the current in S_1 and the worst case for S_2 occurs for α values close to 1.

Since quasi-instantaneous mean voltage value on each inductor is zero, the maximum voltage value across capacitor C_1, neglecting the high frequency component, which is exceedingly small, is determined by:

$$v_{C1\max} = V_1 + V_{opk}. \tag{27}$$

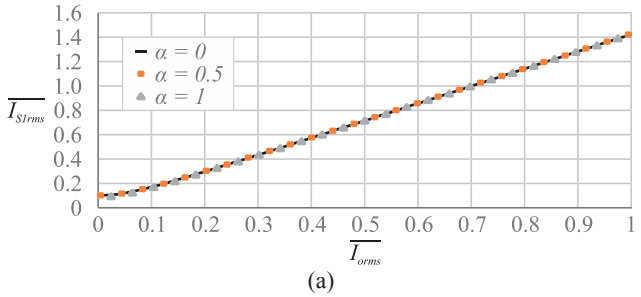
The ideal value of the voltage across the switches is given by:

$$V_{S\max} = 2V_1 + V_{opk}. \tag{28}$$

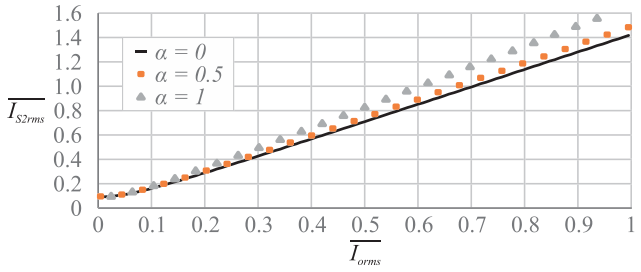
Thus, the semiconductors of this topology are subjected to a much higher voltage than those of a conventional inverter, which is equal to V_1.

D. Input Filter

The high frequency present in the input current is a common issue, as seen in the classic VSI inverters. As is normally done, a filter is inserted between the inverter and the batteries, as shown in Figure 12. The chosen filter can reduce the high frequency harmonics in the batteries.



(a)



(b)

Fig. 11. Parameterized RMS current in the switches as a function of the normalized RMS load current, for different values of α: (a) current in switch S_1; and (b) current in switch S_2.

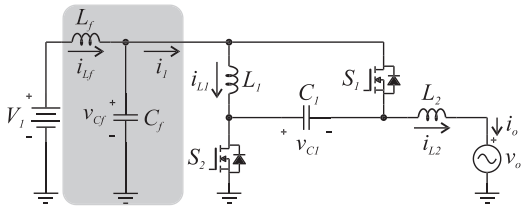


Fig. 12. Schematic showing insertion of LC filter.

Current i_1 is equal to i_{L2} during the time interval of mode 1 and equal to i_{L1} during that of mode 2. The equation that describes i_{L1} can be obtained by analyzing the current in capacitor C_1, since this mean value is zero in steady state. Therefore,

$$\left\langle i_{C1}(\omega t)\right\rangle_{T_s} = i_{L1}(\omega t)d(\omega t) + i_{L2}(\omega t)(1-d(\omega t)) = 0\,. \quad (29)$$

Hence,

$$i_{L1}(\omega t) = -i_{L2}(\omega t)\frac{(1-d(\omega t))}{d(\omega t)}\,. \quad (30)$$

Replacing (12) in (30), for the fundamental component of the current in L_2, (31) is found.

$$i_{L1}(\omega t) = I_{opk}\sin(\omega t)\left[\alpha\sin(\omega t)-1\right]. \quad (31)$$

Thus, current i_1 switches at high frequency between $i_{L1}(\omega t)$ and $i_{L2}(\omega t)$ and its low frequency behavior can be seen in Figure 13. Unitary α and a pure and unitary sinusoidal current i_{L2} were considered.

The maximum current ripple in both L_1 and L_2 occurs at $\omega t = 3\pi/2$ and the peak value in L_1 is given by:

$$I_{L1pk} = I_{opk}(1+\alpha)\,. \quad (32)$$

The capacitance of the input filter capacitor is determined by the following expression:

$$C_f = \frac{\sqrt{2}I_{orms}(1+\alpha)}{2\Delta v_{Cf} f_s}\,. \quad (33)$$

This filter cutoff frequency is given according to (34). By rearranging this equation, L_f can be calculated for the desired cutoff frequency using (35).

$$\omega_f = 2\pi f_f = \frac{1}{\sqrt{L_f C_f}} \quad (34)$$

$$L_f = \frac{1}{\left(2\pi f_f\right)^2 C_f}\,. \quad (35)$$

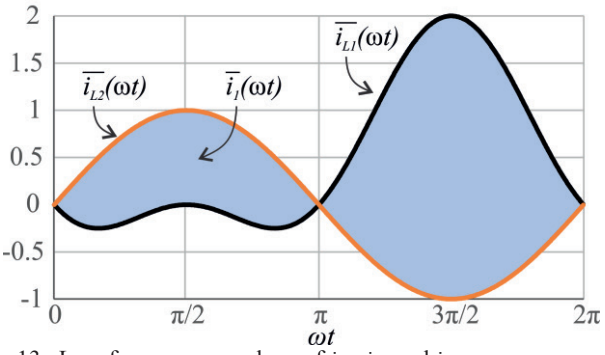


Fig. 13. Low frequency envelope of i_{L1}, i_{L2} and i_1.

IV. EXPERIMENTAL RESULTS

A 1 kW prototype was designed, built and tested in the laboratory. An RC load was used instead of the grid in order to validate the theoretical analysis. The experimental prototype specifications are shown in Table I. The parameters determined using the equations obtained in the theoretical analysis are shown in Table II. The thermal design was performed considering both power semiconductors mounted on a single heatsink. A junction temperature of 100 ºC was adopted and an ambient temperature that was considered to be 40 ºC.

The components used in the prototype construction are listed in Table III and a photograph can be seen in Figure 14. In addition to the power stage, the prototype includes a signal processing printed circuit board (PCB), used to generate the semiconductor gate signals, employing the DSP LAUNCHXL-F28069M.

The results reported below were obtained from tests performed in open loop, in order to verify the operation described herein.

The output voltage and current in the resistive load, v_o and i_{Ro} respectively, are shown in Figure 15. This figure also shows the input voltage V_1 and current i_{Lf}. The voltage THD was 3.96%, according to the power analyzer (Tektronix PA4000).

The currents on inductors L_1 and L_2 can be seen in Figure 16. As expected, these currents are envelope-shaped, similarly to that shown in Figure 13.

The voltages on the power semiconductors can be seen in Figure 17, where the peak value occurs at the negative peak of the output voltage. This time interval is shown in detail in Figure 18. It is interesting to note that there are almost no overvoltages in these waveforms, even though there is no voltage clamping circuit.

The leakage current measurement has been performed and is shown in Figure 19. The 50 mA/div scale is observed in the reading of this current because it is a low amplitude signal, whose measured RMS value is 1.4 mA.

Figure 20 presents the theoretical mapping of the main power losses in the proposed converter operating at rated power. Considering that, the expectation is for the inverter to achieve about 96.2% efficiency at rated power. However, it can be seen that 77% of the power losses are in the transistors, so using better transistors can allow higher efficiencies to be reached, similar to those achieved by well-known converters.

TABLE I
Experimental Prototype Specifications

Symbol	Description	Value
V_1	DC input voltage	400 V
V_{orms}	Load voltage (RMS)	220 V
P_o	Output power	1 kW
f_s	Switching frequency	50 kHz
f_g	Output voltage frequency	60 Hz
$\Delta i_{L1\%}$	Current ripple in L_1	50%
$\Delta i_{L2\%}$	Current ripple in L_2	50%
$\Delta v_{C1\%}$	Voltage ripple across C_1	5%
$\Delta v_{Cf\%}$	Voltage ripple across C_f	1%
f_f	Filter cutoff frequency	4.8 kHz

TABLE II
Design of Components and Stresses

Symbol	Description	Value
L_1	Inductance L_1	4.10 mH
L_2	Inductance L_2	1.59 mH
C_1	Capacitance C_1	2.31 µF
C_f	Capacitance C_f	28.57 µF
L_f	Inductance L_f	38.48 µH
I_{L1rms}	RMS current in L_1	5.53 A
I_{L2rms}	RMS current in L_2	4.60 A
I_{C1rms}	RMS current in C_1	4.58 A
I_{S1rms}	RMS current in S_1	6.46 A
I_{S2rms}	RMS current in S_2	7.16 A
I_{L1pk}	Peak current in L_1	11.43 A
I_{L2pk}	Peak current in L_2	6.43 A

TABLE III
Prototype Components

Component	Specification
Inductor L_1	Inductance: 4.13 mH Number of turns: 173 Wire: 1 x 15 AWG Core: 2 x MMTS60T7713 (Magmattec)
Inductor L_2	Inductance: 1.60 mH Number of turns: 152 Wire: 1 x 15 AWG Core: 1 x MMTS60T7713 (Magmattec)
Inductor L_f	Inductance: 39.26 µH Number of turns: 19 Wire: 1 x 15 AWG Core: 1 x MMT026T4015 (Magmattec)
Capacitor C_1	2 µF (2 x 1 µF/1.25 kV - B32656S7105K577)
Capacitor C_f	30 µF/650 V - C4AQCBW5300A3JJ
Capacitor C_o	1 µF/630 V
Switches S_1 and S_2	C2M0080170P (1700 V/40 A)
Heatsink	LAM 3 K 150 12 (Fischer Elektronik)

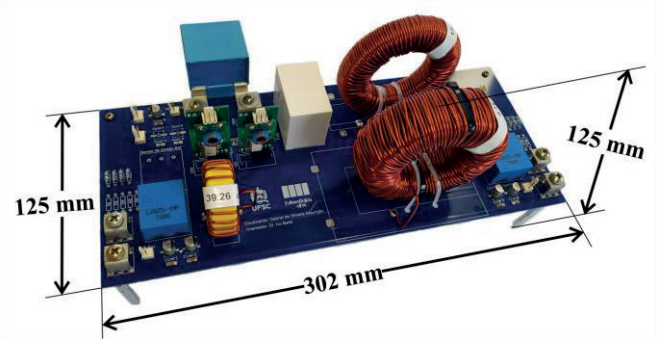


Fig. 14. Photograph of the converter prototype.

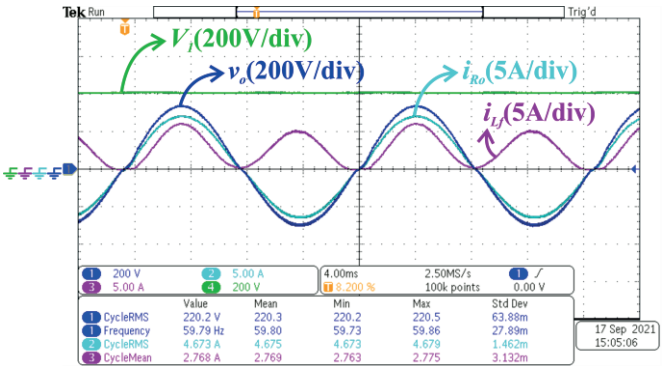


Fig. 15. Experimental input and output voltages and currents for resistive load for rated power condition and 60 Hz frequency.

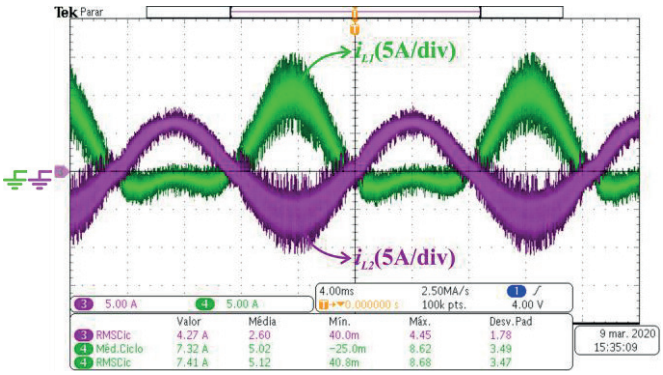


Fig. 16. Current in inductors L_1 and L_2 for rated power condition and 60 Hz frequency.

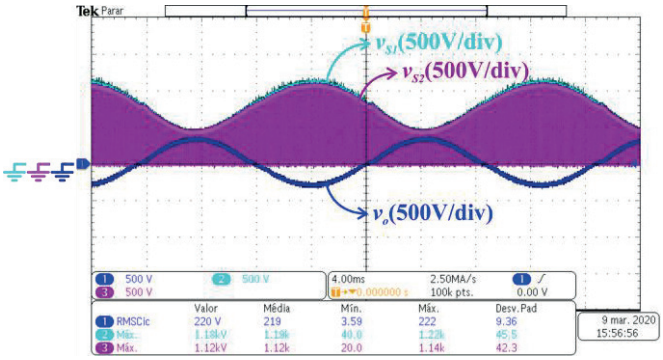


Fig. 17. Output and switch voltage for rated power condition and 60 Hz frequency.

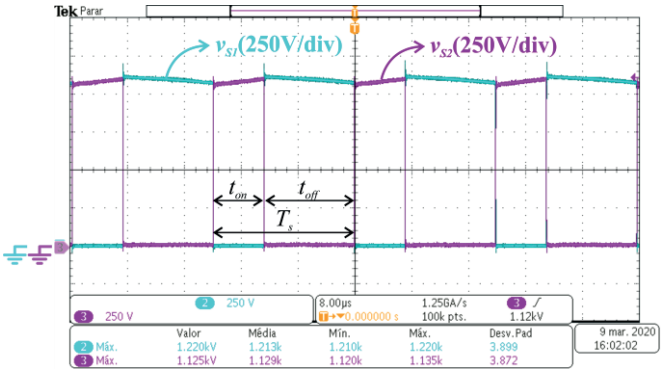


Fig. 18. Detail of the switch voltage during the output current negative peak for rated power condition and 60 Hz frequency.

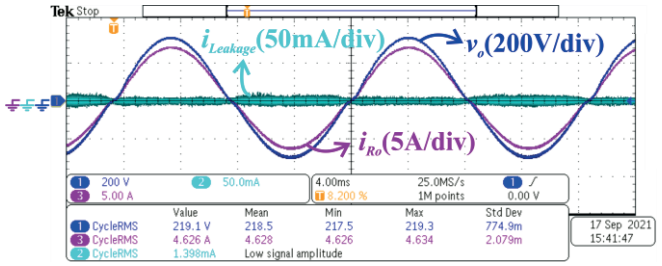


Fig. 19. Experimental output voltage, current in R_o load, and leakage current of the experimental prototype of the inverter, operating at rated power condition.

The experimental efficiency curve can be seen in Figure 21. The measurements were taken with the Tektronix PA4000 power analyzer. According to this figure, the efficiency is greater than 90% when the output power is

higher than 20% of the rated power. At over 50% of rated power the efficiency is greater than 94%, with a maximum of 95.25% in the rated power. Due to the components available, the design was not optimized to reduce losses.

After thermal stabilization of the converter at rated power, the maximum temperatures occurred in the semiconductors and inductors, especially in S_2 and L_2, which reached values of 66.3 °C and 65.5 °C, respectively.

V. COMPARISON

The summarized data gathered in Table IV allow a comparison between the proposed topology and other non-isolated inverters with common-ground in terms of the number of components, input and output voltage, maximum voltage stress on the semiconductor, output power, switching frequency and efficiency at rated power. It can be noted that, of the structures included in Table IV, this proposal contains the smallest number of components and employs the lowest number of power semiconductors. The efficiency obtained was adequate, even with the non-optimized prototype.

It should be noted, however, that considering the voltage stress in the semiconductors the value for the prototype is among the highest, which may be a limitation in terms of the choice of components.

VI. CLOSED-LOOP CONTROL

In this section, the modeling and control are presented in a summarized way. Some simulation results are shown to prove that the proposed inverter can operate connected to the grid by controlling the output current.

Figure 22 depicts the connection of the inverter to the electrical grid, with the current control stage represented as a block diagram.

The dynamic behavior of the inverter, considering the resistances in the inductors and the transistors, is described by the set of differential equations

$$L_1 \frac{di_{L1}}{dt} = -v_{C1}d + V_1(1-d) - i_{L1}(R_L + R_{DSon}) + i_{L2}R_{DSon} \quad (36)$$

$$L_2 \frac{di_{L2}}{dt} = V_1 d - v_{C1}(1-d) - v_o + i_{L1}R_{DSon} - i_{L2}(R_L + R_{DSon}) \quad (37)$$

$$C_1 \frac{dv_{C1}}{dt} = i_{L1}d + i_{L2}(1-d). \quad (38)$$

Thus, the small-signal model $\tilde{i}_{L2}(s)/\tilde{d}(s)$ is given by

$$\frac{\tilde{i}_{L2}(s)}{\tilde{d}(s)} = \frac{num_2 s^2 + num_1 s + num_0}{den_3 s^3 + den_2 s^2 + den_1 s + den_0} \quad (39)$$

where

$$num_2 = L_1 C_1 (V_1 + V_{C1}) \quad (40)$$

$$num_1 = L_1(1-D)(I_{L2} - I_{L1}) \quad (41)$$

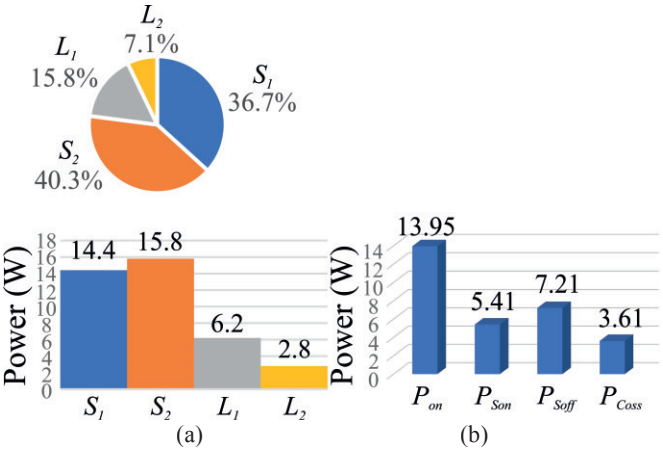


Fig. 20. Power losses distribution for the proposed topology at rated power: (a) per element and (b) detailed in the transistors.

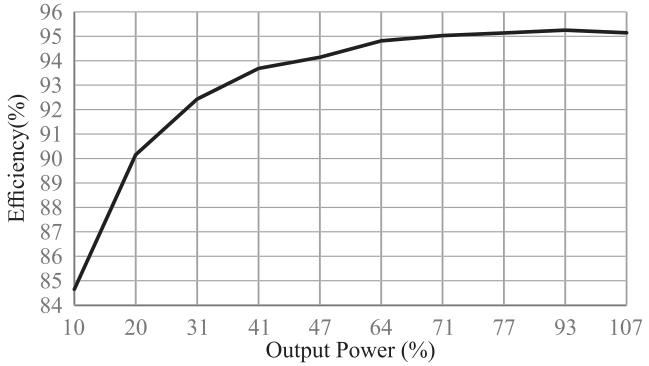


Fig. 21. Efficiency of the converter under unity power factor load.

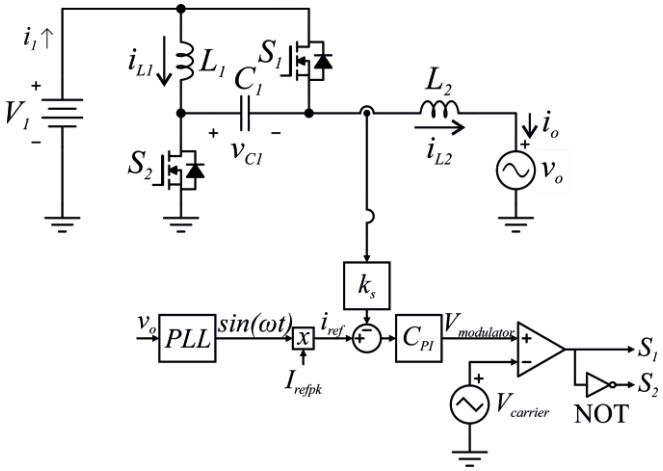


Fig. 22. Power losses distribution for the proposed topology at rated power: (a) per element and (b) detailed in the transistors.

$$num_0 = D(V_1 + V_{C1}) + R_{DSon}(I_{L2} - I_{L1}) \quad (42)$$

$$den_3 = L_1 L_2 C_1 \quad (43)$$

$$den_2 = C_1 R_{DSon}(L_1 + L_2) \quad (44)$$

$$den_1 = L_1(1-D)^2 + L_2 D^2. \quad (45)$$

TABLE IV
Comparation of Transformerless Common-Ground Inverters

Transformerless Common-Ground Topology	Number of components				Voltage			Output power	Switching frequency	Reported efficiency at rated power
	Switches	Diodes	Inductors	Capacitors	Input (V_{DC})	Output (V_{RMS})	Max. semiconductor stress			
Proposed	2	0	2	1	400	220	$2V_1+V_{opk}$	1 kW	50 kHz	95.2 %
Converter in [4]	8	1	1	2	200	240	$2V_1$	1 kW	20 kHz	96 %
Converter in [7]	5	0	2	1	≈ 100	220	$> V_{opk}$	200 W	20 kHz	92.5 %
Converter in [8]	4	1	1	2	350	230	V_1	1 kW	24.4 kHz	99.2 %
Converter in [9]	4	2	2	3	400	220	$2V_1$	500 W	24 kHz	97.4 %
Converter in [10]	5	1	2	2	340	220	$2V_1$	1 kW	100 kHz	91.6 %
Converter in [13]	5	0	1	1	400	220	V_1	500 W	20 kHz	≈ 96.5 %
Converter in [14]	5	3	2	1	92	100	-	168 W	10 kHz	≈ 87 %
Converter in [15]	4	0	3	2	60	120	≈ 300 V	250 W	50 kHz	-
Converter in [16]	3	1	4	3	38	110	1.6Vopk*	280 W	40 kHz	93 %
Three-phase converter in [22]	4	1	2	2	200	≈ 110	-	≈ 460 W per phase	9 kHz	-

* Only for V_{opk}/V_1 equal to 4.1

$$den_0 = R_{DSon} \cdot \quad (46)$$

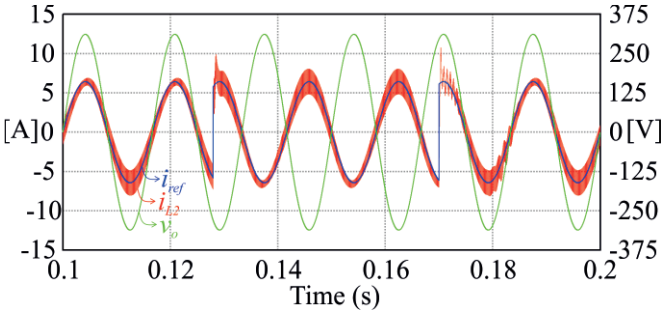


Fig. 23. Grid voltage, current reference, and i_{L2} current of the grid-connected inverter.

Substituting the parameters of the power stage given in Table III, with $R_L = R_{DSon} = 0.1\Omega$, and obtaining the variables function of the ωt angle for $\omega t = 2\pi/3$, which is the critical angle from the system stability point of view, it can be found:

$$\frac{\tilde{i}_{L2}(s)}{\tilde{d}(s)} = \frac{6.945\times10^5 s^2 - 3.555\times10^9 s + 3.0048\times10^{13}}{s^3 + 173.4 s^2 + 1.437\times10^8 s + 1.165\times10^{10}} . \quad (47)$$

A PI controller was employed, with a current sensor gain equal to 3×10^{-4} and a PWM modulator gain equal to 1. The transfer function of the controller with these parameters is given by

$$C_{PI} = \frac{13.339(s+4788)}{s} . \quad (48)$$

The simulation result of the system in Figure 22 is presented in Figure 23, which shows the grid voltage, current reference, and current in L_2. It can be observed that regardless of the phase angle ωt , the output current i_{L2} follows the reference current i_{ref} , indicating that the inverter operates with both positive and negative power flow.

VII. CONCLUSIONS

A new single-phase voltage source inverter has been proposed. The converter topology contains few components and a simple modulation strategy. Also, it eliminates the leakage current in the parasitic capacitors.

The effectiveness of the proposed converter was demonstrated. The prototype built in the laboratory and subsequently tested confirmed the operation principle and the theoretical analysis results. Although this prototype was not optimized for loss reduction, a maximum efficiency of 95.25% was obtained.

Through computer simulation, it was shown that the inverter with proper current control can interconnect a bidirectional DC voltage source with the grid, being able to operate with both positive and negative power flow.

Thus, the proposed inverter topology is suitable for the power interface between a battery bank and the grid, without the need for a high or low frequency transformer. A disadvantage, however, with respect to the conventional voltage source inverters is a higher voltage stress across the power semiconductors.

ACKNOWLEDGMENTS

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