HYBRID POWER FILTER BASED ON A SIX-SWITCH TWO-LEG INVERTER

Leonardo R. Limongi, Luiz G. B. Genú, Luís R. Silva Filho, Fabrício Bradaschia, Gustavo M. S. Azevedo
Universidade Federal de Pernambuco (UFPE), Recife, Pernambuco, Brazil
leonardo.limongi@ufpe.br, fabricio.bradaschia@ufpe.br, gustavomsa@aim.com

***Abstract* - Hybrid power filters (HPFs) are considered an attractive solution to overcome the problem of current harmonics generated by nonlinear loads. They mix low power rating active filters with passive filters, but many of these HPF topologies have a great number of passive components and/or transformers. Based on this fact, new concepts of HPFs, consisting of small rated inverters and LC filters, have been introduced with wide acceptance. The advantage comes from the fact that these HPFs are connected to the grid without any matching transformer. This paper proposes a transformerless HPF based on a new six-switch two-leg inverter with an enhanced harmonic compensation capability. Besides presenting a reduced number of switches when compared with dual topologies, the proposed solution is capable of providing good compensation even for loads with a high harmonic content. Experimental results are presented for a HPF inverter prototype in order to demonstrate the effectiveness of the proposed topology.**

***Keywords* – Active Power Filters, Diode Rectifiers, Harmonics, Hybrid Power Filters.**

I. INTRODUCTION

Nowadays, the large number of computers and other sensitive electrical loads connected to the power grid are directly affected by power quality problems [1]. One of the most important power quality issues is related to current harmonics generated by the increasing number of nonlinear loads connected to the power grid. Harmonic restriction standards, such as IEEE 519 [2], have been recommended to limit the harmonic currents injected into the grid by nonlinear loads.

Shunt passive filters, consisting of tuned LC filters and high-pass filters, have traditionally been used as a simple and low cost solution to compensate current harmonics. Nevertheless, their performance strongly depend on the grid impedance and can possibly cause the unwanted parallel resonance phenomena with the grid [3].

In the last decades, the increasing reliability of power semiconductor devices motivated the development of power electronics solutions to the problem of harmonic circulation into the grid. The shunt active power filter (APF), consisting basically of a voltage source inverter (VSI) with a large capacitor on its dc-link, is considered a well-established solution to reduce the current harmonics to the recommended standards limits. The major drawback of shunt APFs is the high power rating components required for compensating high peak harmonic currents and their associated costs [4]- [20].

An alternative, called hybrid power filter (HPF), mixes low power rating active filters with passive filters, aiming the cost reduction [21]- [24]. The converters used in HPFs require typically 5-8% of the load kVA rating, which is considerably lower than the power rating of conventional APFs, making HPF systems attractive and cost-effective. The principle of operation of these converters is based on improving the filtering characteristics of passive filters avoiding the undesirable resonances with the grid. Unfortunately, many of these HPF topologies have, as common disadvantage, a great number of passive components and/or transformers, that directly influence the weight and size of these filters [23]- [31].

On the other hand, a great effort has been made in order to decrease the number of components in HPFs. In [32], it was presented a HPF consisting of a low power rating three-phase VSI connected to the load at the point of common coupling (PCC) through a LC passive filter without any matching transformer. The LC filter absorbs some harmonic currents produced by the non-linear load, whereas the active filter improves the filtering characteristics of the LC filter.

A reduced switch version of the transformerless HPF was proposed in [33]. This was achieved eliminating one phase leg of the inverter and connecting the remaining phase to the negative pole of the dc-link. This is feasible because the capacitors of the LC filter block the dc components generated by the connection of one phase to the negative pole of the dc-link. As advantage, reduced switch topologies are more reliable and present lower cost and complexity.

Other topologies use dual converters configurations to compensate highly nonlinear loads, high values of di/dt, or to supply the load reactive power [34], [35]. In [34], a transformerless back-to-back HPF [33] is used to compensate current harmonics and reactive power. Both outputs of back-to-back converter are connected to the PCC through two sets of passive filters tuned on 7^{th} and 13^{th} harmonics. The main advantage of this topology comes from its enhanced compensation capabilities.

Aiming not only an improvement of the compensation performance but also a cost reduction, this paper presents a transformerless HPF based on a new six-switch two-leg (SSTL) inverter. The SSTL inverter is connected to the PCC through two sets of passive filters tuned on 7^{th} and 13^{th} harmonics, similar to [34]. Thus, the proposed HPF presents an enhanced harmonic compensation capability with the advantage of having a reduced number of switches (six, instead of eight). Experimental results are presented for the HPF prototype to demonstrate the effectiveness of the

Manuscript received on 20/12/2013. First revision on 20/02/2014. Accepted for publication on 18/05/2014, by recommendation of the Editor Henrique A. C. Braga.

proposed topology.

II. PROPOSED HYBRID POWER FILTER

The HPF, shown in Figure 1, is based on a new SSTL inverter, which is a two-leg version of the nine-switch inverter (Figure 2) [36]. The SSTL inverter, shown in Figure 3, can be seen as two three-phase inverter units connected in series with two passive LC filters tuned in different harmonic frequencies. The top unit, consisting of outputs *ABC*, is connected to the PCC through a LC filter tuned around the 7^{th} harmonic component and it is responsible to eliminate the harmonic pair 5^{th} and 7^{th} and also to maintain the dc-link voltage constant in a desired value. Similarly, the bottom unit, represented by the outputs *RST*, is connected to the PCC through a LC filter tuned around the 13^{th} harmonic component, being responsible for compensating the harmonic pair 11^{th} and 13^{th}. Thus, the objective of the proposed topology is to obtain a superior compensation capability when compared with conventional HPFs, without increasing the number of switches in the active filter: the SSTL inverter has the same number of switches of a conventional three-phase VSI.

Since the SSTL inverter is a non-conventional topology, the proposed HPF have two peculiarities that should be noted. Firstly, the connection of both inverter units to the PCC could naturally generate a dc current circulation in the system, through phases *ABC* and *RST*. Additionally, the direct connection of phases *C* and *T* in the PCC could cause a short-circuit in positive and negative poles of the dc-link. Fortunately, the capacitors of the passive LC filters ($C_{F_{TOP}}$ and $C_{F_{BOT}}$) block the dc current circulation and avoid the short-circuit in the dc-link. Secondly, as the output voltages of the top inverter unit should be always higher than the output voltages of the bottom inverter unit, it is necessary a minimum dc-link voltage capable of generating the sum of both output voltages. Fortunately, the series connection of the inverter with the passive filters in HPFs guarantees a much lower voltage requirement at inverter's output when compared with conventional APFs. Thus, the dc-link voltage requirement is not a issue in the proposed topology.

In this section, the SSTL inverter is analysed and a specific modulation technique is presented. Subsequently, the design guidelines for the passive LC filters is carried out.

A. Six-Switch Two-Leg Inverter Analysis

As can be seen in Figure 2, there are three possible switching states for each leg of the nine-switch inverter, i.e. always one switch is open and the other two are closed. Depending on the switching state, two different voltage levels can be imposed at each inverter output terminal. The switching states and the output voltages for inverter leg *AR* are described in Table I.

Focusing only on inverter leg *AR* and considering Table I, it is possible to find that switch S_A controls the voltage v_{Ao} as follows:

$$v_{Ao} = (2S_A - 1)\frac{v_{dc}}{2}, \tag{1}$$

where $S_A = 0$ and $S_A = 1$ represent switch open and closed, respectively.

The duty cycle D_A of switch S_A can be determined taking the average value of (1) in one switching period:

$$D_A = \frac{1}{2} + \frac{v_A^*}{v_{dc}}, \tag{2}$$

where v_A^* is the reference voltage imposed at the output terminal *A*, which is equal to $\overline{v}_{Ao}$ (average value) if the switching frequency is sufficiently high.

Similarly, observing Table I, it is possible to note that switch S_R controls the voltage v_{Ro} through the following expression

$$v_{Ro} = (1 - 2S_R)\frac{v_{dc}}{2}, \tag{3}$$

where $S_R = 0$ and $S_R = 1$ represent switch open and closed, respectively.

Taking the average value of (3) in one switching period, is possible to find the duty cycle D_R of switch S_R:

$$D_R = \frac{1}{2} - \frac{v_R^*}{v_{dc}}, \tag{4}$$

where v_R^* is the reference voltage imposed at the output terminal *R*, which is equal to $\overline{v}_{Ro}$ (average value) if the switching frequency is sufficiently high.

It can be noted that switches S_A and S_R have opposite behavior: while v_{Ao} is positive when $S_A = 1$, v_{Ro} is positive when $S_R = 0$, and vice-versa. For this reason, the duty cycle D_R presents an opposite sign when compared with D_A. Moreover, after a careful inspection in Table I, it is possible to find that $v_{Ao} \geq v_{Ro}$ for all possible switching states. Considering the average value in a switching period, it is found that $\overline{v}_{Ao} \geq \overline{v}_{Ro}$ and, consequently, the following inequality should be respected:

$$v_A^* \geq v_R^*. \tag{5}$$

Based on the inequality in (5), it is impossible for the SSTL inverter to synthesize two pure sinusoidal voltages at outputs A and R, since at some point the sinusoidal voltage v_R^* would become greater than v_A^*.

Nevertheless, this restriction can be overcome by shifting the sinusoidal waveforms in v_A^* and v_R^*, in order to guarantee that always $v_A^* \geq 0$ and $v_R^* \leq 0$. Considering $\widehat{V}_A$ and $\widehat{V}_R$ as the amplitudes of the sinusoidal waveforms in v_A^* and v_R^*, respectively, that depend on the chosen modulation index, and $\widehat{V}_A^{max}$ and $\widehat{V}_R^{max}$ as the maximum amplitudes achieved by the sinusoidal waveforms in the limit of the linear region of the modulation index, the reference voltages can be defined as

$$\begin{aligned} v_A^* &= \widehat{V}_A \cdot sin(\omega_A t) + \widehat{V}_A^{max} \\ v_R^* &= \widehat{V}_R \cdot sin(\omega_R t) - \widehat{V}_R^{max}. \end{aligned} \tag{6}$$

Therefore, with the reference voltages defined in (6), it is possible to guarantee that $v_A^* \geq 0$, $v_R^* \leq 0$ and the condition imposed by (5) is always respected. Replacing (6) in (2) and (4), yields:

$$D_A = \frac{1}{2} + \frac{\widehat{V}_A \cdot sin(\omega_A t)}{v_{dc}} + \frac{\widehat{V}_A^{max}}{v_{dc}} \tag{7}$$

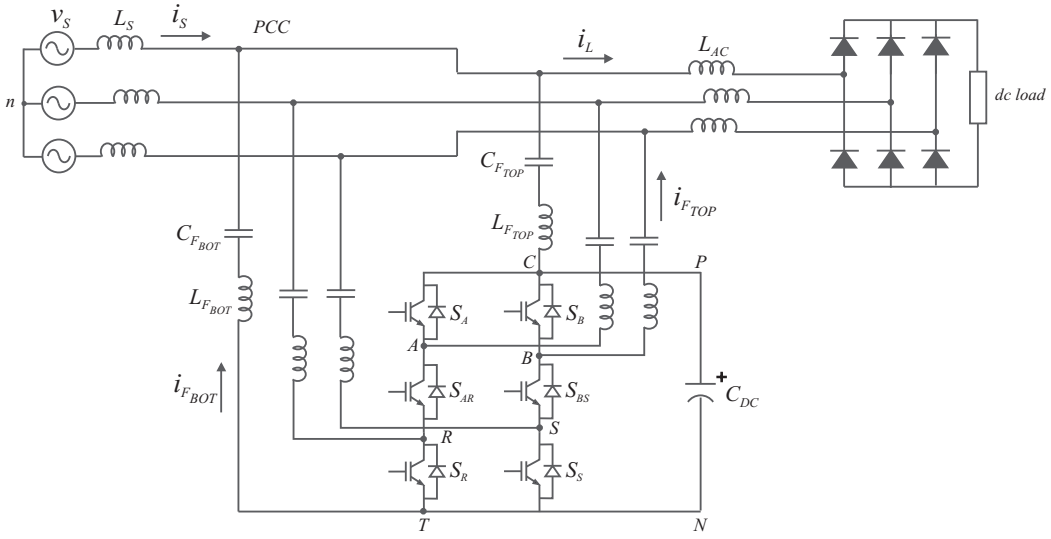


Fig. 1. Proposed transformerless HPF based on a SSTL inverter.

$$D_R = \frac{1}{2} - \frac{\widehat{V}_R \cdot sin(\omega_R t)}{v_{dc}} + \frac{\widehat{V}_R^{max}}{v_{dc}}. \tag{8}$$

Taking into account that $0 \leq \{D_A, D_R\} \leq 1$, it is possible to find that

$$\widehat{V}_A^{max} = \widehat{V}_R^{max} = \frac{v_{dc}}{4}. \tag{9}$$

Replacing (9) in (7) and (8), yields

$$\begin{aligned} D_A &= \tfrac{3}{4} + \tfrac{\widehat{V}_A \cdot sin(\omega_A t)}{v_{dc}} \\ D_R &= \tfrac{3}{4} - \tfrac{\widehat{V}_R \cdot sin(\omega_R t)}{v_{dc}}. \end{aligned} \tag{10}$$

The duty cycles D_A and D_R in (10) synthesize the average output voltages $\overline{v}_{Ao}$ and $\overline{v}_{Ro}$, respectively. Also, observing the SSTL inverter topology, shown in Figure 3, it can be seen that $\overline{v}_{Ao} = v_{AC}^* + v_{dc}/2$ and $\overline{v}_{Ro} = v_{RT}^* - v_{dc}/2$. Therefore, the dc components in $\overline{v}_{Ao}$ and $\overline{v}_{Ro}$ are synthesized by the dc components in (10) and the reference line voltages v_{AC}^* and v_{RT}^* are synthesized by the sinusoidal components in (10). Thus, renaming the sinusoidal components in (10) as v_{AC}^* and v_{RT}^*, yields

$$\begin{aligned} D_A &= \tfrac{3}{4} + \tfrac{v_{AC}^*}{v_{dc}} \\ D_R &= \tfrac{3}{4} - \tfrac{v_{RT}^*}{v_{dc}}. \end{aligned} \tag{11}$$

Based on (11), valid for one leg of the SSTL inverter (Figure 3), it is possible to derive the duty cycle expressions for both legs of the SSTL inverter:

$$\begin{aligned} D_A &= \tfrac{3}{4} + \tfrac{v_{AC}^*}{v_{dc}}, \quad D_B = \tfrac{3}{4} + \tfrac{v_{BC}^*}{v_{dc}} \\ D_R &= \tfrac{3}{4} - \tfrac{v_{RT}^*}{v_{dc}}, \quad D_S = \tfrac{3}{4} - \tfrac{v_{ST}^*}{v_{dc}} \end{aligned} \tag{12}$$

It is important to mention that (12) presents only the duty cycles of the top and bottom switches of the SSTL inverter. Based on Table I, the states of the intermediate switches are defined as the *exclusive or* of the top and bottom switches states, i. e. $S_{AR} = XOR(S_A, S_R)$ and $S_{BS} = XOR(S_B, S_S)$.

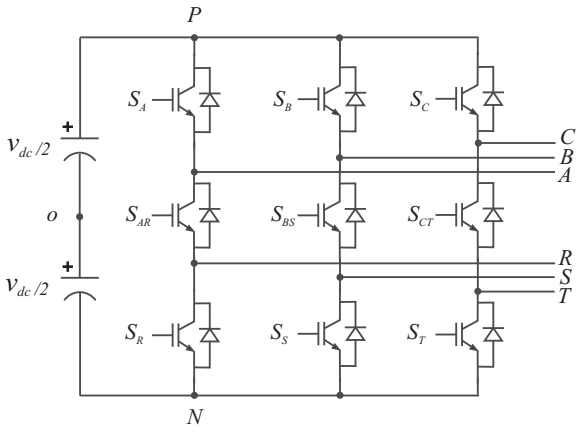


Fig. 2. Nine-switch inverter.

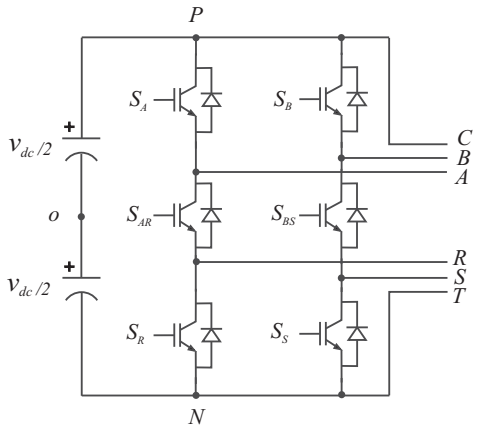


Fig. 3. SSTL inverter.

TABLE I
Switching states and output voltages for leg *AR*

Switching State	S_A	S_{AR}	S_R	v_{Ao}	v_{Ro}
1	On	On	Off	$+v_{dc}/2$	$+v_{dc}/2$
2	On	Off	On	$+v_{dc}/2$	$-v_{dc}/2$
3	Off	On	On	$-v_{dc}/2$	$-v_{dc}/2$

B. Passive Filters Design and Analysis

The design characteristics of the passive LC filters, i.e. the resonant frequency and quality factor, have an important influence on the compensation performance of the HPF. Usually, the filter inductance and capacitance are defined based on three guidelines:

1. The resonant frequencies, $\omega_{F_{TOP}} = 1/\sqrt{L_{F_{TOP}}C_{F_{TOP}}}$ and $\omega_{F_{BOT}} = 1/\sqrt{L_{F_{BOT}}C_{F_{BOT}}}$, have to be chosen around to the frequencies of main harmonic components to be compensated. Thus, the passive filters alone are able to partially absorb the desired harmonic components;
2. In order to guarantee low impedance values for the harmonic components in the vicinity of the resonant frequencies, the filters quality factors, $Q_{F_{TOP}} = (1/R_{F_{TOP}})(\sqrt{L_{F_{TOP}}/C_{F_{TOP}}})$ and $Q_{F_{BOT}} = (1/R_{F_{BOT}})(\sqrt{L_{F_{BOT}}/C_{F_{BOT}}})$, have to be minimized. Since the values of $R_{F_{TOP}}$ and $R_{F_{BOT}}$ should be low to reduce the losses in the HPF, the aim is to minimize the relations $L_{F_{TOP}}/C_{F_{TOP}}$ and $L_{F_{BOT}}/C_{F_{BOT}}$;
3. The rated voltage of each passive filter capacitor should be higher than a specific value that depends on the dc-link and grid voltages. This subject is further analyzed in this section;
4. The capacitances, $C_{F_{TOP}}$ and $C_{F_{BOT}}$, have to be chosen to guarantee a specific amount of reactive power generated by the passive filters at the fundamental frequency. This subject is further analyzed in this section.

The above guidelines can be used to design any HPF system. In order to explain the third and fourth guidelines, the interaction between the two passive LC filters should be analyzed both in dc and fundamental frequency, as can be seen in the equivalent circuits in Figure 4.

The dc equivalent circuit of the HPF is shown in Figure 4(a). Analyzing this equivalent circuit, it is possible to determine the dc voltage components of the passive filter capacitors. Since the grid does not present any dc voltage component, it appears as short-circuits in the equivalent model. Moreover, the passive filter inductors, $L_{F_{TOP}}$ and $L_{F_{BOT}}$, can be disregarded in a steady-state analysis. Based on the dc components in (11), the SSTL inverter can be represented as four dc voltages sources as shown in Figure 4(a). A careful analysis in the equivalent circuit results in the follow expressions:

$$\begin{aligned} v_{F_R} - v_{F_A} &= \tfrac{v_{dc}}{2} \\ v_{F_S} - v_{F_B} &= \tfrac{v_{dc}}{2}. \\ v_{F_T} - v_{F_C} &= v_{dc} \end{aligned} \tag{13}$$

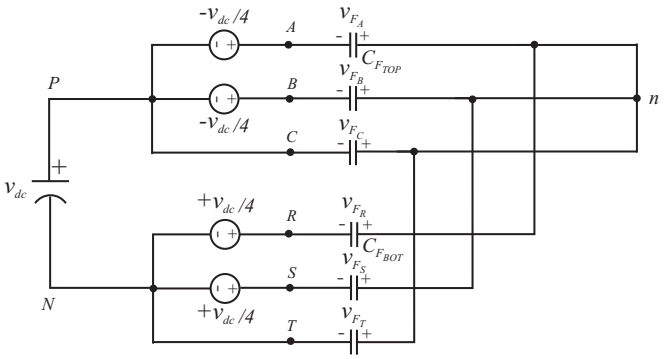
Since the capacitors of each phase pair *AR*, *BS* and *CT* are in series, it can be assumed that their voltages are related as follows:

$$\begin{aligned} v_{F_A} &= -\frac{C_{F_{BOT}}}{C_{F_{TOP}}} v_{F_R} \\ v_{F_B} &= -\frac{C_{F_{BOT}}}{C_{F_{TOP}}} v_{F_S} \\ v_{F_C} &= -\frac{C_{F_{BOT}}}{C_{F_{TOP}}} v_{F_T} \end{aligned} \tag{14}$$

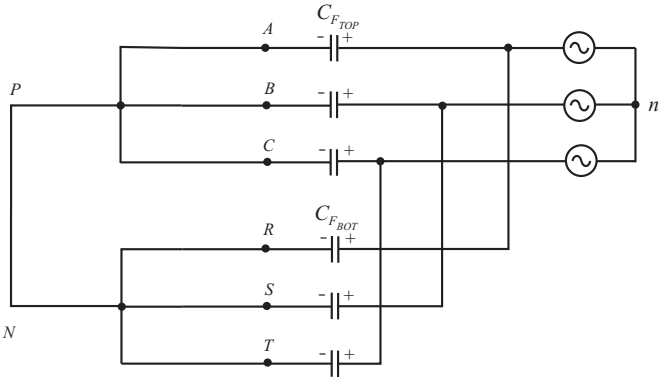
Combining (13) and (14), the following relations can be found:

$$\begin{aligned} v_{F_A} &= -\left(\frac{C_{F_{BOT}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)\frac{v_{dc}}{2}, \quad v_{F_R} = \left(\frac{C_{F_{TOP}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)\frac{v_{dc}}{2}, \\ v_{F_B} &= -\left(\frac{C_{F_{BOT}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)\frac{v_{dc}}{2}, \quad v_{F_S} = \left(\frac{C_{F_{TOP}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)\frac{v_{dc}}{2}, \\ v_{F_C} &= -\left(\frac{C_{F_{BOT}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)v_{dc}, \quad v_{F_T} = \left(\frac{C_{F_{TOP}}}{C_{F_{TOP}}+C_{F_{BOT}}}\right)v_{dc}. \end{aligned} \tag{15}$$

It should be noted that the relations in (15) define only the dc voltage component present in the capacitors of the passive filters. There is also a fundamental frequency voltage component that should be analyzed. The fundamental frequency equivalent circuit of the HPF is shown in Figure 4(b). Since the SSTL inverter only compensates harmonic components, i.e. does not generate fundamental frequency voltages, it can be represented as a short-circuit as well as the dc-link. Moreover, in the fundamental frequency, the inductor impedance is negligible when compared to the capacitor impedance and could be disregarded. Therefore, the grid phase voltages are applied directly in the capacitors of



(a) Equivalent dc circuit.



(b) Equivalent circuit for the fundamental frequency.

Fig. 4. Equivalent circuits of the proposed HPF.

the passive filters. In short, the rated voltage of each filter capacitor in the proposed HPF should be higher than the grid phase voltage plus the dc voltage component defined in (15).

Additionally, in Figure 4(b), it is possible to see that the capacitors $C_{F_{TOP}}$ are in parallel with the capacitors $C_{F_{BOT}}$. Thus, the proposed HPF can supply a fixed reactive power equal to:

$$Q_F \approx 3\omega_1(C_{F_{TOP}} + C_{F_{BOT}})V_{PCC}^2, \tag{16}$$

where ω_1 is the fundamental frequency and V_{PCC} is the rms value of the grid phase voltages at the PCC. The capacitors rated voltage constrain and the reactive power defined in (16) are the fourth and the fifth guidelines to be followed when designing the proposed HPF.

III. DESCRIPTION OF OVERALL CONTROL SYSTEM

The overall control block diagram of the proposed HPF is shown in Figure 5. It is possible to define three main subsystems: the top inverter unit control, the bottom inverter unit control and the shared control block, that is connected to both top and bottom inverter unit controls. Each unit control contains feedback and feedforward loops based on the control system proposed in [32].

A. Top Inverter Unit Control

As can be seen in Figure 1, the top inverter unit is connected to the grid through a LC filter tuned on the vicinity of the 7^{th} harmonic. The control system senses the grid and load currents to perform the feedback and feedforward controls, respectively. The top inverter unit is also responsible to regulate the dc-link voltage using a feedback voltage controller, although the bottom unit could be used for the same purpose.

The feedback control of top inverter unit is shown in Figure 5. The first step is to isolate the harmonic components from the fundamental component of the grid currents. This is achieved through a $d_1 - q_1$ transformation, synchronized with the PCC voltage vector, and a first order high-pass filter with a cutoff frequency of 16Hz (both located in the shared control block). Then, the $d_1 - q_1$ inverse transformation (located in the top inverter unit control) produces the harmonic currents in *abc* referential frame, which is amplified by the gain k_{top}, as follow:

$$v^*_{ABC_{fb}} = k_{top} \cdot i_{S_{ABC_h}} \tag{17}$$

These signals are added to the voltage references produced by the feedforward control, resulting in the voltage references v^*_A, v^*_B, v^*_C for the top inverter unit.

The top inverter unit is also responsible to maintain the dc-link at a desired value. A proportional plus integral (PI) controller is used and its output is added to the signal $\widetilde{i}_{q1}$ in the feedback loop.

The feedforward control is used to compensate only the 5^{th} harmonic component in the top inverter unit. The purpose is to make the LC filter, naturally tuned on the 7^{th} harmonic, absorb all amount of the 5^{th} harmonic. The 5^{th} harmonic component of the load current is seen as a dc component in a reference frame synchronized in a frequency five times the grid frequency. This is performed using a $d_5 - q_5$ transformation and a first-order low-pass filter with cutoff frequency of 16Hz. The feedforward voltage reference is given by [32]

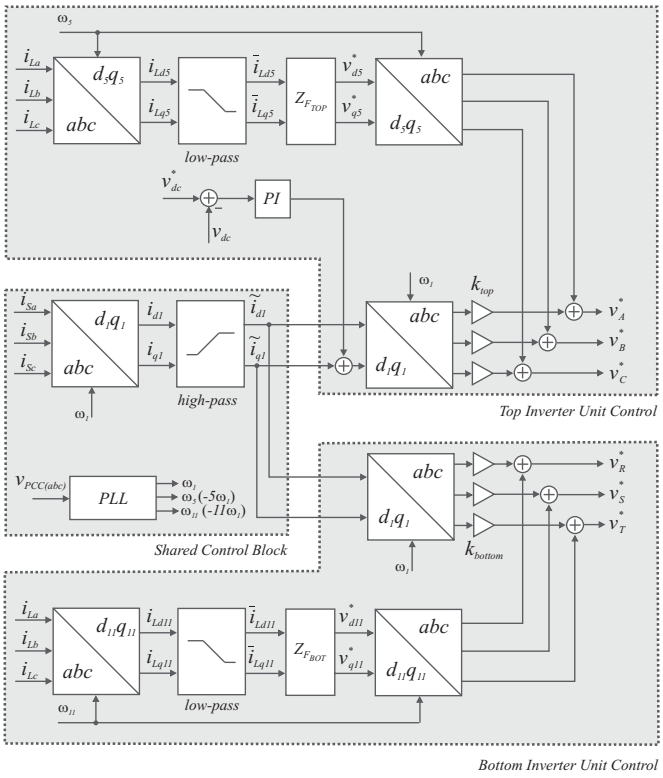


Fig. 5. Control block diagram of the proposed HPF.

$$v^*_{dq_5} = Z_{F_{TOP}} \cdot \bar{i}_{L_{dq_5}}, \tag{18}$$

where

$$Z_{F_{TOP}} = R_{F_{TOP}} + j(\omega_5 L_{F_{TOP}} - \tfrac{1}{\omega_5 C_{F_{TOP}}}). \tag{19}$$

Therefore, the inverse transformation produces the feedforward voltage references in *abc* referential frame, that are added to the feedback references.

The equivalent single-phase circuit of the proposed system for the SSTL top unit is given in Figure 6(a) [32]. The top unit inverter is represented by a voltage source v_{TOP}, the load is modeled as a current source I_L and $Z_{F_{TOP}}$ is the LC filter impedance of the top unit. The SSTL top unit inverter helps the passive filter to absorb all amount of 5^{th} and 7^{th} harmonics of the load current I_L. For better understanding, the equivalent circuit considering only the harmonics of interest is shown in Figure 6(b), where the k_{top} virtual resistance represents the ability of the SSTL top unit to block the harmonic components injected in the grid. In this scenario, the harmonic current in the grid is given as follows:

$$I_{Sh} = \frac{Z_{F_{TOP}}}{k_{top} + sL_S + Z_{F_{TOP}}} I_{Lh}, \tag{20}$$

where I_{Lh} is the load current considering only the 5^{th} and 7^{th} harmonics. If $k_{top} \gg |Z_{F_{TOP}}|$, the harmonic currents injected by the load are absorbed entirely by the LC filter. Moreover, if the value of k_{top} is considerably high, the risk of resonance with the grid is avoided [32].

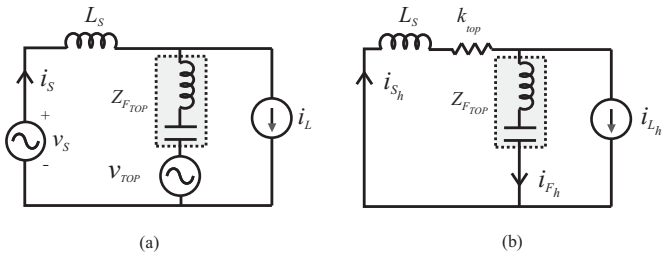


Fig. 6. Equivalent system model: (a) single-phase equivalent circuit and (b) equivalent circuit only for harmonic components.

B. Bottom Inverter Unit Control

The bottom inverter unit is connected to the PCC through a LC filter tuned on the vicinity of the 13^{th} harmonic, as shown in Figure 1. The control system uses also the grid and load currents to perform feedback and feedforward controls, respectively.

A similar procedure is performed for the feedback control of the bottom inverter unit as shown in Figure 5. However, there is no dc-link control and the k_{bottom} gain can be chosen different from k_{top}, resulting in the following voltage references:

$$v^*_{RST_{fb}} = k_{bottom} \cdot i_{S_{ABC_h}} \tag{21}$$

The feedforward control is used to compensate the 11^{th} harmonic component in the bottom inverter unit. Then, the dq transformations are performed using $\omega_{11} = -11\omega_1$ and the feedforward voltage reference and the impedance for the 11^{th} harmonic are defined as:

$$v^*_{dq_11} = Z_{F_{BOT}} \cdot \bar{i}_{L_{dq_11}} \tag{22}$$

$$Z_{F_{BOT}} = R_{F_{BOT}} + j(\omega_{11} L_{F_{BOT}} - \frac{1}{\omega_{11} C_{F_{BOT}}}) \tag{23}$$

The same system model analysis performed for the top unit stands for the bottom inverter unit if the superposition theorem is used. Therefore, If $k_{bottom} \gg |Z_{F_{BOT}}|$, the 11^{th} and 13^{th} harmonic currents injected by the load are going to sink into LC filter connected to the bottom unit. On the same way, if the value of k_{bottom} is considerably high the risk of resonance between the grid and this LC filter is avoided [32].

IV. EXPERIMENTAL RESULTS

The block diagram of the proposed SSTL HPF prototype is shown in Figure 7. The quantities measured from the system are: the grid currents $i_{S_{ABC}}$, the load currents $i_{L_{ABC}}$, the PCC voltages $v_{PCC_{ABC}}$ and the dc-link voltage v_{dc}. The system and control parameters are given in Tables II and III, respectively.

The hardware platform used to control the SSTL inverter is a dSPACE development modular system based on a DS1005 processor board and several boards for each special hardware task, i.e. DS5101 board for PWM generation, DS2004 board for A/D conversion, DS4002 board for Digital I/O. All boards are hosted in a dSpace PX10 expansion box that uses the DS817 board for bidirectional communication with a PC through optical fibers.

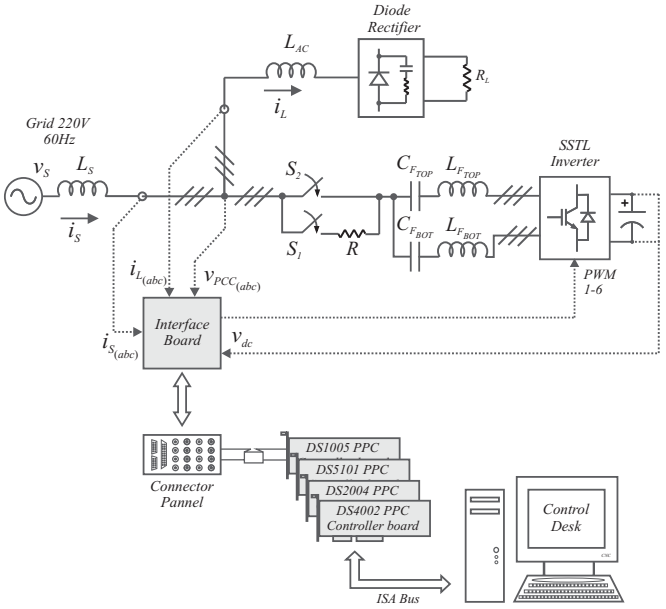


Fig. 7. Experimental setup of proposed transformerless HPF.

TABLE II
Experimental Setup Parameters

Parameter	Symbol	Value
Grid voltage amplitude (line-to-line)	V_S	$220V$
Grid frequency	f_S	$60Hz$
Switching and sampling frequency	$f_{sw}, f_{samp.}$	$20kHz$
Dc-link voltage reference	v_{dc}	$120V$
Dc-link capacitor of the SSTL inverter	C_{dc}	$4700\mu F$
Top filter capacitor (7^{th} harmonic)	$C_{F_{TOP}}$	$30.7\mu F$
Top filter inductor (7^{th} harmonic)	$L_{F_{TOP}}$	$5mH$
Bottom filter capacitor (13^{th} harmonic)	$C_{F_{BOT}}$	$61.2\mu F$
Bottom filter inductor (13^{th} harmonic)	$L_{F_{BOT}}$	$0.8mH$
Top and bottom filters reactive power	Q_F	$1.7kvar$
Nonlinear load input inductor	L_{AC}	$2.5mH$
Nonlinear load dc-link resistor	R_{load}	33Ω
Nonlinear load power	P_{load}	$2.5kW$

TABLE III
Control Parameters

Parameter	Symbol	Value
Feedback loop gain for top unit	k_{top}	11
Feedback loop gain for bottom unit	k_{bot}	28
Proportional gain for dc link control	k_p	1
Integral gain for dc link control	k_i	5

Due to the nature of the system, some attention should be given during the prototype startup and its insertion in the grid. This insertion operation is performed by switches S_1 and S_2, as shown in Figure 7. When switch S_1 is closed, both sets of LC filters are charged by the grid through a resistor R. After the transient, switch S_2 is closed. During the insertion procedure, all top and middle switches (S_A, S_B, S_{AR} and S_{BS}) of the SSTL inverter must be in *on* state; and all bottom switches (S_R, S_S) must be in *off* state. This is mandatory in order to avoid a premature charging of the dc-link capacitor.

The experimental results of the proposed HPF based on the SSTL inverter are shown in Figures 8-14. The results have been obtained through a oscilloscope and a power analyzer to identify the harmonic content in the system. All oscilloscope figures present waveforms for phase *a* in the following order:

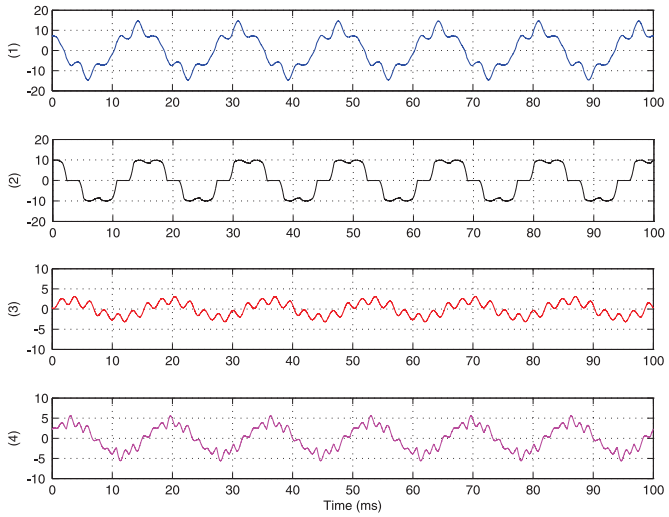


Fig. 8. Steady-state operation with top and bottom units off: (1) grid current [A]; (2) load current [A]; (3) top unit filter current [A]; (4) bottom unit filter current [A].

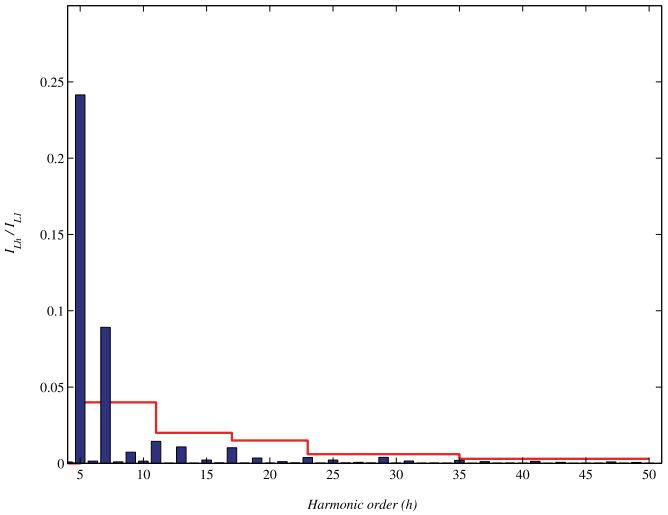


Fig. 9. Harmonic spectrum of the load current, including the harmonic component limits defined by IEEE 519-1992 [2].

grid current i_S, load current i_L, top unit filter current $i_{F_{TOP}}$ and bottom unit filter current $i_{F_{BOT}}$. In order to notice each inverter unit harmonic compensation capability, the steady-state performance is presented in four different scenarios: only with the passive filters; passive filters working with the top inverter unit on; passive filters working with the bottom inverter unit on; and passive filters and both inverter units working together. The performance of both sets of passive filters, tuned in the 7^{th} and 13^{th} harmonic frequencies, is shown in Figure 8. The total harmonic distortion (THD) of the load current is about 24%. It is possible to see, in Figure 9, the individual contribution of each harmonic component up to the 50^{th} harmonic, including the harmonic component limits defined by IEEE 519-1992 [2]. As expected, the harmonic compensation performance only considering the passive filters is not sufficient. The operation of the SSTL top inverter unit with both passive filters is shown in Figure 10. The THD for phase *a* has been reduced from 24.8% to 10%. The 5^{th} and 7^{th} harmonic components have been reduced from 22.5% to 5.6% and from 7.9% to 4.5%, respectively. Similarly, it is possible to see, the operation of the SSTL bottom inverter unit in Figure 11. The 11^{th} and 13^{th} harmonic components are reduced to 0.1% and 0.8%, respectively.

Finally, the performance of both inverter units is presented in Figure 12. The THD of grid currents is about 4% and all harmonic components have been reduced below the limits defined by IEEE 519-1992 [2], as can be seen in Figure 13. Finally, the transient performance of HPF based on the SSTL inverter with both inverters units on is shown in Figure 14 for a load step change from zero to 100%. It is possible to see a stable transient operation, reaching the steady-state after seven fundamental cycles.

V. CONCLUSIONS

This paper has proposed a transformerless hybrid power filter topology based on a new six-switch two-leg inverter. The proposed inverter, divided in two units, is connected in

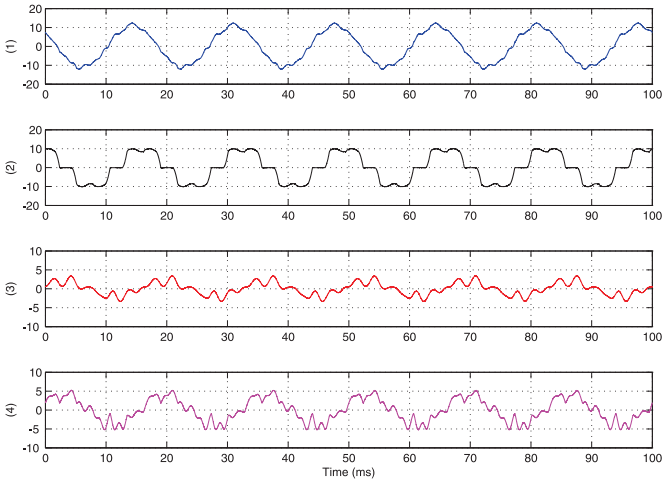


Fig. 10. Steady-state operation only with the top inverter unit on: (1) grid current [A]; (2) load current [A]; (3) top unit filter current [A]; (4) bottom unit filter current [A].

series with two passive LC filters tuned in different harmonic frequencies of interest, aiming an improvement in the harmonic compensation performance with a reduced number of switches when compared with other dual topologies. A complete analysis of both inverter and passive filters, including the guidelines necessary to design the hybrid power filter has been presented. The control algorithm of the proposed system improves the performance of both passive filters through feedback and feedforward compensations and also controls the dc-link voltage. Experimental tests were carried out, including the individual response of each inverter unit and the overall response of the proposed system, proving its feasibility.

ACKNOWLEDGEMENT

This work was supported by the *Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (CAPES)* and by the *Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq)*, Brazil.

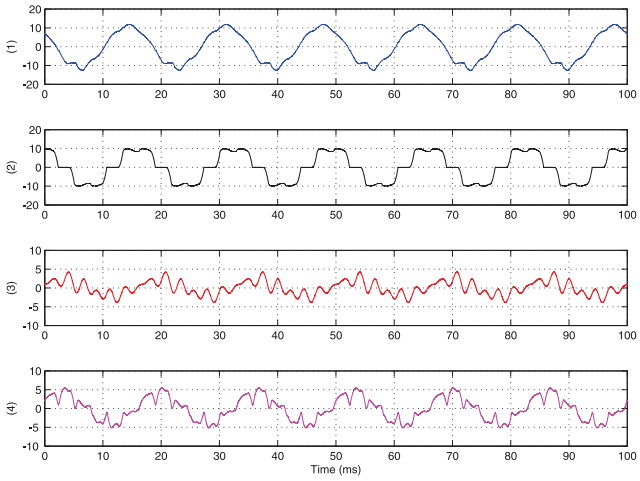


Fig. 11. Steady-state operation only with the bottom unit on: (1) grid current [A]; (2) load current [A]; (3) top unit filter current [A]; (4) bottom unit filter current [A].

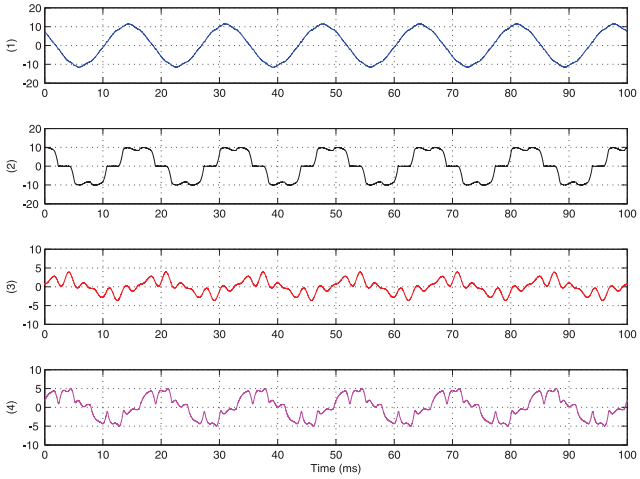


Fig. 12. Steady-state operation with both top and bottom units on: (1) grid current [A]; (2) load current [A]; (3) top unit filter current [A]; (4) bottom unit filter current [A].

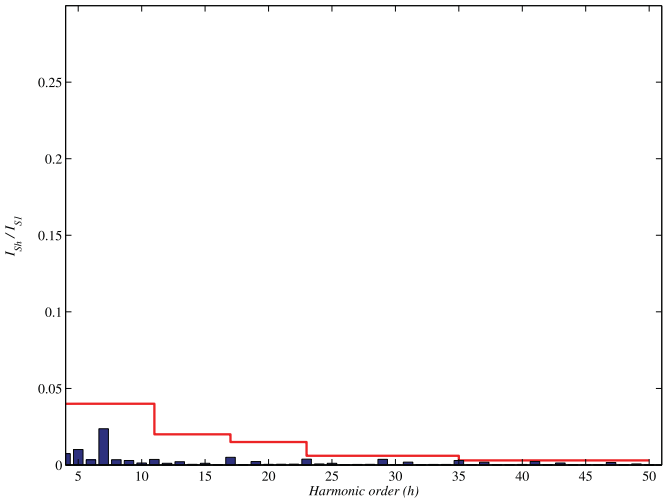


Fig. 13. Harmonic spectrum of the grid current with both top and bottom units on, including the harmonic component limits defined by IEEE 519-1992 [2].

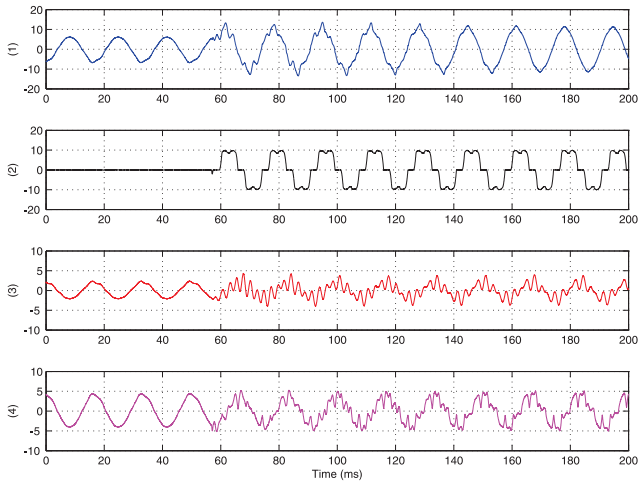


Fig. 14. Load transient response with both top and bottom units on: (1) grid current [A]; (2) load current [A]; (3) top unit filter current [A]; (4) bottom unit filter current [A].

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BIOGRAPHIES

Leonardo R. Limongi was born in Recife, Brazil, in 1978. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 2004 and 2006, respectively. He received the Ph.D degree from Politecnico di Torino, Torino, Italy, in 2009. Since 2010, he is working as a professor in the

Department of Electrical Engineering at the Federal University of Pernambuco. His research interests are renewable energy systems and power quality.

Luiz G. B. Genú was born in Pesqueira, Brazil, in 1988. He received the B.Sc. degree in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 2012, where he is currently working toward the M.Sc. degree. His research interests are power quality and power electronics.

Luís R. Silva Filho was born in Tatuí, Brazil, in 1981. He received the B.Sc. degree in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 2012, where he is currently working toward the M.Sc. degree. His research interests are power quality and power electronics.

Fabrício Bradaschia was born in São Paulo, Brazil, in 1983. He received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 2006, 2008 and 2012, respectively. He worked as a visiting scholar at the University of Alcalá, Madrid, Spain, from 2008 to 2009. Since 2013, he is working as an associate professor in the Department of Electrical Engineering at the Federal University of Pernambuco. His research interests are renewable energy systems and power quality.

Gustavo M. S. Azevedo was born in Belo Jardim, Brazil, in 1981. He received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from the Federal University of Pernambuco, Recife, Brazil, in 2005, 2007 and 2011, respectively. He worked as a visiting scholar at the Polytechnical University of Catalunya, Barcelona, Spain, from 2008 to 2009. Since 2014, he is working as an associate professor in the Department of Electrical Engineering at the Federal University of Pernambuco. His research interests are renewable energy systems and microgrids.