DIMMABLE SINGLE-STAGE SEPIC-BUCK CONVERTER FOR LED LIGHTING WITH REDUCED STORAGE CAPACITOR

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***Abstract* – This paper presents an analysis and design of an LED driver aiming to eliminate or substitute the electrolytic capacitors. Considering the low lifetime of electrolytic capacitors compared to LEDs, this topology aims for reducing the storage capacitance and replaces it by a longer lifetime capacitor, increasing the overall system life span. This reduction is based on designing of the control dynamic with a compromise between the input current distortion and the output current ripple. The power factor correction stage is based on a Single Ended Primary Inductance Converter operating under discontinuous conduction mode because of its low input current distortion characteristic making it possible to eliminate the electromagnetic interference filter. The power control stage is performed by a Buck converter using its output current source behavior, suitable for LED application. A 106 W LED driver prototype is implemented resulting in 27.1% total harmonic distortion, 50% current ripple on the LED and an efficiency of 92.18%. Furthermore an effective simple dimming strategy is proposed and implemented by an LED parallel active switch.**

***Keywords* – Electrolytic Capacitor Substitution, Integrated Converter, LED Driver, SEPIC.**

I. INTRODUCTION

A considerable amount of electrical energy generated all over the world is converted in artificial lighting [1], [2]. The efficient utilization of this energy contextualizes the high-frequency electronic ballasts application for lighting. Furthermore, due to the features of the LED in terms of color rendering index, color temperature, size, robustness, reliability, luminous efficacy and lifetime, these devices have been used increasingly in general lighting [2]-[8].

However, traditional LED drivers use electrolytic capacitors which limit the overall system lifetime [3]-[8]. Electrolytic capacitors present a useful life between 1-18 kilohours in general [9], [10]. Meanwhile the LED reaches 80 kilohours under typical operating conditions [4]. Therefore the topology proposed in this paper aims for reducing the storage capacitance, replacing this component by a film capacitor, increasing the overall system lifetime. The reached capacitance value is smaller than any other high-frequency DC-DC converter topology found in the literature for the considered output power [5]-[8].

According to the IEC 61000-3-2 Standard, lighting systems require an adequate limit of input current harmonic content for power above 25 W [11]. High-frequency DC-DC converters have been proposed as an efficient method to perform the PFC for LED drivers [4]-[8], [12]-[14].

A simplified scheme for a typical LED driver using high-frequency switched converters is presented in Figure 1. Considering an alternating current (AC) line, the first stage is the EMI filter followed by a rectifier bridge, a PFC stage and a PC stage connected to the load, providing a LED constant current.

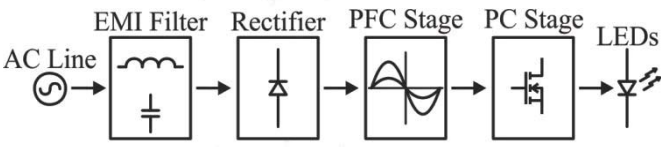

Fig. 1. Typical LED driver system stages.

The integration of both PFC and PC stages is a method to reduce the number of active switches and to simplify the command circuitry and consequently, to reduce the cost of the lighting system [15]. Thus, an integrated converter (IC) composed of PFC and PC stages is proposed in this paper, considering an integration and design methodology which allows for using a reduced storage capacitance value not previously found on literature for the considered design parameters.

This paper is organized in six sections. In Section II the IC is presented with its operational stages and waveforms. The main design equations for the topology are presented in Section III. The implemented prototype is presented in Section IV. The experimental results are shown in Section V where they are analyzed and discussed. Section VI summarizes the conclusions.

II. INTEGRATED CONVERTER ANALYSIS

Among the well-known classical DC-DC converters used as PFC, the SEPIC has attractive characteristics. It presents a step-up or step-down voltage ratio, high power factor (PF), possibility of galvanic insulation, a single switch, which shares the input and output reference, and it also might operate performing an EMI input filter. This converter also has a voltage source characteristic, which can fit the input of PC stage. The SEPIC operating under DCM as PFC allows

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for a simplified control circuitry [16], [17]. Meanwhile, to provide a 50.8 V_{DC} level to the output, from a 220 V_{AC} input source, the maximum duty cycle (D) of the SEPIC is 14.2%. Comparing to an integrated topology, this duty cycle generates higher currents in the switches. It also requires an eight times bigger bus capacitance. Thus another converter is suitable to provide an adequate power to the load, behaving as PC stage.

An option is to use a Buck converter operating in Continuous Conduction Mode (CCM) behaving as an output continuous current source, which is very convenient to feed the LED. This operation mode allows applying a reduced output capacitance (C_o) to the converter which is substantial to PWM shunt dimming strategy [18]. The Buck topology has some attractive features as low number of components and step-down voltage ratio.

The integration technique requires both converters to be operated at the same switching frequency (f_s) and duty cycle [19]. The schematic of each converter is shown in Figure 2.

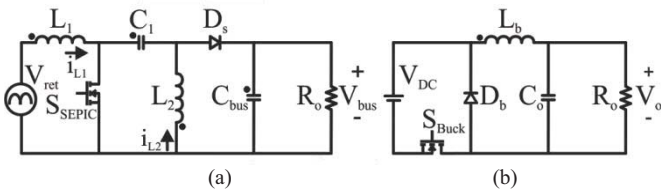

Fig. 2. Simplified schematic of SEPIC (a) and Buck (b).

Connecting the output of SEPIC to Buck converter input, a common node between the source of both switches S_{Buck} and S_{SEPIC} is identified, characterizing the T-type connection [19]. The combined circuitry is shown in Figure 3.

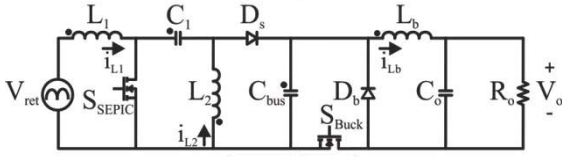

Fig. 3. Connection of both converters characterizing the T-type connection.

Using the auxiliary diodes D_1 and D_2, both switches S_{SEPIC} and S_{Buck} are replaced by only one switch S which is shared by both stages. This connection produces an intrinsic switch over current. The LED simplified model is also added, replacing the resistance R_o at the output, resulting in the integrated topology shown in Figure 4.

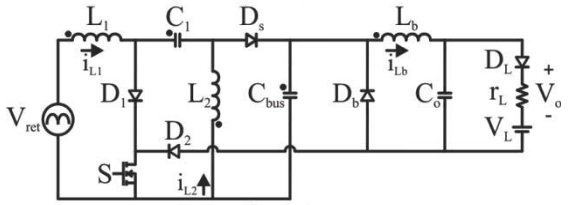

Fig. 4. Simplified schematic of the IC.

The equivalent schematic circuitry considering each IC operation stage is shown in Figure 5. This analysis considers the capacitor C_1 as a voltage source with the same instantaneous value as the input voltage during a switching period (T_s). Moreover the semiconductors are considered ideal. Figure 6 presents the element voltage and current waveforms of interest according to each operational stage.

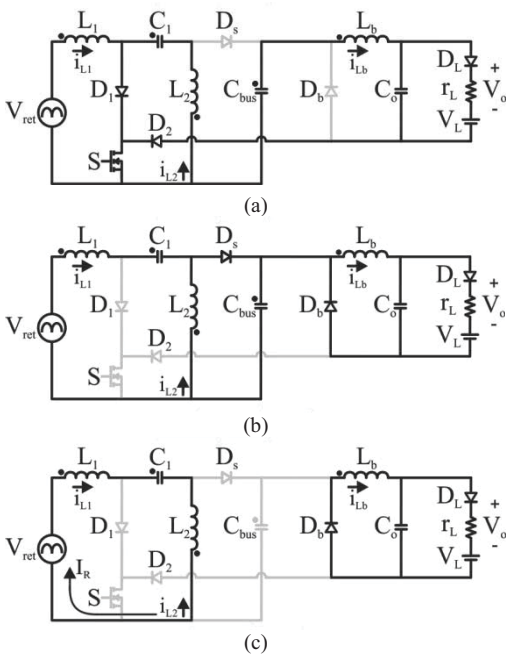

Fig. 5. First (a), second (b) and third (c) operational stage of the IC.

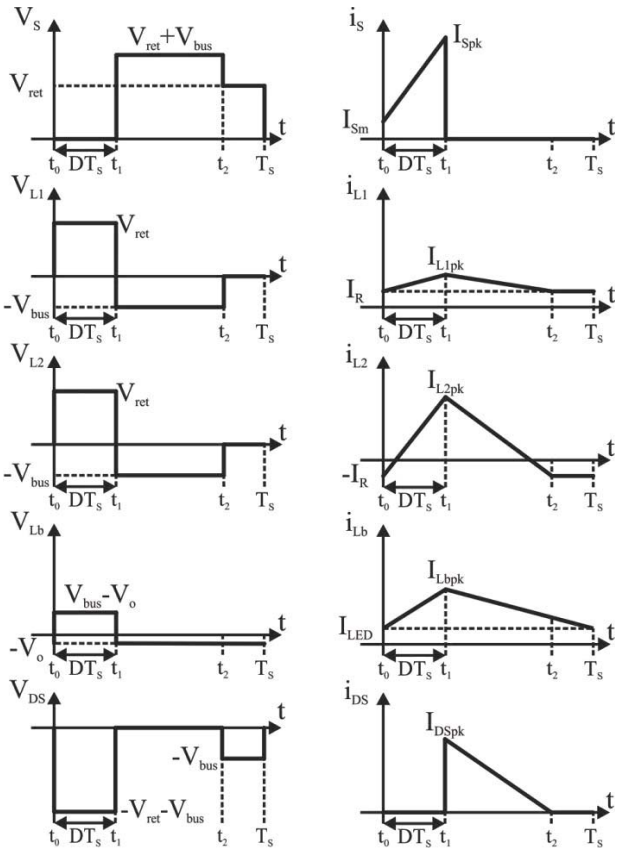

Fig. 6. Main waveforms of the IC.

First stage ($t_0 \leq t < t_1$): In this stage the shared switch S is turned on according to the duty cycle D. The switch current stress is defined by the sum of SEPIC typical on current (i_{L1} + i_{L2}) and Buck typical on current (i_{Lb}). The bus capacitor C_{bus} assures the delivered output power.

Second stage ($t_1 \leq t < t_2$): At this time, the switch is turned off and the diodes D_s and D_b conduct. The sum of the i_{L1} and i_{L2} currents flows through D_s. During this period the capacitor C_{bus} is charged until the current across D_s reaches zero.

Third stage ($t_2 \leq t < T_s$): In this stage, the Buck inductor L_b supplies the LED. The current i_{L1} is equal to $-i_{L2}$, called residual current I_R.

III. TOPOLOGY DESIGN

In this section, design equations and assumptions for the IC topology and its control circuitry are presented and analyzed.

A. SEPIC-Buck Design

According to the presented IC operational stages, the SEPIC and the Buck converter operate as each single converter. It allows designing each stage, PFC and PC, separately. The SEPIC operating under DCM may be represented using the equivalent circuitry shown in Figure 7 [20].

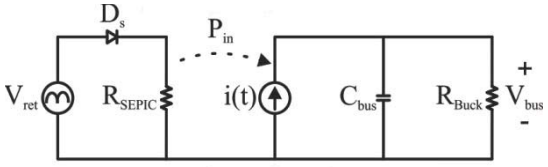

Fig. 7. Equivalent circuitry of the SEPIC in DCM.

The PFC stage instantaneous output current is represented by the current source *i(t)* in Figure 7, and is calculated through (1). The resistances R_{SEPIC} and R_{Buck}, representing the PFC and PC stages equivalent input resistances, are given by (2) and (3), respectively. A high PF is assured due to the resistive load emulation performed by the SEPIC stage for a constant D.

$$i(t) = \frac{D^2 T_s {V_{pk}}^2 sin^2(\omega t)}{2 L_{eq} V_{bus}} \tag{1}$$

$$R_{SEPIC} = \frac{2L_{eq}}{D^2 T_s} \tag{2}$$

$$R_{Buck} = R_o \frac{{V_{bus}}^2}{{V_o}^2} \tag{3}$$

The variable V_{pk} represents the peak value of the input voltage and L_{eq} corresponds to the parallel association of both inductances L_1 and L_2, and it is given by (4). The transferred input power P_{in} is determined by this inductance.

$$L_{eq} = \frac{{V_{pk}}^2 D^2 T_s}{4 P_{in}} \tag{4}$$

The inductances L_1 and L_2 are determined through (5) and (6), respectively. The input current ripple percentage Δi_{L1} is a design parameter. I_{pk} corresponds to the input current peak value, which is observed at the peak line voltage [21].

$$L_1 = \frac{V_{pk} D T_s}{I_{pk} \Delta i_{L1}} \tag{5}$$

$$L_2 = \frac{L_1 L_{eq}}{L_1 - L_{eq}} \tag{6}$$

It is assumed that the voltage across the capacitor C_1 is constant within a switching period, but at the same time it must follow the line voltage low frequency variation. When operating as PFC stage, the resonant frequency (f_{res}) given by C_1, L_1 and L_2 must be higher than the line frequency, in order to avoid input current oscillations within each line half cycle. Additionally, this resonant frequency must be lower than the switching frequency, so that a constant voltage within a switching period can be assured [21]. In this way, the capacitance C_1 may be calculated for a defined resonant frequency f_{res} (usually 1/10th of the f_s) through (7).

$$C_1 = \frac{1}{\left(2\pi f_{res}\right)^2 (L_1 + L_2)} \tag{7}$$

The output inductance L_b must be calculated assuring the CCM for the Buck converter. This is shown in (8), where $\Delta i L_b$ is the output high frequency current ripple percentage and I_{LED} is the average output current.

$$L_b = \frac{\left(V_{bus} - V_o\right) D T_s}{\Delta i L_b I_{LED}} \tag{8}$$

The bus capacitor C_{bus} is designed from (9), considering the maximum acceptable bus voltage ripple ΔV_{bus} and the average charging current $\langle I_{Cbus} \rangle$ through capacitor C_{bus}. This ripple is related to the output current ripple Δi_{LED} according to (10).

$$C_{bus} = \frac{\langle I_{Cbus} \rangle T_r}{2 \Delta V_{bus}} \tag{9}$$

$$\Delta V_{bus}(\Delta i_{LED}) = \frac{\Delta i_{LED} r_L I_{LED}}{D V_{bus}} \tag{10}$$

The DCM assures that the SEPIC behaves as an equivalent resistance to the line [20]. To guarantee the DCM at the PFC stage the maximum duty cycle is given by (11). The duty-cycle of a Buck converter in CCM is given by (12).

$$D_{max}(V_{bus}) = \frac{V_{bus}}{V_{pk} + V_{bus}} \tag{11}$$

$$D = D_{Buck}(V_{bus}) = \frac{V_o}{V_{bus}} \tag{12}$$

Therefore, the IC bus voltage must be chosen before defining D. This voltage must also assure the SEPIC DCM operation. According to the SEPIC topology, the voltage stress over the switch S is V_{pk}+V_{bus}. The switch current

waveform is given by the sum of the currents from PFC and PC stages. Thus, the switch current is determined in (13).

$$i_S(t)=\begin{cases}\left(\frac{V_{in}(t)}{L_{eq}}+\frac{(V_{bus}-V_o)}{L_b}\right)t+I_{LED}-\frac{(V_{bus}-V_o)DT_s}{2L_b} & if \quad t_o\le t<t_1\\ 0 & t_1\le t<T_s\end{cases} \quad (13)$$

The sum of the peak currents through the three inductors L_1, L_2 and L_b results in the current stress across the shared switch S (i_{Spk}), as shown in (14).

$$i_{S\,pk}=\frac{V_{pk}DT_s}{L_{eq}}+\frac{(V_{bus}-V_o)DT_s}{2L_b}+I_{LED}(1+\frac{\Delta i_{LED}}{2}) \quad (14)$$

The rms current across switch S is obtained by (15).

$$i_{S_{rms}}=\sqrt{\frac{1}{T_r}\int_0^{Tr}[i_S(t)]^2\,dt} \quad (15)$$

B. Control Circuitry Design

A classical control circuitry is designed for the IC topology aiming to minimize the output current ripple through varying D. It makes possible to reduce the bus capacitance C_{bus} value. However the input current harmonic content must be observed, because this control action increases the THD and it cannot meet the standard. Therefore the designed Buck converter operating in CCM is modeled through the state space averaging method for small signals yielding the converter transfer function G(s) as shown in (16). Table I presents the Buck converter parameters. This equation relates the output current over duty cycle variation in frequency domain.

TABLE I
CCM Buck converter modeling parameters

Bus voltage	V_{bus}= 170 V
Switching frequency, Duty cycle	f_s = 48 kHz, D = 0.303
LEDs threshold voltage	V_L = 45 V
LEDs dynamic resistance	r_L = 2.77 Ω
Buck inductance	L_b= 3.5 mH
Output capacitance	C_o= 10 nF

$$G(s)=\frac{4.81\cdot10^4 s+1.737\cdot10^{12}}{s^2+3.61\cdot10^7 s+2.83\cdot10^{10}} \quad (16)$$

Figure 8 shows the simplified structure of the system where K(s) and H(s) are the controller transfer function and the current sensor transfer function, respectively.

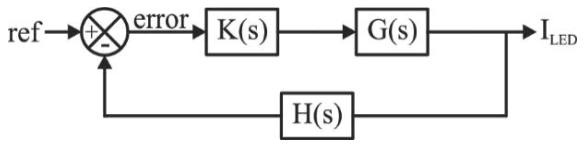

Fig. 8. Simplified scheme of the system.

A proportional integral (PI) controller is chosen due to its capability to increase the open-loop gain for low frequencies. The controller design is done through Bode diagram tool. Firstly a real pole is added at the origin to assure low steady-state error. A real zero is inserted in 180 Hz to keep a satisfactory phase margin.

The chosen gain margin is given by the controller transfer function and the CCM Buck converter transfer function model simulation under bus voltage variation for distinct gain margins observing the minimal output current ripple. The chosen gain margin returns 50% output current ripple considering a 25 µF bus capacitance, which is the minimal feasible value according to the complete topology simulation for the given bus voltage ripple.

The design procedure also complies two criteria: input current THD and output current ripple, fulfilling the standard and the LED manufacture requirements [7].

C. Dimming Strategy

The PWM dimming strategy is the best choice in terms of chromatic stability for power LEDs [22]. The output delivered current is controlled according to the current sensor C_{sense}. Thus the control circuitry allows using a dimmable circuit formed by an LED parallel switch without need controlling LED current dynamic for each switching period, as it is need for series switch dimmable technic. The proposed dimmable circuit is presented in Figure 9.

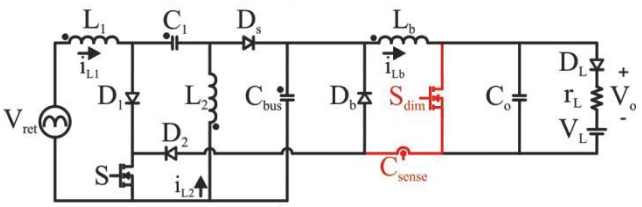

Fig. 9. IC schematic within dimming circuit and control reference.

By varying the S_{dim} duty cycle the LED average current changes, providing the dimming action.

The LED intrinsic voltage source characteristic assures low output voltage ripple. This ripple depends on the intrinsic LED dynamic resistance. Moreover since the Buck converter is operating in CCM, the capacitance C_o can be not necessary. However a small capacitance C_o= 10 nF is employed in order to avoid output voltage noise. This capacitance does not cause relevant effects to the switch S_{dim} because of its relative small value.

IV. PROTOTYPE

In this section the IC prototype design is presented. Table II shows the parameters and the components of the system.

The load is formed by two Bridgelux LED arrays in series, model BXRA-C4500. Each module generates a 5600 K cool-white light, with a typical luminous flux of 5 klm, generating a total flux around 10 klm. Typical voltage and current for each module are 25.4 V and 2.1 A, resulting in a total voltage of 50.8 V with the same current, giving a total equivalent resistance R = 24.2 Ω. According to the tangent traced across the I-V curve [23] the threshold voltage and dynamic

resistance of the LED array can be found. Thus, the result is V_L = 45 V and r_L = 2.77 Ω, defining the load model.

TABLE II
System Parameters and Components

Design Specifications	
Input RMS voltage, Line frequency	V_{in} = 220 V, f_r = 60 Hz
Switching frequency, Duty cycle	f_s = 48 kHz, D = 0.303
Output power, Efficiency	P_{out} = 106 W, η = 85%
Output current, Output current ripple	I_{LED} = 2.1 A, Δ i_{LED} = 50%
Inductors current ripple	Δ i_{L1} = Δ i_{Lb} = 10%
Bus voltage, Resonance frequency	170 V, f_{res} = 3.2 kHz
Controller Specifications	
Gain margin, Phase margin	Gm = 0.3 dB, PM = 88°
Cut-off frequency, Steady state error	Fc = 2 kHz, err = 0
Current sensor	C_{sense}: ACS712ELCTR-05B-T
LED Lamp Parameters	
2 Bridgelux LED array	Model: BXRA-C45000
Threshold Voltage, Dynamic Resistance	V_L = 45 V, r_L = 2.77 Ω

Component	Specification	Model	Value
D_{A-D}	Rectifier diodes	1N4007	1A, 1000 V
SEPIC-Buck			
D_1	Diode	UF5408	3 A, 1000 V
D_2, D_B	Diode	15TH06	15 A, 600V
D_S	Diode	MUR4100	4 A, 1000 V
S	MOSFET	FQA10N80C	10 A, 800 V
S_{dim}	MOSFET	IRF620	6 A, 200 V
L_1, L_2, L_b	Inductor	24. 3 mH, 437 µH, 3.5 mH	
C_1 , C_{bus}, C_o	Capacitor	100 nF, 25 µF, 10 nF	

First, the bus voltage of the IC is defined, and then the duty cycle. Figure 10 shows a relation between the maximum duty cycle D_{max}, obtained through (11), and the duty cycle D, obtained by (12), which must be chosen for a specific bus voltage V_{bus}, considering a 220 V_{RMS} input voltage.

In order to avoid high voltage stress across the switch, and assure the DCM for the SEPIC, the bus voltage is defined as V_{bus} = 170 V which is 10% above the point where the curves matches each other. The resulting duty cycle is D = 0.303 (below the maximum value 0.356).

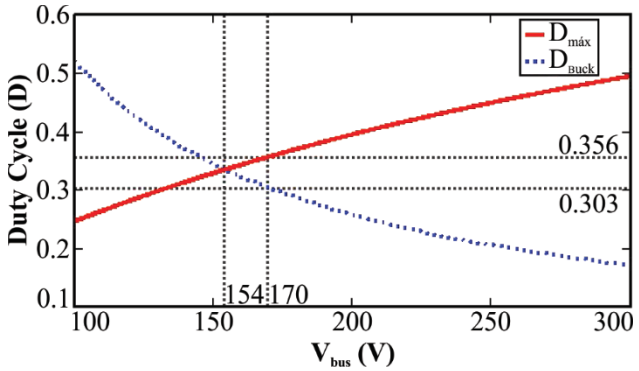

Fig. 10. Duty cycle definition according to V_{bus}.

The inductor L_1 and L_2 are calculated through (5) and (6). According to (7) and f_{res}, the capacitor C_1 is calculated. The capacitor C_{bus} is chosen according to the relation between the bus voltage ripple ΔV_{bus} and the output current ripple Δi_{LED} for the open-loop configuration. If a Δi_{LED}=50% is chosen, for a V_{bus}= 170 V, the corresponding bus capacitor is C_{bus}= 187.5 µF, for instance, as shown in Figure 11.

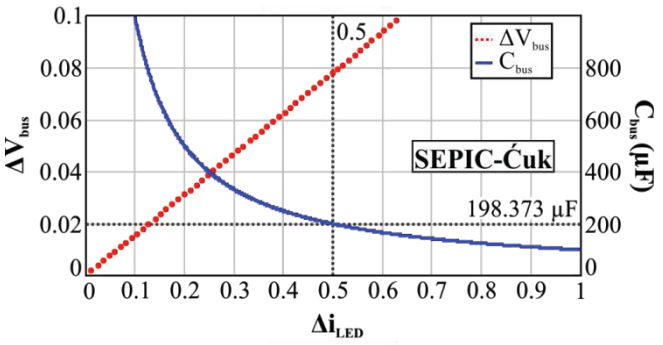

Fig. 11. Bus voltage ripple ΔV_{bus} and bus capacitance C_{bus} definition according to the current ripple Δi_{LED} for open-loop configuration.

The current ripple Δi_{LED} = 50% does not cause a visible flicker to the human eye [24]. In [25] power LEDs are tested under 50% current ripple and the luminous flux and luminous efficiency drop under 1% and 2% respectively. Through the control technique this capacitance is significantly reduced to only C_{bus}= 25µF, as shown in Section III-B. It makes possible the use of larger lifetime capacitor technologies, i.e. film capacitor technology. Even if long lifetime electrolytic capacitors have been commercialized, the cost of these components is substantially superior compared to film capacitors [26].

V. EXPERIMENTAL RESULTS

The main experimental waveforms are shown in this section, thus validating the proposed converter design and control methodologies. It is divided in three sub-sections A, B, and C. First relates the open-loop topology waveforms with the first calculation of the bus capacitance C_{bus} = 187.5 µF. The sub-section B relates the closed-loop topology which allows for using the bus capacitance C_{bus}=25 µF resulting Δi_{LED}=50%. Third sub-section presents the dimming results considering the same circuit specifications for sub-section B. In the sub-section A the implemented bus capacitor uses the electrolytic technology while the film technology is applied in sub-sections B and C.

A. Open-Loop Topology Using Larger Capacitor

According to Section III, the open-loop design result in a bus capacitance C_{bus}=187.5 µF, complying the output current ripple and the bus voltage ripple. Figure 12 shows the low-frequency bus voltage ripple waveform and the output current ripple waveform.

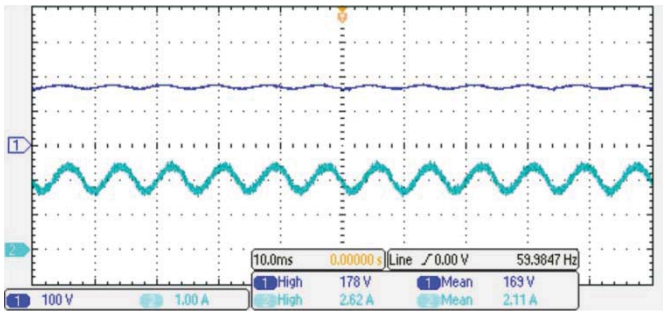

Fig. 12. Bus voltage (Ch. 1, 100 V/div) and LED current (Ch. 2, 1 A/div). Horizontal scale: 10 ms/div.

The average value of the waveforms is close to the design one. An output current ripple Δi_{LED}=48.3% can be observed while the bus voltage ripple ΔV_{bus} remains 10.6%. The same waveforms are presented by Figure 13 for 20 µs time window.

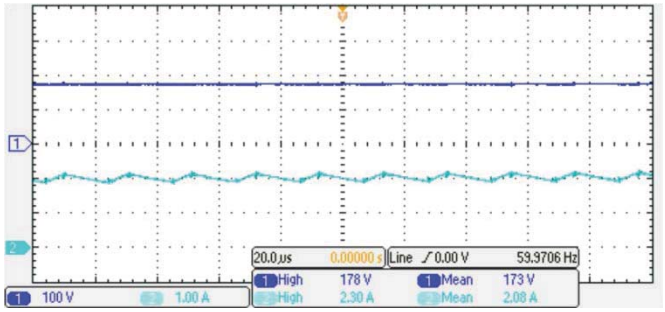

Fig. 13. Bus voltage (Ch. 1, 100 V/div) and LED current (Ch. 2, 1 A/div). Horizontal scale: 20 µs/div.

Figure 14 presents the input voltage and current waveforms and the instantaneous input power. The measured power factor is 0.99. The topology reached a THD = 4.79%.

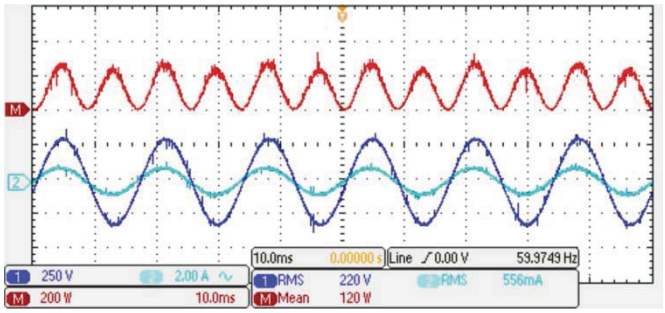

Fig. 14. Input power (Ch. M, 200 W/div), voltage (Ch. 1, 250 V/div) and current (Ch. 2, 2 A/div). Horizontal scale: 10 ms/div.

The LED output power, the current and voltage are shown by Figure 15. An efficiency of 87.5% has been measured, which was near the estimated one. However the driver power has not been considered.

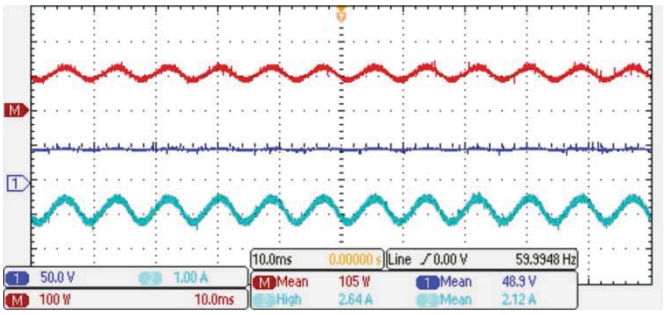

Fig. 15. Output power (Ch. M, 100 W/div), voltage (Ch. 1, 50 V/div) and current (Ch. 2, 1 A/div). Horizontal scale: 10 ms/div.

B. Closed-Loop Topology Using Smaller Capacitor

The controller specifications are previously given in Table II. The control circuitry allows for bus capacitance reduction. The input current harmonic component has to be observed according to this reduction. A bus capacitance C_{bus}=25 µF generates an output ripple Δi_{LED}=50%. The input current harmonic content agrees with standard [11]. Figure 16 presents the low-frequency bus voltage ripple waveform and the output current ripple waveform.

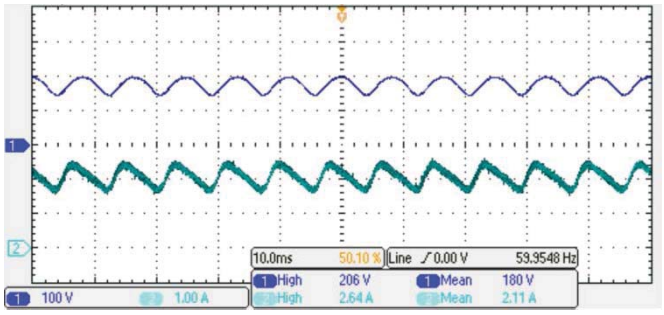

Fig. 16. Bus voltage (Ch. 1, 100 V/div) and LED current (Ch. 2, 1 A/div). Horizontal scale: 10 ms/div.

The average value of the waveforms was kept very close to the designed one as in the previous sub-section. However the voltage and current ripple get significantly superior. The output current ripple Δi_{LED}=50.23% can be observed while the bus voltage ripple ΔV_{bus} remains around 28.88%. A 20 µs window for the same waveforms is shown in Figure 17.

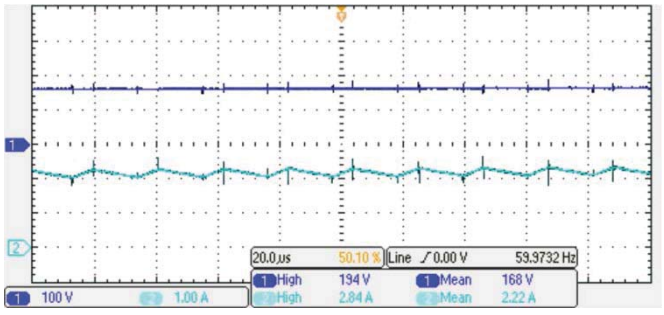

Fig. 17. Bus voltage (Ch. 1, 100 V/div) and output current (Ch. 2, 1A/div) and. Horizontal scale: 20 µs/div.

Figure 18 shows the input voltage, current and power waveforms. The measured power factor is 0.98.

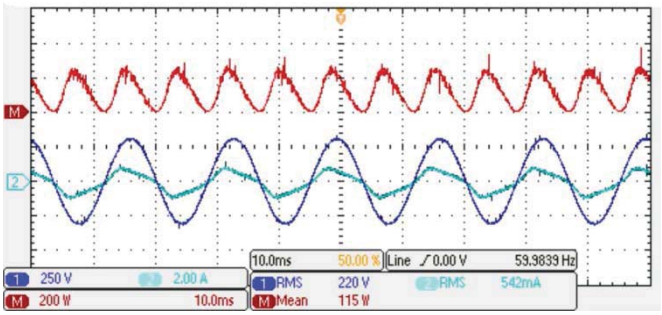

Fig. 18. Input power (Ch. M, 200 W/div), voltage (Ch. 1, 250 V/div) and current (Ch. 2, 2 A/div). Horizontal scale: 10 ms/div.

The harmonic spectrum for the input current is shown in Figure 19, comparing to the standard [11]. The THD is 17.1%. The harmonic content and efficiency are calculated extracting 15,000 oscilloscope acquisition points of each waveform.

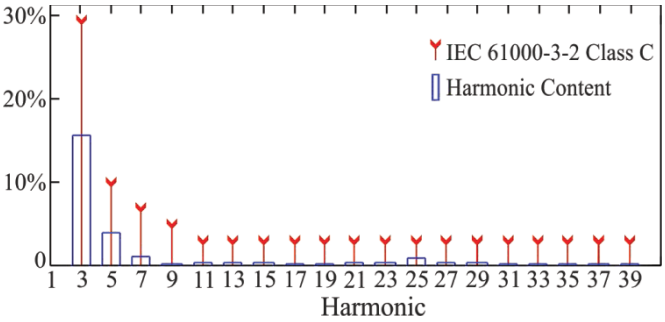

Fig. 19. Input current harmonic content (C_{bus} = 25 µF).

The LED output power, the current and voltage are shown in Figure 20. An efficiency of 92.18% is reached.

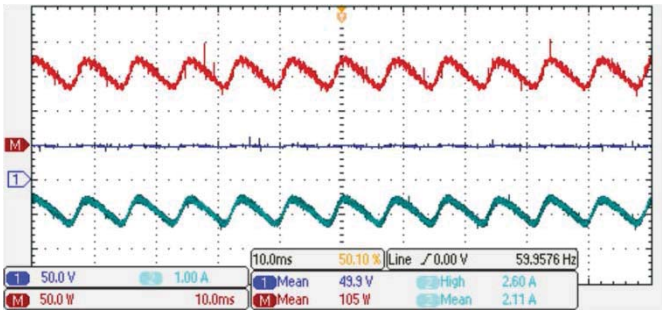

Fig. 20. Output power (Ch. M, 50 W/div), voltage (Ch. 1, 50 V/div) and current (Ch. 2, 1 A/div). Horizontal scale: 10 ms/div.

Figure 21 presents the switch S power, voltage and current waveforms. The switching losses are less than 6 W for the nominal output power.

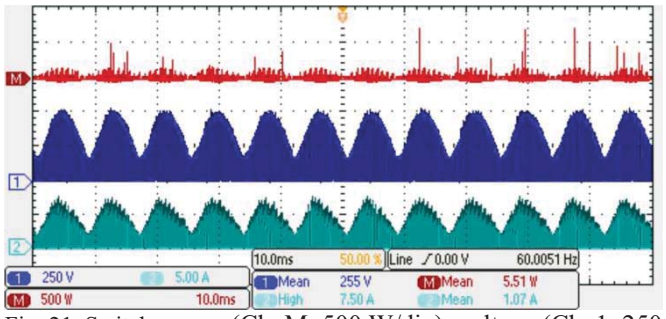

Fig. 21. Switch power (Ch. M, 500 W/div), voltage (Ch. 1, 250 V/div) and current (Ch. 2, 5 A/div). Horizontal scale: 10 ms/div.

C. Dimmable Circuit

By using the bus capacitor C_{bus}=25 µF, the dimmable circuit is experimented in this sub-section. Figure 22 presents the output power, voltage and current for a 0.50 duty cycle applied to S_{dim}. This duty cycle is proportional to the 50% of the LED nominal current. The dimming frequency is defined as 24 kHz which is out of the human audible frequency range.

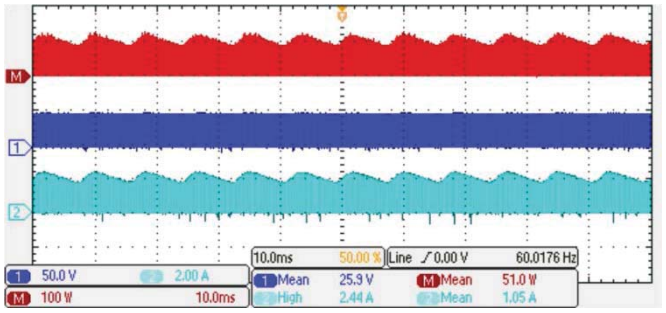

Fig. 22. Output power (Ch. M, 100 W/div), voltage (Ch. 1, 50 V/div) and current (Ch. 2, 2 A/div). Horizontal scale: 10 ms/div.

Figure 23 presents the bus voltage and output current waveforms for a dynamic behavior. The topology is under nominal operation until the transition where the dimming circuit is turned on under 50%. The bus voltage decreases as expected.

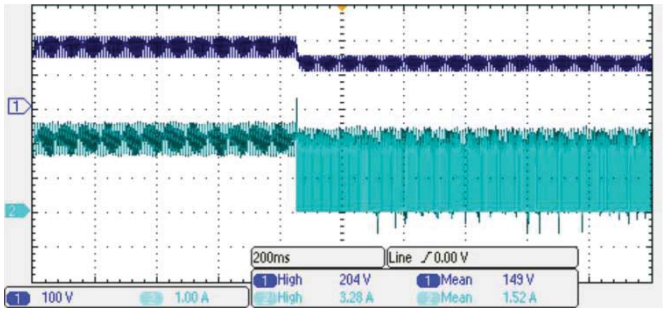

Fig. 23. Bus voltage (Ch. 1, 100 V/div) and output current (Ch. 2, 1 A/div). Horizontal scale: 200 ms/div.

This dimming circuit is very simple and easy feasible for Buck topology. The dimmable output current I_{LED} is compared to the converter efficiency η, power factor and THD in Figure 24 for dimming values from 10% to 90%. All cases complies the input current harmonic content standard,

validating the proposed idea as a very simple, low cost and efficient full range dimming solution.

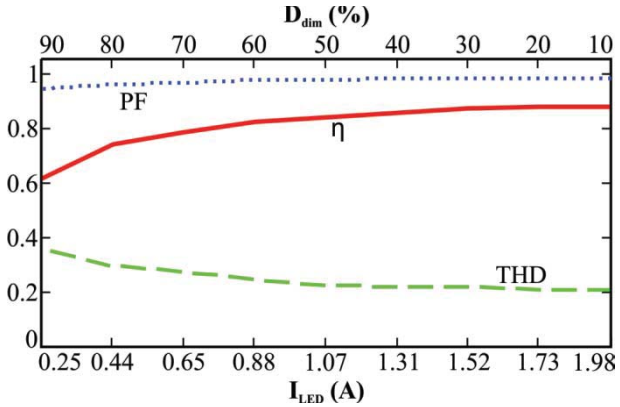

Fig. 24. Dimmable output current x PF, η and THD.

The S_{dim} power dissipation is also observed and it does not exceed 3 W for the worst case, where the dimming duty cycle is 0.9. For 50% output current the S_{dim} power dissipation is less than 1 W.

Comparative results are summarized in Table III according to the results of sub-sections A and B. It relates the efficiency, LED low frequency ripple and the THD of each sub-section.

TABLE III
Comparison

Sub-Section Specifications	η (%)	LED ripple (%)	THD (%)
A: Open Loop, C_{bus}= 187.5 μF	87.5	48.3	4.79
B: Closed Loop, C_{bus}=25 μF	92.18	50.23	17.1

VI. CONCLUSION

In this paper a study of the integrated SEPIC-Buck converter for LED lighting has been accomplished. The integrated converter was analyzed for the SEPIC operating in DCM and the Buck converter operating in CCM. The components design is done defining an LED current ripple. A ratio of current ripple to voltage ripple at the bus capacitor is presented to find its capacitance. Through modeling the topology, a PI controller is designed and the bus capacitance minimization is allowed. The capacitance reduction allows replacing the electrolytic capacitor with film capacitor, increasing the lifetime of the lighting system. It also allows implementing a very simple PWM dimmable circuit which provides distinct LED average currents.

A prototype has been built and the experimental results have shown the satisfactory behavior of the circuit. The result for the open-loop circuitry has shown that the output current ripple increases by the reduction of the bus capacitor. This reduction is possible when the controller is well designed to keep the desired LED current ripple.

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Marcelo Freitas da Silva was born in São Paulo, Brazil, in 1970. He received the B.S., M.Sc. and Ph.D. degree in electrical engineering from the Federal University of Santa Maria, Santa Maria, Brazil, in 1995, 2000 and 2012, respectively. He is currently working toward the Ph.D. degree in power electronic applied to lighting systems. Since 1993, he has been with the Federal University of Santa Maria, where he is currently a Professor in the Colégio Técnico Industrial de Santa Maria (CTISM). He also serves as a Reviewer for IEEE journal and conferences in the field of power electronics. He has been with the Electronic Ballast Research Group (GEDRE), Federal University of Santa Maria, as a Researcher. Electrical and Computational Systems Research and Development Group (GSEC) since 2010. His research interests include electronic ballasts, lamps, dimming systems, power factor correction, fluorescent lamps and LEDs.

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Prof. Alonso has been awarded with the Early Career Award of the IEEE Industrial Electronics Society in 2006. He was honoured with the University of Oviedo Electrical Engineering Doctorate Award for 1996. He also holds three IEEE paper awards. Since 2002 he serves as an Associate Editor of the IEEE Transactions on Power Electronics. He has been Co-Guest Editor of two special issues in lighting applications published in the IEEE Transactions on Power Electronics (2007) and IEEE Transactions on Industrial Electronics (2012) and has co-organized several conference special sessions. He also serves as secretary of the IEEE IAS Industrial Lighting and Display Committee (ILDC). He has been elected as Member-at-Large of the IEEE IAS Executive Board for the term 2013-2014. He is also member of the European Power Electronics Association and he belongs to the International Steering Committee of the European Conference on Power Electronics and Applications (EPE), where he has collaborated as topic co-chair since 2007.

Ricardo Nederson do Prado was born in Itapiranga, Brazil, in 1961. He received the B.Sc.degree from the Federal University of Santa Maria, Santa Maria, Brazil, in 1984, and the M.Sc. and Ph.D. degrees from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1987 and 1993, respectively, all in electrical engineering. From 1987 to 1992, he was an assistant Professor in the Electronics Department, Federal University of Minas Gerais, Belo Horizonte, Brazil. Since 1993, he has been with the Federal University of Santa Maria, Brazil, where he is currently an Associate Professor in the Electrical Energy Processing Department. In 1997, He founded the Electronic Ballast Research Group (GEDRE). From 2005 to 2006, he was with the Fraunhofer Institute, Sankt Augustin, Germany, as a Postdoctoral Research Scholar. He has authored more than 250 technical papers published in conference proceedings and magazines. His research directions include high-frequency high-density power converters, fluorescent and high-pressure lamps, dimming systems, luminous efficiency, electronic ballasts, LED as a source light and power-factor correction. Dr. Prado is a founding member of the Brazilian Power Electronics Society, member of Brazilian Automatic Control Society, and several IEEE societies. Dr. Prado is a reviewer of the Brazilian Power Electronics Society, Brazilian Automatic Control Society, and several IEEE societies.