MODULATION TECHNIQUE APPLIED FOR THD REDUCTION IN 3-LEVEL FLYING CAPACITOR MULTILEVEL INVERTER

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***Abstract* – This paper introduces a modulation technique for a three-level flying capacitor multilevel inverter applied in total harmonic distortion reduction. The proposed modulation improves power quality, reducing the total harmonic distortion and combining the advantages of two modulation techniques: HE-PWM and CSV-PWM. In order to validate the proposed method, the THD analysis, the loss study and the experimental results are shown concerning a three-level 6 kW 0.92 power factor flying capacitor inverter. The total harmonic distortion experimental results presented line voltage around 42.09% and phase voltage around 79.06%.**

***Keywords* - Flying Capacitor, Modulation Technique, Multilevel Inverter, THD Reduction.**

I. INTRODUCTION

In recent years, multilevel inverters are increasingly presenting themselves as viable and effective applications, especially for high power motor drives [1], [2]. Given the voltage and current levels in electrical systems, electronic devices are been used in the expansion of energy capacity. However, these systems produce major efforts in semiconductors and they need an energy conversion with reduced harmonic content [3].

The capacitors and semiconductors array of the multilevel inverters contributes to their main feature: allow the output voltage to reach three or more levels. Although, the increase in the number of levels results in a more complex modulation, as well as problems of unbalanced voltage on the bus capacitors and the increasing number of components [4].

The researches to enhance the topologies of multilevel inverters are focused on reducing the total harmonic distortion (THD) and improving the modulation strategies, balancing the voltage at DC link and reducing the current ripple [5].

Among the well-known multilevel topologies, the Neutral-Point Clamped (NPC) presents several advantages such as the reduction of efforts on the switches and electromagnetic interference (EMI) effects while enhancing the quality of the voltage waveform. However, the NPC provides a voltage unbalance in bus capacitors while the Flying Capacitor (FC) topology, shown in Figure 1, presents an advantage over it: once the flying capacitor is balanced, the DC link capacitor is also balanced [4], [5]. Besides, it presents another advantage over other topologies which enables the inverter to operate in a wide variety of modulation techniques [6], [7].

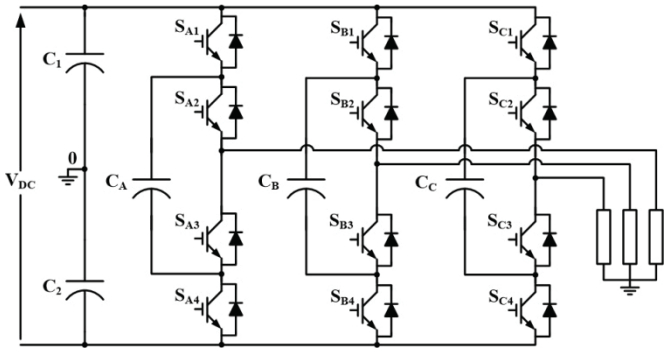

Fig. 1. Three-level flying capacitor multilevel inverter topology.

Although, it has an addition of capacitors in its structure, thus complicating their loading and unloading process, affecting the balance of the flying capacitor voltage levels in applications with more levels [8].

The Cascade H-Bridge (CHB) is another important multilevel topology which has fewer components to achieve the same number of output voltage levels. It is one of the most widely used topologies due to its reliability and increased capacity to operate under fault conditions in the cells but needing isolated sources for its operation [9].

Regarding the modulation techniques, these can be divided into two groups: pulse width modulation (PWM) and space vector modulation (SVM). Within the PWM group, the phase-shift modulation (PSPWM) is the most known, having triangular carriers and a sinusoidal modulator for each phase, which they are compared and determine how each converter leg to operate. The PSPWM is widely used in inverters for its simplicity [10].

A carrier-based PWM technique proposed in [11], named as HE-PWM in this paper, proved very effective to obtain low rates of harmonic distortion when it is desired even when the inverter operates at low modulation index. This feature is provided for its modified carriers configuration and compared with a sinusoidal modulator per phase.

Otherwise, in the SVM, a reference rotation phasor in the plane (α,β) is sampled within the switching period while each switching state of an inverter is defined as a point in complex space (α,β). Then, the three nearest states are selected with the calculated duty cycle to synthesize the desired average voltage during each switching period. Thus, the line voltages of the inverter are controlled directly allowing the THD reduction [12].

The CSV-PWM (Centered Space Vector - Pulse Width Modulation) proposed in [12] shows an adaptation on the

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modulator in space-vector domain in conjunction with triangular carriers in the time domain which resulted in good rates of THD.

Thus, this paper proposes a modulation to the flying capacitor topology combining the features of the carriers developed in [11] and the reference signals generation presented in [12], pursuing the quality improvement of the voltage across the load from the reduction of its harmonic content [1]. Compared to [1], this work also presents a better-detailed study of the modulation technique, loss study and theoretical THD analysis proven by the experimental results.

II. PROPOSED MODULATION TECHNIQUE

The proposed modulation combines the carrier introduced in [11] and the modulator based on SVM presented in [12], since both are characterized by reducing the total harmonic distortion of the output voltage when applied to multilevel inverters with flying capacitor.

Considering X = A, B, C. The S_{X1} and S_{X2} switches are controlled in a complementary way to the S_{X4} e S_{X3} switches, respectively, the modulation concepts are applied to the flying capacitor inverter multilevel, shown in Figure 1, having the following features:

- Each leg has 4 switching states and 3 output voltage levels (P = positive, O_1 = zero, O_2 = zero and N = negative);
- There are 27 possible switching states for the three level FC inverter which 19 vectors are effective and 8 vectors are redundant.

Figure 2 shows the proposed modulation carriers and modulators waveforms where the carrier P_1 is corresponding to S_{X1} switch and the carrier P_2 is corresponding to S_{X2} switch.

The reference waveforms V_{MA}, V_{MB} and V_{MC} are generated from an algorithm shown in [1]. The carriers can be separated into two regions: the bottom with a reference voltage between 0 and $V_P/3$ and the upper is between $V_P/3$ and V_P. Each region is chosen according to the reference voltage magnitude.

Figures 3, 4 and 5 present the modulator waveforms (summarized as V_{REF}), carriers (P_1 and P_2) and their corresponding gate signals (V_{GSX1} and V_{GSX2}) when reference voltage is between (0 and $V_P/3$), ($V_P/3$ and $2V_P/3$) and ($2V_P/3$ and V_P). The waveforms follow the same pattern of the HE-PWM modulation having a remarkable similarity [11]. However, in the proposed modulation there are intervals that change the duty cycle and, consequently, the charging and discharging processes of the flying capacitor.

Thus, the gate signal V_{GS1} (referred to switch S_{X1}) comes from the comparison between the reference and the carrier P_1, and the gate signal V_{GS2} (referred to switch S_{X2}) comes from the comparison between the reference and the carrier P_2.

In Figure 3 is shown the case where the reference voltage is between 0 and $V_P/3$. The order of the resulting switching states is "O-N-O-N-O". It is noticed that the flying capacitor voltage balance could not be achieved as in the HE-PWM [11]. This is caused by the regions that change the duty cycle ranges and, consequently, the amount of charge that the capacitor takes in and out.

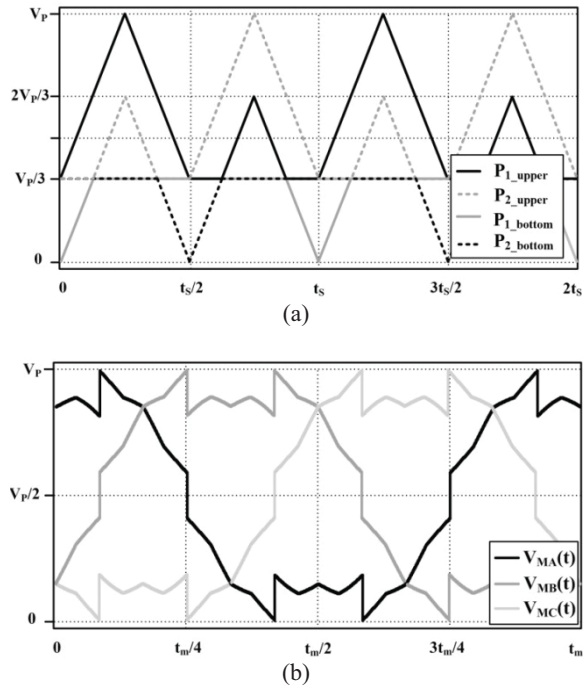

Fig. 2. Proposed modulation waveforms: (a) carriers (b) modulators.

When the reference voltage is between $V_P/3$ and $2V_P/3$, as shown in Figure 4, the order of switching states is shown as "P-O-N-O-P-O-N-O-P".

When the reference voltage is between $2V_P/3$ and V_P, as shown in Figure 5, the resulting switching states are "P-O-P-O-P".

It is observed that in all cases, there are intervals where the duty cycle does not allow the symmetric charging and discharging time and the flying capacitors do not reach equilibrium in the same way that the HE-PWM (see [11]). Symmetric would be reached when same switching states (P, O or N) have equal time intervals. This may be one drawback of the proposed modulation. Nevertheless, in experimental situation, this disadvantage is not significant on the use of a high switching frequency.

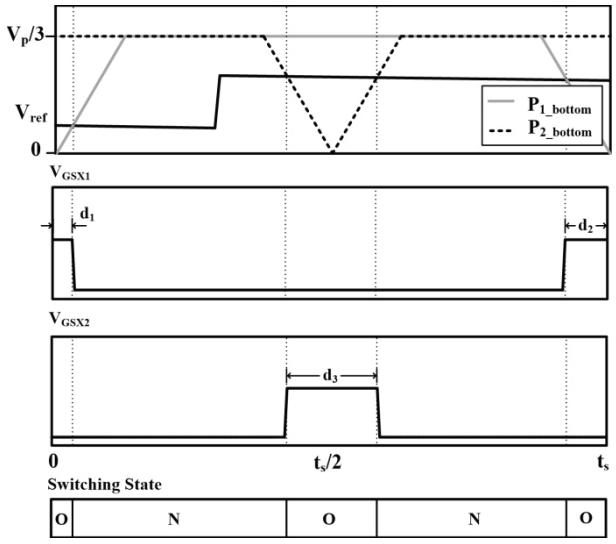

Fig. 3. The proposed modulation principle when the reference voltage is between 0 and $V_P/3$.

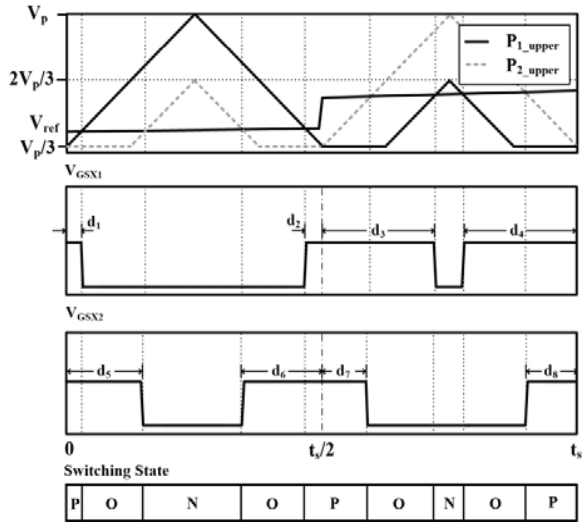

Fig. 4. The proposed modulation principle when the reference voltage is between $V_P/3$ and $2V_P/3$.

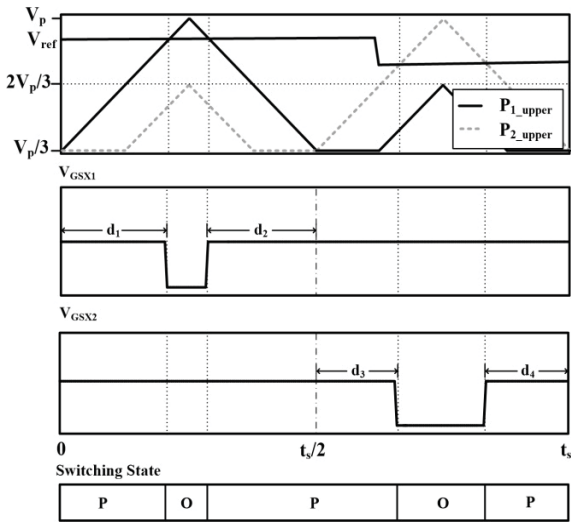

Fig. 5. The proposed modulation principle when the reference voltage is between $V_P/3$ and $2V_P/3$.

III. LOSS STUDY

Due to the higher complexity to determine the modulation functions with the HE-PWM, CSV-PWM and proposed modulations, Tables I, II, and III show, respectively, their current efforts in the components for one inverter leg, where X is the phase (A, B, C) and Y is the switch (1, 2, 3, 4) obtained through simulation on PSIM® software. The flying capacitor currents are determinated on Table IV. The inverter specifications for the loss study are shown in Table V.

TABLE I
Current efforts in the switches/diodes (HE-PWM)

	Average current (A) $I_{SXY.AVG}$	RMS current (A) $I_{SXY.RMS}$
S_{A1}	8.513	14.902
S_{A2}	8.516	14.904
S_{A3}	8.495	14.884
S_{A4}	8.493	14.883
D_{A1}	1.787	6.240
D_{A2}	1.785	6.237
D_{A3}	1.787	6.241
D_{A4}	1.790	6.246

TABLE II
Current efforts in the switches/diodes (CSV-PWM)

	Average current (A) $I_{SXY.AVG}$	RMS current (A) $I_{SXY.RMS}$
S_{A1}	6.983	12.562
S_{A2}	6.967	12.553
S_{A3}	7.097	12.724
S_{A4}	7.112	12.731
D_{A1}	1.914	6.247
D_{A2}	1.929	6.263
D_{A3}	1.897	6.188
D_{A4}	1.881	6.171

TABLE III
Current efforts in the switches/diodes (proposed modulation)

	Average current (A) $I_{SXY.AVG}$	RMS current (A) $I_{SXY.RMS}$
S_{A1}	5.638	10.557
S_{A2}	5.652	10.569
S_{A3}	5.717	10.646
S_{A4}	5.707	10.638
D_{A1}	1.971	5.685
D_{A2}	1.961	5.669
D_{A3}	1.934	5.630
D_{A4}	1.947	5.653

TABLE IV
Current efforts in the capacitors

	RMS current (A)
HE-PWM	9.432
CSV-PWM	12.426
PROPOSED	11.254

TABLE V
Design parameters for one inverter leg

Output active power (P_o)	2 kW
Bus voltage (V_{DC})	400 V
Switching frequency (f_s)	1080 Hz
Load power factor (PF)	0.92
Converter efficiency (η)	0.95
Output voltage frequency (f_o)	60 Hz
Modulation index (m_a)	0.8

According to [13]-[15], the conduction losses across the switches and diodes can de determinated using (1) and (2).

$$P_{SXY.COND} = V_{TO} \cdot I_{SXY.AVG} + R_S \cdot I^2_{SXY.RMS} \quad (1)$$

$$P_{DXY.COND} = V_D \cdot I_{DXY.AVG} + R_D \cdot I^2_{DXY.RMS} \quad (2)$$

The commutation losses across the switches are calculated from (3) to (6), while the reverse recovery losses associated to the diodes are determined using (7) and (8). The procedure to calculate all the used parameters is presented in [13]-[15].

$$W_{SXY.ON} = k_{0.ON} + k_{1.ON} \cdot I_{SXY}(\omega t) + k_{2.ON} \cdot I^2_{SXY}(\omega t) \quad (3)$$

$$W_{SXY.OFF} = k_{0.OFF} + k_{1.OFF} \cdot I_{SXY}(\omega t) + k_{2.OFF} \cdot I^2_{SXY}(\omega t) \quad (4)$$

$$P_{SXY.ON} = \frac{1}{2\pi} \cdot \int_0^{2\pi} f_s \cdot W_{SXY.ON}(\omega t) \cdot d(\omega t) \quad (5)$$

$$P_{SXY.OFF} = \frac{1}{2\pi} \cdot \int_0^{2\pi} f_s \cdot W_{SXY.OFF}(\omega t) \cdot d(\omega t) \quad (6)$$

$$W_{rr}(\omega t) = \frac{V_{CC}}{2} \cdot t_{rr} \cdot \left(0.35 \cdot I_{rrN} + 0.15 \cdot \frac{I_C}{I_{CN}} \cdot i_{rrN} + i_C\right) \quad (7)$$

$$P_{rr} = \frac{1}{2\pi} \cdot \int_0^{2\pi} f_s \cdot W_{rr}(\omega t) \cdot d(\omega t) \quad (8)$$

Table VI presents the calculated overall losses for one leg of the flying capacitor multilevel inverter. The adopted switches are IGBT GP50B60D1 while the diodes are MUR 860. Besides, Figure 6 shows the losses distribution for the modulations HE-PWM, CSV-PWM and proposed.

Although Table IV shows that flying capacitor currents of proposed modulation are higher than HE-PWM, Tables I, II, and III demonstrate that the proposed modulation has lower currents (average and RMS) in switches and diodes. Thus, Table VI and Figure 6 presents that overall losses and the losses distribution, respectively, are lower and better when compared to HE-PWM and CSV-PWM. The reason is that the peak amplitude of the proposed modulation never reaches the maximum value of the carrier (even for modulation index equal to 1) combined with the carrier based on HE-PWM.

TABLE VI
Overall losses for the different modulation techniques for one inverter leg

	Losses (W)
HE-PWM	75.26
CSV-PWM	82.34
PROPOSED	70.71

IV. THD ANALYSIS

In order to evaluate the total harmonic distortion of the inverter unfiltered line voltage with different modulation techniques applied to the flying capacitor topology, simulations were performed for various modulation indexes in PSIM® software.

In Figure 7 is shown the THD simulation results for the modulations PSPWM, LSPWM-POD, CSV-PWM and the proposed modulation by varying modulations indexes where the performance of the proposed modulation technique is superior to the entire range of modulation index, surpassing other conventional techniques.

In Figure 8 is made a THD comparison between the HE-PWM and proposed modulation and it can be noticed that when the modulation index values are between 0 and 0.4, both modulations have the same performance, but this range is not much used in practice, but when the values are between 0.4 and 1 the proposed modulation presents a level of THD to 5% less than the HE-PWM modulation, proving its efficacy.

In addition to the THD rates comparison, it is interesting to show the efficiency of the proposed modulation technique by equations which represent the output voltage and include harmonic components of high and low frequencies.

The output voltage analysis of the proposed modulation applied to the flying capacitor multilevel inverter is performed based on [16] which expresses the output phase voltage as a function of the fundamental frequency, the carrier frequency and its harmonics and the function f(t) decomposed through Fourier series. Once the equations are determined, the resulting unitary cell of the inverter is obtained, Figure 9.

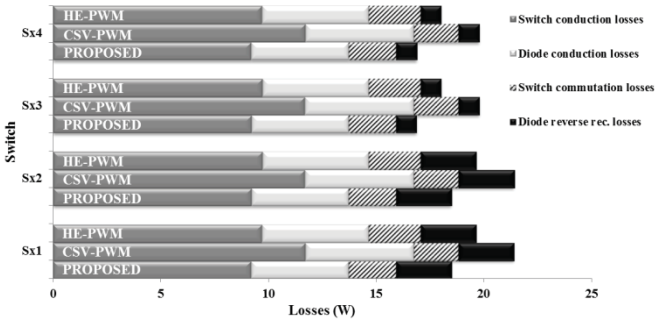

Fig. 6. Switches and diodes losses distribution for the modulations HE-PWM, CSV-PWM and proposed.

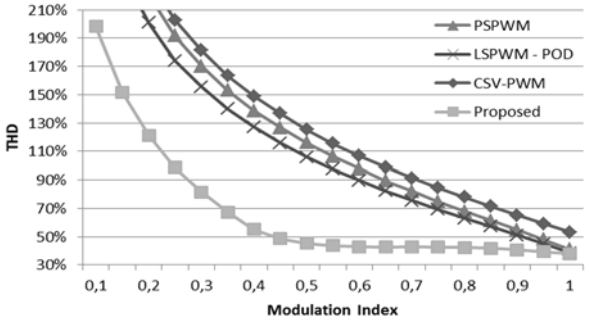

Fig. 7. THD results for output line voltage with PSPWM, LSPWM-POD, CSV-PWM and proposed modulation.

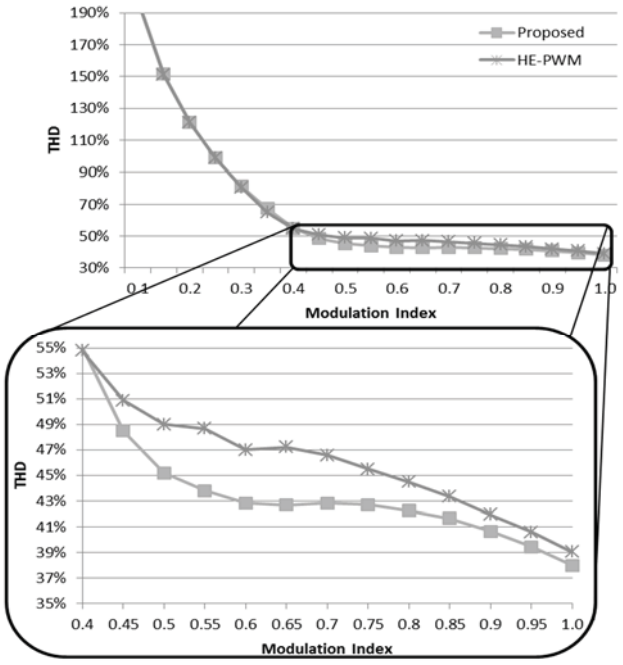

Fig. 8. THD results for output line voltage with HE-PWM and proposed modulation.

The variables x(t) and y(t) stand for the instantaneous angles to switching and fundamental frequencies, respectively. It this way, this analysis conducts to determine analytically the amplitude of each harmonic component.

In Figure 10 is shown a simplified diagram in time resulted from the comparison between the reference and the unitary cell functions. For comparison, Figure 11 presents the output

phase waveform obtained from PSIM® software simulation where it can be observed the similarity between them.

From the analysis of the unitary cell and the Fourier transform, it is possible to determine the equations for the calculation of the phase voltage harmonic components as it will be shown in results.

V. RESULTS

Figure 12 presents the theoretical results for the first 51 output voltage harmonics with a modulation index of 0.8 and switching frequency equal to 1080 Hz.

Figures 13 and 14 show the theoretical study comparisons with the simulated phase voltage and the line voltage, respectively, where there are great similarity between the results and validating the presented study. The simulation results presented THD rates of 78.52% and 41.38% for phase and line voltages, respectively, and for the calculated THD values from the study presented 75.23% and 39.35% for phase and line voltages, respectively.

Figure 15 shows the five levels of line voltage, the three levels of phase voltage and the line current and Figure 16 presents the voltage across the flying capacitors which indicate the negligible unbalance stated in section II.

In Figures 17 and 18 are shown the experimental results of line and phase voltage harmonic spectrum and THD measurement, respectively, with 42.09% and 79.06% values.

Table VI shows the summary of the results obtained through the calculated, simulated and experimental values.

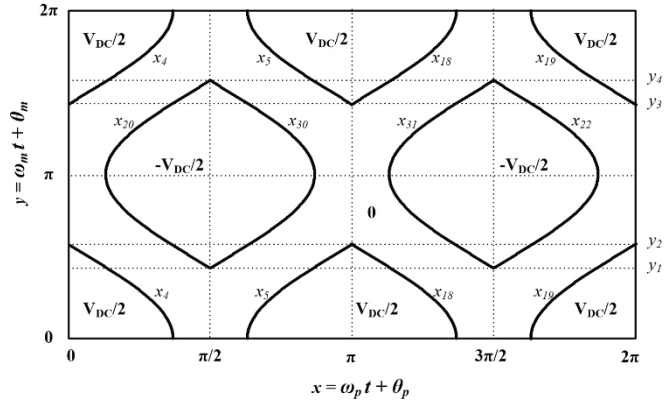

Fig. 9. Representation of the FC inverter unitary cell with the proposed modulation.

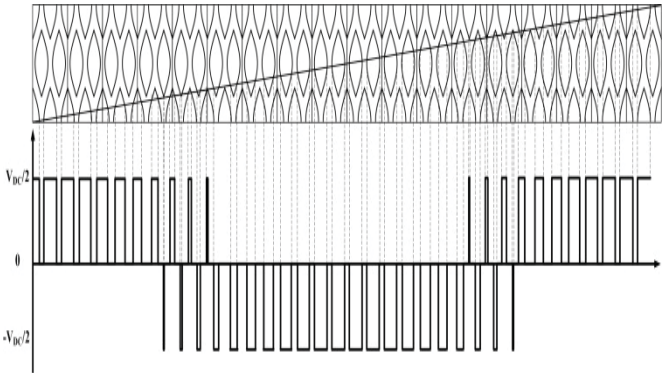

Fig. 10. Representation of output voltage with unitary cells.

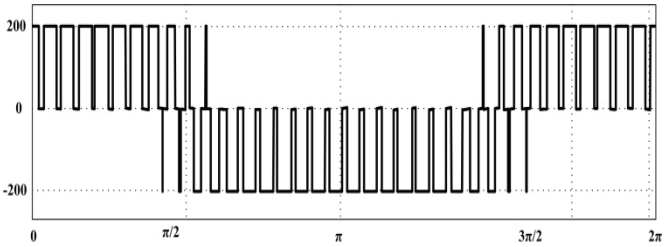

Fig. 11. Output voltage waveform (simulation).

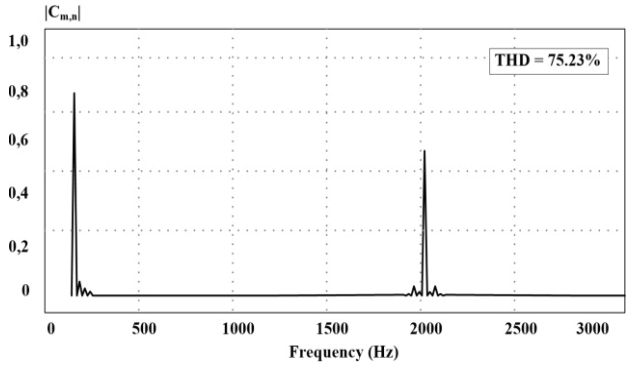

Fig. 12. Calculated harmonic components for output phase voltage.

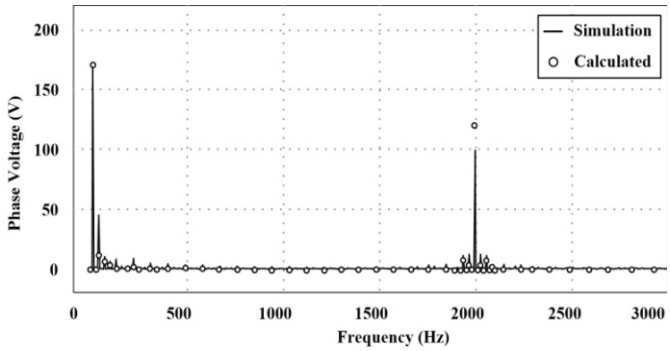

Fig. 13. Fast Fourier transform of the output phase voltage obtained through the PSIM® software compared to the theoretical waveform.

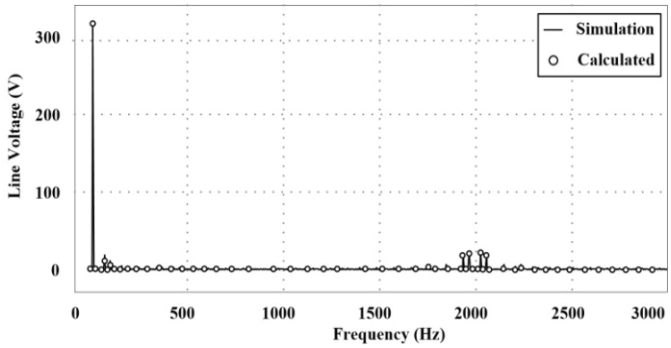

Fig. 14. Fast Fourier transform of the output line voltage obtained through the PSIM® software compared to the theoretical waveform.

TABLE VI
Summary of THD values

	Line Voltage	Phase Voltage
Calculated	39.35 %	75.23 %
Simulation	41.38 %	78.52 %
Experimental	42.09 %	79.06 %

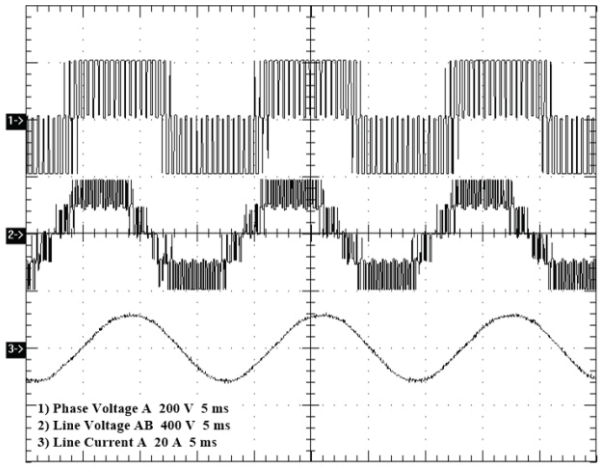

Fig. 15. Experimental results for the three-level flying capacitor multilevel inverter: 1) line voltage, 2) phase voltage and 3) line current.

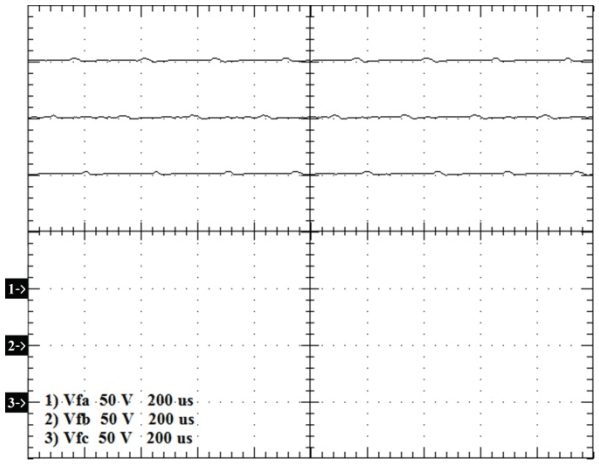

Fig. 16. Voltage across the flying capacitors.

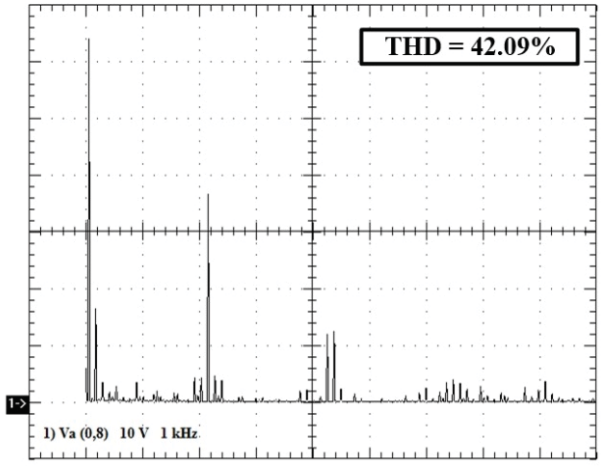

Fig. 17. Harmonic spectrum and THD measurement of line voltage.

VI. CONCLUSION

In this paper was presented a modulation technique that combines the features of two modulations HE-PWM and CSV-PWM which are considered as good contributions in reducing the total harmonic distortion when used in a flying capacitor multilevel inverter.

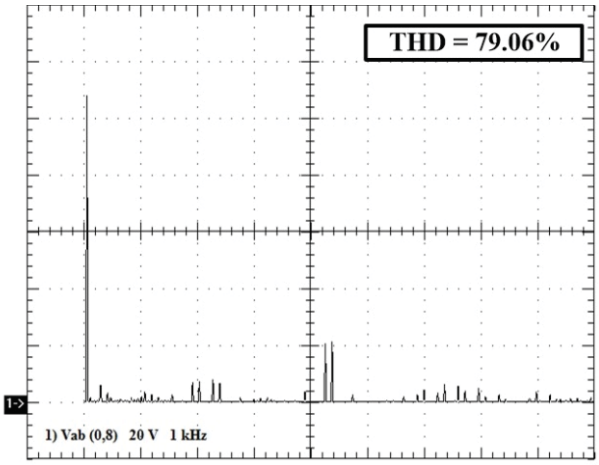

Fig. 18. Harmonic spectrum and THD measurement of phase voltage.

Analyses were submitted about the switching characteristics, the losses study and the theoretical THD calculations.

Even with the approaches, the comparison presented good similarity between the theoretical calculations, simulation and experimental results validating the presented study.

The experimental results with the flying capacitor multilevel inverter validate the proposed modulation which presented better performance than PSPWM, LSPWM, CSV-PWM modulations for all range of modulation index and up to 4.5% better than HE-PWM, showing its contribution.

However, the main drawbacks of the proposed technique are the higher complexity on its implementation and the voltage across the flying capacitors in which there is no guarantee of charging and discharging in one switching period. The authors leave as future work the detailed study on the balance of voltage in capacitors, the common mode voltage and study to expand to more voltage levels.

Also, the authors did not extend the proposed topology and suggest its implementation on CHB topology. The NPC topology cannot be used on because it allows only level-shifted carried-based modulations [19].

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