A GENERALIZED SCALAR PULSE-WIDTH MODULATION FOR NINE-SWITCH INVERTERS

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***Abstract* - The nine-switch inverter has been proposed recently and, since then, a large number of applications has been investigated, specially as a substitute to the dual-bridge (back-to-back) converter. The main advantage of the nine-switch inverter is its lesser number of switches (nine instead of twelve of the back-to-back converter), which has as a tradeoff some restrictions in the total attainable amplitude at its outputs, dependent on the phase shift between its two terminal sets. Thus, when migrating modulation techniques from the conventional three-phase inverter to the nine-switch inverter, more concerns have to be addressed. This paper deals with pulse-width modulation strategies that can be easily implemented by using the concept of generalized scalar modulation in this type of inverter. In fact, such concept leads to a systematic and straight approach to the generation of any continuous or discontinuous pulse-width modulation strategy. Aiming the reduction of switching losses, the generalized modulation is applied with a specific distribution parameter that reduces the number of switchings and the power losses of the three-phase nine-switch inverter. Experimental results confirm the validity of the proposed method.**

***Keywords* – Nine-Switch Inverter, Pulse-Width Modulation, Switching Losses.**

I. INTRODUCTION

In the last decades, the increasing reliability of power semiconductor devices allowed the development of the field of power electronics in a wide variety of applications for renewable energy sources and power quality solutions [1], [2]. This growth has boosted the development of pulse-width modulation (PWM) techniques providing a wide linear modulation range to the converters, a reduced computational burden in its implementation, fewer losses and a lower total harmonic distortion (THD) of the switching waveforms.

The modulation techniques for three-phase inverters can be classified in three types: indirect, such as space-vector modulation (SVM) [3], [4] and scalar modulation [5]; direct, such as synchronous optimal modulation [6] and selective harmonic elimination PWM [7]; and based on switching tables, where the switches' states are defined directly from control strategies, such as sliding mode control [8] and direct torque control [9]. Considering the indirect modulation techniques, in SVM, the duty cycles of the switches in one inverter leg depend on the variables of other output phases, while, in scalar modulation, the duty cycles of the switches in one inverter leg do not depend on the other output phases. Scalar modulation and SVM techniques have been largely used to command six-switch two-level voltage source inverters (VSI) or multilevel inverters [10]-[12].

The conventional SVM is based on the reference space vector, composed of a volt-second average of the three nearest switching vectors. In scalar modulation, the inverter switching states are identified by comparing a carrier signal (usually a triangle waveform) with a modulating signal. In particular, modified modulation techniques, that use non-sinusoidal modulating signals generated by adding zero axis components (homopolar components) to the three sinusoidal reference waveforms, could be applied in order to enhance a particular characteristic of the inverter, such as wider linear modulation range, efficiency or THD. Previous works [3]-[5] have shown that SVM produces switching sequences identical to those obtained with the modified scalar modulation when the appropriate zero axis components is used. Since the scalar approach uses simple equations only with scalar variables to determine the switches duty cycles, its implementation is more straightforward than the SVM, that uses lookup tables and trigonometric equations, specially if applied to nonconventional converter topologies.

In the last decades, several authors proposed to generalize the PWM techniques of various three-phase converter topologies, such as conventional six-switch two-level VSIs [5], [13]-[15], multilevel inverters [16], [17] and matrix converters [18]-[20]. Based on a detailed analysis of these past efforts, it is observed that, unfortunately, the process of generalization is not straightforward and the derived PWM techniques of each topology bear little resemblance among them. On the other hand, most of the generalizations used the scalar approach, that is easier to understand and implement, instead of the two or three dimension vectorial approach. One possible use of generalized scalar PWM is in the reduction of switching losses in high-efficiency power converters [19]. High switching losses are responsible for excessive thermal stress, reduction of the lifetime of semiconductor devices and additional cost associated with the heat sink and packaging. This issue becomes specially important in applications that require high switching frequencies such as power filters and variable frequency drives for high-speed motors.

These same issues are equally applicable to the nine-switch inverter, which is composed of two three-phase inverter units, named top and bottom units, that share not only the dc-link voltage but also three switches, i. e. the three bottom switches of the top unit and the three upper switches of the bottom unit are the same [21]. The large number of applications already

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explored for this topology in a short amount of time only proves its feasibility as a possible substitute to the back-to-back converter, formed from two six-switch two-level VSIs sharing the same dc-link [22]-[27]. The main disadvantages of the nine-switch inverter when compared with the back-to-back converter are: larger voltage stress in the switches; more complex modulation techniques, switching patterns and dead-time algorithms; and uneven power loss distribution on the switches. Notwithstanding, the main advantage of the nine-switch inverter is its reduced number of switches (three fewer than the back-to-back converter), impacting on the cost, volume and weight of the system.

The first PWM technique proposed for the nine-switch inverter was based on a sinusoidal modulation, which compares a high frequency triangular carrier with three sinusoidal reference signals, in order to create gating pulses for the switches [21]. The nine-switch inverter presents some restrictions in the total attainable amplitude at its outputs, dependent on the phase shift between its two terminal sets, which means that when migrating modulation techniques from the six-switch two-level VSI to the nine-switch inverter, more concerns have to be addressed. These concerns were investigated in [28], using the concepts of continuous and discontinuous modulations.

Moreover, a SVM has been proposed to extend the linear region of both top and bottom units of the nine-switch inverter [29]. The method increases the sum of modulation indexes up to 15% in contrast with the sinusoidal modulation. In order to reduce the number of semiconductor switchings, the authors presented a specific SVM switching pattern [29]. However, this conventional SVM can be used only in the different frequency (DF) operation mode. Recently, Dehghan *et. al* proposed a new SVM for the nine-switch inverter that supports both the common frequency (CF) and DF operation modes [30].

Although these papers explore specific modulation techniques, there is not any work that presents a generalized PWM strategy for nine-switch inverters. In this paper, a generalized PWM strategy for nine-switch inverters is proposed, in which the switching sequence is easily implemented by using the concept of scalar PWM. Moreover, the scalar approach for the generalized PWM uses the non-sinusoidal modulating signals as reference voltages of the inverter legs to determine the switches duty cycles, making the implementation much simpler than the SVM. Based on this generalization, this paper presents specific PWM techniques that reduce the number of switchings in the nine-switch inverter, aiming the reduction of its power losses. Experimental results demonstrate the validity of the generalization concept and the feasibility of the specific PWM techniques.

II. GENERALIZED SCALAR PWM TECHNIQUE FOR SIX-SWITCH TWO-LEVEL INVERTERS

The conventional three-phase six-switch two-level VSI is shown in Figure 1. Due to the capacitive nature of the dc-link and the inductive nature of the load, there are eight possible switch combinations, categorized in the SVM as active vectors

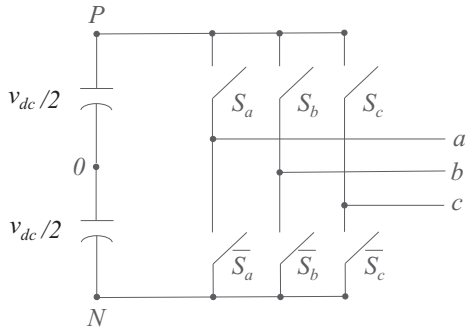

Fig. 1. Three-phase six-switch two-level VSI.

(V_1, V_2, V_3, V_4, V_5 and V_6) and zero vectors (V_0 and V_7). In the SVM, at every switching period (T_{sw}), the reference voltage vector, defined by the $abc - \alpha\beta$ transformation of the three voltage references, is synthesized by four vectors, the two adjacent active vectors and the two zero vectors, weighted by their respective duty cycles. The output voltages are completely defined by the two active vectors, whist the remaining of the switching period (the total zero time interval) is freely distributed between the two zero vectors, since both vectors produce null voltage at the inverter's outputs. Different PWM techniques are produced by simply changing the total zero time interval distribution between V_0 and V_7. This is the base for the generalized scalar PWM technique for the three-phase six-switch two-level VSI, presented in [5], [13], [14]. Since the generalization is essentially scalar, a general solution for the duty cycles of the upper switches of the six-switch two-level VSI is calculated and compared with a triangular carrier, in order to determine the *on-off* state of all six switches. The methodology to determine the general solution for the duty cycles is carried out as follows.

Consider the output voltage references defined by

$$v_{j0}^{*} = v_{j0}^{s} + v_h, \;\; j = \{a, b \text{ or } c\} \tag{1}$$

where v_h is the homopolar voltage component, known also as zero axis voltage component, and v_{j0}^{s} are the sinusoidal voltage components given by

$$\begin{cases} v_{a0}^{s} &= m\frac{v_{dc}}{\sqrt{3}}\cos(\omega t) \\ v_{b0}^{s} &= m\frac{v_{dc}}{\sqrt{3}}\cos(\omega t - \frac{2\pi}{3}) \\ v_{c0}^{s} &= m\frac{v_{dc}}{\sqrt{3}}\cos(\omega t + \frac{2\pi}{3}) \end{cases} \tag{2}$$

where m is the modulation index, v_{dc} is the dc-link voltage and ω is the desired angular frequency of the output voltages.

The general solution for the duty cycles is given by

$$D_j^G = \frac{1}{2} + \frac{v_{j0}^{*}}{v_{dc}} \tag{3}$$

where D_j^G is the generalized duty cycle of the switch S_j and the carrier used henceforth is defined as a triangular waveform limited between 0 and 1 with frequency equal to f_{sw}.

Substituting (1) in (3), it is possible to find that

$$D_j^G = \underbrace{\frac{1}{2} + \frac{v_{j0}^s}{v_{dc}}}_{D_j} + \underbrace{\frac{v_h}{v_{dc}}}_{D_h} \tag{4}$$

where D_j is the duty cycle associated with the sinusoidal voltage component and D_h is the duty cycle associated with the homopolar voltage component.

In order to complete the generalization process, it is necessary to associate the duty cycle D_h with the infinite possible distributions of the zero vectors in the total zero vector time interval. Figure 2 shows three possible switching states generated by the same sinusoidal components and different homopolar components and their influence in the zero vectors distribution. Observing Figure 2(a), it is possible to note that

$$\begin{cases} D_{V7} &= D_{min} \\ D_{V0} &= 1 - D_{max} \\ D_{null} &= D_{V0} + D_{V7} = 1 - D_{max} + D_{min} \end{cases} \tag{5}$$

where D_{V0} and D_{V7} are the duty cycles of the zero vectors V_0 and V_7, respectively, D_{min} and D_{max} are the minimum and maximum duty cycles of the upper switches of the six-switch two-level VSI using sinusoidal references, respectively, and D_{null} is the total zero vector duty cycle.

In Figure 2(b), the vector V_0 is not applied which means that D_{null} is exclusively for V_7. The opposite occurs in Figure 2(c) where the vector V_7 is not applied. However, it is important to see that regardless of which switching state is being used, the expression given by (5) is always valid.

In order to carry out the generalization, it is necessary to define a parameter μ responsible for distributing the total zero vector duty cycle between V_0 and V_7 as follows:

$$\begin{cases} D_{V0} &= \mu D_{null} \\ D_{V7} &= (1-\mu) D_{null} \end{cases} \tag{6}$$

where $0 \leq \mu \leq 1$.

The generalization is then performed by removing the existent contribution of the zero vector V_7 ($D_{V7} = D_{min}$) from the duty cycles of the sinusoidal PWM, D_j, and adding the new contribution of the zero vector V_7 as a function of the parameter μ ($D_{V7} = (1-\mu)D_{null} = (1-\mu)(1 - D_{max} + D_{min})$), leading to

$$D_j^G = D_j \underbrace{-D_{min}}_{\text{existent } D_{V7}} \underbrace{+(1-\mu)(1 - D_{max} + D_{min})}_{\text{new } D_{V7}}. \tag{7}$$

Rearranging (7), it is possible to determine the duty cycle of the generalized scalar PWM [5], [13], [14]:

$$D_j^G = D_j \underbrace{-\mu D_{min} + (1-\mu)(1 - D_{max})}_{D_h}. \tag{8}$$

When $0 < \mu < 1$, the generalized scalar PWM is known as continuous modulation. A particular case occurs when $\mu = 0.5$, leading to the symmetrical SVM. Also, the parameter μ can assume extreme constant values, i. e., $\mu = 0$, $\mu = 1$ or even change from 0 to 1 or from 1 to 0 at any time. These cases are known as discontinuous modulation. In Figure 3, three normalized non-sinusoidal voltage references (v_{a0}^*) with their associated sinusoidal (v_{a0}^s) and homopolar voltage (v_h) components are shown, in which two of them use constant values of μ and the other uses a pulsed pattern for μ.

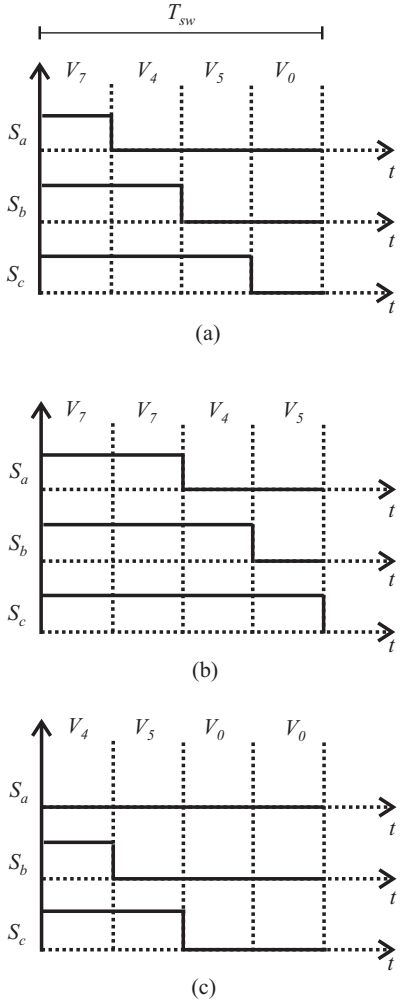

Fig. 2. Possible switching states of the three-phase six-switch two-level VSI: (a) $t_{V0} = t_{V7} = t_{null}/2$; (b) $t_{V7} = t_{null}$; (c) $t_{V0} = t_{null}$.

When comparing (4) and (8), it is possible to note that the duty cycle of the homopolar voltage component depends on the distribution parameter μ that defines the time intervals for the zero voltage vectors V_0 and V_7. Thus, this association between the homopolar voltage and the distribution parameter μ is the prove of the generalization process. The generalized scalar PWM yields non-sinusoidal reference voltages, while the sinusoidal PWM yields sinusoidal ones. Although the load phase voltages remain sinusoidal for both cases, the maximum output phase voltage of the sinusoidal PWM is equal to $v_{dc}/2$ ($m \leq \sqrt{3}/2$), while in the generalized scalar PWM is equal to $v_{dc}/\sqrt{3}$ ($m \leq 1$), due to the addition of the homopolar component. It is important to mention that, independently of

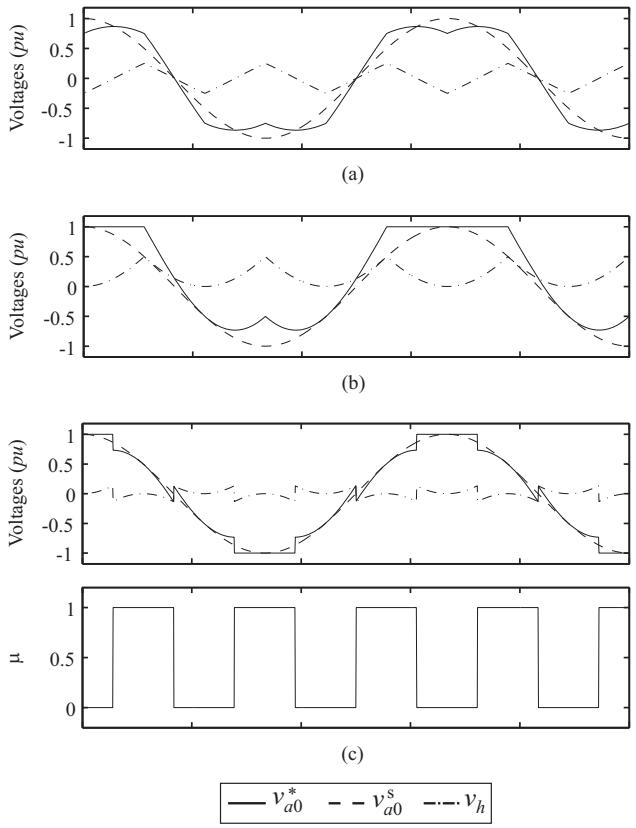

Fig. 3. Three normalized non-sinusoidal voltage references (v^*_{a0}) with their associated sinusoidal (v^s_{a0}) and homopolar voltage (v_h) components for: (a) $\mu = 0.5$ (constant); (b) $\mu = 0$ (constant); and (c) pulsed pattern for μ.

the choice of μ, the maximum output phase voltage is always equal to $v_{dc}/\sqrt{3}$, i.e., the use of the dc-link voltage in the linear region is maximum for all values of μ.

The algorithm for the generalization process can be described as follows: first, compute the sinusoidal PWM solution for the duty cycles D_j in (4), using the reference voltages in (2); second, determine the minimum and maximum duty cycles among them; third, choose μ; fourth, calculate the general solution for the duty cycles in (8).

III. GENERALIZED SCALAR PWM TECHNIQUE FOR NINE-SWITCH INVERTERS

In the nine-switch inverter, shown in Figure 4, each leg is composed of three switches and two available output terminals. This approach results in a dual inverter with two power units, named top and bottom inverter units, with two sets of three-phase output terminals (abc and rst). The middle switch in each leg is shared by both inverter units.

It is important to mention that, although the nine-switch inverter can operate in both CF and DF modes, a much wider range of application is found when operating in the DF mode, i.e. with both inverter units operating independently. For this reason, the generalization process for the nine-switch inverter is carried out considering it always in the DF mode.

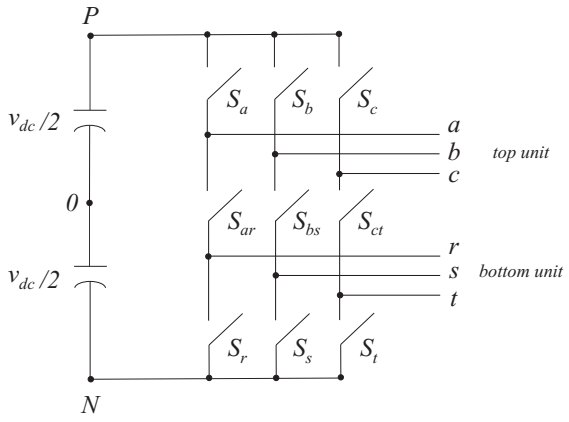

Fig. 4. Nine-switch inverter.

A. Topology Constraints and Scalar PWM Approach

The reduction of the number of devices in the nine-switch inverter topology imposes certain switching constraints that should be considered in the PWM method. As can be seen in Figure 4, there are eight possible switching states for each leg of the nine-switch inverter, but there are only three valid switching states, i.e. one switch is always open and the other two are closed. Depending on the switching state, two different voltage levels can be imposed at each inverter output terminal. The valid switching states and the output voltages for the inverter leg *ar* are described in Table I.

Considering Table I, it is possible to find that switch S_j controls the output voltage v_{j0} as follows:

$$v_{j0} = (2S_j - 1)\frac{v_{dc}}{2} \tag{9}$$

where $S_j = 0$ and $S_j = 1$ represent switch open and closed, respectively, and $j = \{a, b \text{ or } c\}$.

The duty cycle D_j of switch S_j in the top inverter unit can be determined taking the average value of (9) in T_{sw}:

$$D_j = \frac{1}{2} + \frac{v^*_{j0}}{v_{dc}} \tag{10}$$

where v^*_{j0} is the reference voltage imposed at the output terminal j, which is equal to $\overline{v}_{j0}$ (average value in the T_{sw}).

Similarly, observing Table I, it is possible to note that switch S_k, where $k = \{r, s \text{ or } t\}$, controls the voltage v_{k0} through the following expression

$$v_{k0} = (1 - 2S_k)\frac{v_{dc}}{2} \tag{11}$$

where $S_k = 0$ and $S_k = 1$ represent switch open and closed, respectively.

TABLE I
Switching States for Inverter Leg *ar*

Switching State	S_a	S_{ar}	S_r	v_{a0}	v_{r0}
1	*On*	*On*	*Off*	$+v_{dc}/2$	$+v_{dc}/2$
2	*On*	*Off*	*On*	$+v_{dc}/2$	$-v_{dc}/2$
3	*Off*	*On*	*On*	$-v_{dc}/2$	$-v_{dc}/2$

Taking the average value of (11) in T_{sw}, it is possible to find the duty cycle D_k of switch S_k:

$$D_k = \frac{1}{2} - \frac{v^*_{k0}}{v_{dc}} \tag{12}$$

where v^*_{k0} is the reference voltage imposed at the output terminal *k*, which is equal to $\overline{v}_{k0}$ (average value).

It can be noted that switches S_j and S_k in the same leg have opposite behavior: for example, while v_{a0} is positive when $S_a = 1$, v_{r0} is positive when $S_r = 0$, and vice-versa. For this reason, the duty cycle D_k presents an opposite sign when compared with D_j. Moreover, in Table I, it is possible to find that $v_{j0} \geq v_{k0}$ for all possible switching states. Considering the average value in T_{sw}, it is found that $\overline{v}_{j0} \geq \overline{v}_{k0}$ and, consequently, the following inequalities should always be respected, for j and k in the same inverter leg:

$$v^*_{j0} \geq v^*_{k0} \Longleftrightarrow D_j \geq 1 - D_k = \overline{D}_k. \tag{13}$$

Based on (13), it is impossible for the nine-switch inverter to synthesize two pure sinusoidal voltages at the outputs j and k, since at some point the sinusoidal voltage at terminal k would become greater than the one at terminal j. Nevertheless, this restriction can be overcome by scaling and shifting the duty cycle expressions of both inverter units, such that $D_j \geq \overline{D}_k$.

B. Generalized Scalar PWM

Based on the nine-switch inverter constraints, the duty cycle spanning range of both inverter units should always be disjunct in the DF operation mode. As a consequence, there is a natural reduction of the modulation index range and a dc-link voltage sharing for both units.

A general approach is achieved when the duty cycle valid range ($0 \leq D \leq 1$) is unequally divided for the top and bottom inverter units as shown in Figure 5, corresponding to an unequal dc-link sharing between units. It is clear that the sum of the modulation index limits of both inverter units should be always equal to unity, i. e. $M_{bot} + M_{top} = 1$. In order to obtain the generalized duty cycles expressions for the top and bottom inverter units, it is necessary to scale and shift the duty cycles D^G_j of the conventional six-switch two-level VSI, given by (8).

For the top unit, the duty cycles are scaled and shifted as

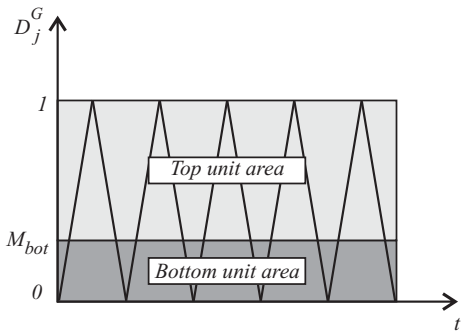

Fig. 5. Top and bottom inverter unit areas for unequal dc-link sharing and the triangular carrier.

follows

$$D^G_{j_{top}} = M_{top} D^G_j + \underbrace{(1 - M_{top})}_{M_{bot}} \tag{14}$$

where $j = \{a, b \text{ or } c\}$ and $M_{bot} = 1 - M_{top}$.

Replacing (8) in (14) and considering $\mu = \mu_{top}$, $v^s_{j0} \cdot M_{top} = v^s_{j0_{top}}$ and $m \cdot M_{top} = m_{top}$, it yields

$$\begin{aligned} D^G_{j_{top}} &= D_{j_{top}} - \mu_{top} D_{min_{top}} + \\ &+ (1 - \mu_{top})(1 - D_{max_{top}}) + (1 - M_{top})\mu_{top} \end{aligned} \tag{15}$$

where $\mu_{top} \in [0, 1]$,

$$D_{j_{top}} = 1 - \frac{M_{top}}{2} + \frac{v^s_{j0_{top}}}{v_{dc}} \tag{16}$$

$$D_{min_{top}} = 1 - \frac{M_{top}}{2} + \frac{v_{min_{top}}}{v_{dc}} \tag{17}$$

$$D_{max_{top}} = 1 - \frac{M_{top}}{2} + \frac{v_{max_{top}}}{v_{dc}} \tag{18}$$

with $v_{min_{top}}$ and $v_{max_{top}}$ being defined by

$$v_{min_{top}} = \min\left(v^s_{a0_{top}}, v^s_{b0_{top}}, v^s_{c0_{top}}\right) \tag{19}$$

$$v_{max_{top}} = \max\left(v^s_{a0_{top}}, v^s_{b0_{top}}, v^s_{c0_{top}}\right). \tag{20}$$

Also, the top inverter unit generalization is valid for the sinusoidal reference voltage set defined by

$$\begin{cases} v^s_{a0_{top}} &= m_{top} \frac{v_{dc}}{\sqrt{3}} \cos\left(\omega_{top} t\right) \\ v^s_{b0_{top}} &= m_{top} \frac{v_{dc}}{\sqrt{3}} \cos\left(\omega_{top} t - \frac{2\pi}{3}\right) \\ v^s_{c0_{top}} &= m_{top} \frac{v_{dc}}{\sqrt{3}} \cos\left(\omega_{top} t + \frac{2\pi}{3}\right) \end{cases} \tag{21}$$

where m_{top} is the modulation index and ω_{top} is the output voltage angular frequency for the top inverter unit. It is important to mention that the modulation index of the top unit is limited at $m_{top} \leq M_{top}$, where $M_{bot} + M_{top} = 1$.

Similarly, the complementary duty cycle expressions for the bottom inverter unit are obtained by scaling the complementary duty cycles of the conventional six-switch two-level VSI, given by (8), as follows:

$$\overline{D}^G_{k_{bot}} = M_{bot} \overline{D}^G_k \tag{22}$$

where $\overline{D}^G_k = 1 - D^G_k$ are the complementary duty cycles of the conventional six-switch two-level VSI using index k instead of j, with $k = \{r, s \text{ or } t\}$ and $M_{bot} = 1 - M_{top}$.

Replacing (8) in (22) and considering $\mu = \mu_{bot}$, $v^s_{k0} \cdot M_{bot} = v^s_{k0_{bot}}$ and $m \cdot M_{bot} = m_{bot}$, yields

$$\begin{aligned} \overline{D}^G_{k_{bot}} &= \overline{D}_{k_{bot}} - \mu_{bot} \overline{D}_{min_{bot}} + \\ &+ (1 - \mu_{bot})(1 - \overline{D}_{max_{bot}}) - (1 - \mu_{bot})(1 - M_{bot}) \end{aligned} \tag{23}$$

where $\mu_{bot} \in [0, 1]$,

$$\overline{D}_{k_{bot}} = \frac{M_{bot}}{2} + \frac{v^s_{k0_{bot}}}{v_{dc}} \tag{24}$$

$$\overline{D}_{min_{bot}} = \frac{M_{bot}}{2} + \frac{v_{min_{bot}}}{v_{dc}} \tag{25}$$

$$\overline{D}_{max_{bot}} = \frac{M_{bot}}{2} + \frac{v_{max_{bot}}}{v_{dc}} \tag{26}$$

with $v_{min_{bot}}$ and $v_{max_{bot}}$ being defined by

$$v_{min_{bot}} = \min\left(v^s_{r0_{bot}}, v^s_{s0_{bot}}, v^s_{t0_{bot}}\right) \tag{27}$$

$$v_{max_{bot}} = \max\left(v^s_{r0_{bot}}, v^s_{s0_{bot}}, v^s_{t0_{bot}}\right). \tag{28}$$

Also, the bottom inverter unit generalization in (23) is valid for the sinusoidal reference voltage set defined by

$$\begin{cases} v^s_{r0_{bot}} &= m_{bot}\frac{v_{dc}}{\sqrt{3}}\cos\left(\omega_{bot}t\right) \\ v^s_{s0_{bot}} &= m_{bot}\frac{v_{dc}}{\sqrt{3}}\cos\left(\omega_{bot}t - \frac{2\pi}{3}\right) \\ v^s_{t0_{bot}} &= m_{bot}\frac{v_{dc}}{\sqrt{3}}\cos\left(\omega_{bot}t + \frac{2\pi}{3}\right) \end{cases} \tag{29}$$

where m_{bot} is the modulation index and ω_{bot} is the output voltage angular frequency for the bottom inverter unit. It is important to mention that the modulation index of the bottom unit is limited at $m_{bot} \leq M_{bot}$, where $M_{bot} + M_{top} = 1$.

This generalization is particularly useful when both inverter units need to synthesize output voltages with different voltage limits and angular frequencies, such as in dual active power filters, dual hybrid power filters and interfacing a low-frequency grid with a high-frequency load.

The algorithm for the generalization process can be described as follows:

1. choose M_{top} and M_{bot}, respecting $M_{bot} + M_{top} = 1$;
2. compute the sinusoidal PWM solutions for the duty cycles in (16) and (24), using the reference voltages in (21) and (29);
3. determine the minimum and maximum duty cycles in (17)-(20) and (25)-(28);
4. choose μ_{top} and μ_{bot};
5. calculate the general solution for the duty cycles in (15) and (23).

A special case, in which the top and bottom inverter units share equally the dc-link voltage (Figure 6), can be derived when $M_{bot} = M_{top} = 0.5$. In this case, the relations (14) and (22) fall respectively to

$$D^G_{j_{top}} = \frac{D^G_j}{2} + \frac{1}{2} \tag{30}$$

$$\overline{D}^G_{k_{bot}} = \frac{\overline{D}^G_k}{2}. \tag{31}$$

The generalization for the equal dc-link sharing is particularly useful when both inverter units need to synthesize output voltages with the same voltage limit but not necessarily the same angular frequency, such as when driving two similar motors at different speeds.

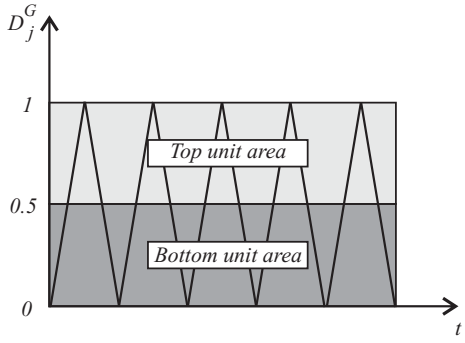

Fig. 6. Top and bottom inverter units areas for equal dc-link sharing and the triangular carrier.

IV. SWITCHING LOSSES REDUCTION MODULATION TECHNIQUES FOR NINE-SWITCH INVERTERS

Based on the generalization method presented in the previous section, it is possible to apply such generalized scalar PWM with a specific pattern for μ_{top} and μ_{bot}, aiming the reduction of the power losses in both top and bottom units of the nine-switch inverter.

A. Modulation Technique Based on the Pulsed Pattern for μ

Chung and Sul [31] studied the possibility of changing the moment of clamping an input phase to achieve lower switching losses in the controlled rectifier. Later, this technique was extended to three-phase six-switch two-level VSI [32]. In this technique, segments of clamped output voltages are synchronized with the positive and negative peaks of the output currents of the six-switch two-level VSI. In order to guarantee the minimization of the switching losses in all range of the output load angle (Φ_{V-I}), the clamping segments defined in [31] were adapted as a function of the distribution parameter μ of the generalized scalar PWM, so that the clamping segments are always in the vicinity of the positive and negative peaks of the output currents.

In the generalized PWM, if $\mu = 1$ is chosen, the output phase with the lowest voltage is clamped in negative point of the dc-link (Figure 1), else if $\mu = 0$ is chosen, the output phase with the highest voltage is clamped in positive point of the dc-link. Thus, with the appropriate choice of μ, always the highest absolute output voltage of the six-switch two-level VSI is clamped as follow: if the highest absolute output voltage reference is positive, choose $\mu = 0$, and if the highest absolute output voltage reference is negative, choose $\mu = 1$. For a balanced three-phase output voltage set, a pulsed pattern for μ, defined by alternating ones and zeros that change at every 60° of the output voltage angle, is obtained.

If the previous logic is used, the clamped voltages segments are synchronized with the positive and negative peaks of the output phase voltages. However, it is desired to synchronize these clamped voltages segments with the peaks of the load currents, in order to decrease the switching losses. One simple way to solve this issue is to choose the value of μ from a set of three-phase logical signals shifted of an angle Φ_μ from the set of three-phase output voltage references (Figure 7) [32]. This guarantees that the new pulsed pattern for μ lags the original

pattern by the angle Φ_μ.

The same PWM technique presented for the six-switch two-level VSI can be applied for both inverter units of the nine-switch inverter, generating pulsed patterns for μ_{top} and μ_{bot}, that guarantee that the clamped voltages segments of both units are synchronized with the peaks of their output currents. The major difference between the nine-switch inverter and the six-switch two-level VSI for this technique is the fact that the top inverter unit cannot clamp the output phase with the lowest voltage in negative point of the dc-link, since the bottom switch of the top unit is shared with the bottom unit, as well as, the bottom inverter unit cannot clamp the output phase with the highest voltage in positive point of the dc-link, since the top switch of the bottom unit is shared with the top unit. Thus, this technique can only clamp the voltage segments half of the times for both inverter units.

Notwithstanding, considering the angle between the output voltages and currents of the top and bottom unit as Φ_{V-I}^{top} and Φ_{V-I}^{bot}, it is possible to find the respective shifting angles Φ_μ^{top} and Φ_μ^{bot} by means of the function defined in Figure 7. Therefore, the pulsed patterns for μ_{top} and μ_{bot} can be defined.

B. 120° Discontinuous Modulation Technique

Since the modulation technique based on the pulsed pattern for μ is only able to clamp half of the output voltage segments for both top and bottom units of the nine-switch inverter, the clamping segments for all output phases of each inverter unit sum $180°$ per fundamental period.

Other possible modulation technique is the $120°$ discontinuous modulation, in which the output voltages of inverter unit are clamped all the time in the positive or the negative point of the dc-link. Since the output voltages of the top inverter unit can only clamp in the positive point of the dc-link, $\mu_{top} = 0$ is chosen. Similarly, since the output voltages of the bottom inverter unit can only clamp in the negative point of the dc-link, $\mu_{bot} = 1$ is chosen. With such technique, the clamping segments for all output phases of each inverter unit sum $360°$ per fundamental period, twice of the modulation technique based on the pulsed pattern for μ.

It is important to mention that, when using modulation techniques to reduce the switching losses, the inverter presents a smaller number of commutations, leading to a slightly larger value of THD for the output currents when compared with modulation techniques that present a higher number of commutations.

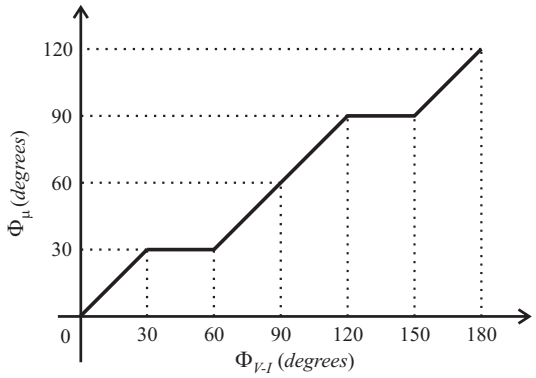

Fig. 7. Behavior of the lag Φ_μ as a function of the load displacement angle Φ_{V-I}, used to determine the values of μ.

V. COMPARISON AMONG TECHNIQUES

The nine-switch inverter performance is compared for three particular modulation techniques: symmetrical SVM (equivalent to $\mu_{top} = \mu_{bot} = 0.5$), $120°$ discontinuous PWM (equivalent to $\mu_{top} = 0$ and $\mu_{bot} = 1$) and modulation based on pulsed pattern for μ (with the objective of synchronizing the clamped voltage segments with the corresponding current peaks).

A. Description of the Performance Metrics

The nine-switch inverter performance metrics adopted for comparison are: number of switchings in each switching period, THD of the output currents and efficiency. For the number of switchings, it is considered the double-sided switching pattern for all modulation techniques, i.e., the first and second halves of the switching period are mirrored. For the THD, it is considered the maximum THD among all output currents, which is calculated up to harmonic order 51.

The conduction and switching losses of the IGBTs and diodes are estimated by simulation using a methodology based on data provided by devices data sheets [33]. In general, the data sheets provide experimental curves of the forward voltage during conduction for the IGBT and diode, the turn on and turn off losses for the IGBT and the reverse recovery loss for the diode. Those curves depend on several device parameters, such as conducting current, blocking voltage, temperature, gate resistance and gate-emitter voltage. In order to make a fair comparison among modulation techniques, the temperature, gate resistance and gate-emitter voltage are considered constant. Therefore, only the effects of the conducting current and blocking voltage on the device loss are considered.

The conduction energy loss for an IGBT or a diode can be expressed as

$$E_{cond} = \int_0^{t_{cond}} v_{cond}(i) i(t) dt \tag{32}$$

where E_{cond} is the conduction energy loss, v_{cond} is the device conduction voltage, i is the conduction current and t_{cond} is the conduction time. The conduction voltage dependence on the conduction current is generally nonlinear. Although a linear approximation is often used, a second order polynomial equation is a better characterization of such dependence. Thus, the polynomial equation is expressed as

$$v_{cond} = A_{cond} i^2 + B_{cond} i + C_{cond} \tag{33}$$

where A_{cond}, B_{cond} and C_{cond} are the coefficients obtained from the curve fitting of the data provided by the device data sheet.

Although the switching and the reverse recovery energy losses are characterized similarly to the conduction energy losses, two variables must be considered: the blocking voltage prior turn on or after turn off and the conduction current

after turn on or prior turn off. The turn on, turn off and the reverse recovery losses dependence on the conduction current is generally nonlinear, being represented by a second order polynomial equation. On the other hand, for some manufacturers, such as Semikron, the dependence on the blocking voltage is approximately linear, being represented by a voltage ratio. Thus, the turn on, turn off and the reverse recovery losses are expressed as

$$E_{sw} = (A_{sw} i^2 + B_{sw} i + C_{sw}) \frac{v_{block}}{V_{block}^{ref}} \tag{34}$$

where A_{sw}, B_{sw} and C_{sw} are the coefficients obtained from the curve fitting of the data provided by the device data sheet, V_{block}^{ref} is the reference blocking voltage used by the manufacturer to obtain the data sheet curves and v_{block} and i are the instantaneous blocking voltage and conduction current measured every time that a switching occurs, respectively. Although the switching losses are represented by the same equation, different coefficients should be considered for the turn on, turn off and reverse recovery losses.

After estimating the conduction and switching energy losses for each switch (IGBT + diode), the total energy loss is calculated and divided by the simulation time, in order to find the total power loss (P_{loss}). Equivalently, the total inverter output power (P_{out}) is calculated as the sum of the output power of each inverter unit. Thus, the efficiency (η) is expressed as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}. \tag{35}$$

B. Comparison Results

In order to evaluate the nine-switch inverter efficiency for each modulation technique, a 50 A / 1200 V Semikron module (formed by one IGBT and one diode in anti-parallel) is chosen with temperature fixed in 125 °C, gate resistance equal to 27 Ω, gate-emitter voltage equal to 15 V and $V_{block}^{ref} = 600$ V. The other system parameters are: output frequencies equal to 60 Hz, dc-link voltage equal to 600 V and equal dc-link sharing ($M_{top} = M_{bot} = m_{top} = m_{bot} = 0.5$).

As for the number of switchings, the SVM does not present any output voltage clamped segments during the fundamental period. Therefore, it always presents 24 switchings (eight for each output phase). Using $\mu_{top} = 0$, each inverter top switch (S_a, S_b and S_c) remains in on state during 120°. For example, while S_a is on, there are four switchings in the leg ar (two for S_r and two for S_{ar}) and eight switchings in the other legs, presenting a total of 20 switchings for both units. Using $\mu_{bot} = 1$, each inverter bottom switch (S_r, S_s and S_t) remains in on state during 120°, presenting also a total of 20 switchings for both units. Therefore, the modulation based on the pulsed pattern for μ (changing at every 60°) presents a total of 20 switchings, although there is no switchings around the positive peaks of the output currents for the top unit and around the negative peaks of the output currents for the bottom unit, resulting in reduced switching losses. A good alternative is the 120° discontinuous modulation ($\mu_{top} = 0$ and $\mu_{bot} = 1$), that presents a total of 16 switchings (eight switchings for the leg that is not clamped and four switchings for the two legs that are clamped). Table II summarizes the number of switchings for each modulation technique. Based on this analysis, it is expected for the 120° discontinuous modulation to present the highest efficiency and for the SVM to present the lowest.

The efficiency and THD performance metrics are evaluated as function of the inverter output power (P_{out}), the load displacement factor (LDF) and the inverter switching frequency (f_{sw}) and the results are presented in Figures 8, 9 and 10, respectively. It is possible to see that the 120° discontinuous modulation presents the best efficiency performance for all studied cases (Figures 8(a), 9(a) and 10(a)), followed by the modulation based on the pulsed pattern for μ and the SVM.

In terms of current THD (Figures 8(b), 9(b) and 10(b)), the pulsed μ modulation presents the best performance, followed by the SVM and the discontinuous modulation. It is important to note that, although the symmetrical SVM is known to have the best voltage THD performance for the six-switch two-level VSI, the THD results presented in this paper are for the output

TABLE II
Number of switchings for the PWM techniques

PWM Technique	Number of Switchings
SVM ($\mu_{top} = \mu_{bot} = 0.5$)	24
Pulsed pattern for μ_{top} and μ_{bot}	20
120° discontinuous ($\mu_{top} = 0$ and $\mu_{bot} = 1$)	16

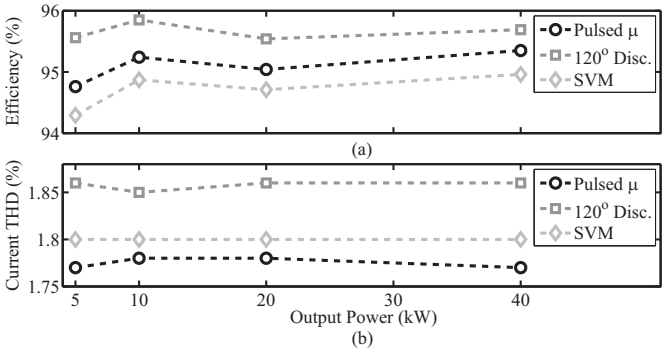

Fig. 8. Comparison results of (a) efficiency and (b) THD of the output currents as function of the inverter output power (LDF = 0.95 and $f_{sw} = 10$ kHz).

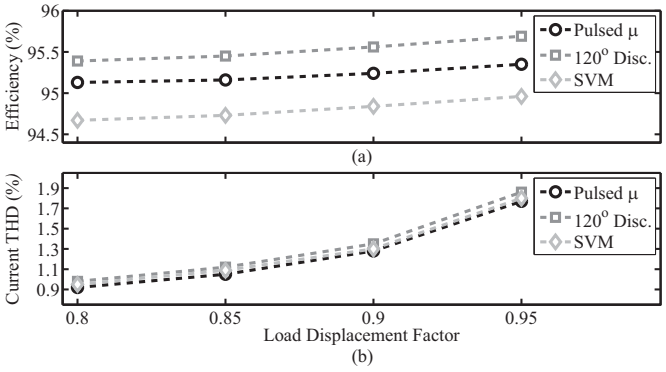

Fig. 9. Comparison results of (a) efficiency and (b) THD of the output currents as function of the load displacement factor ($P_{out} = 40$ kW and $f_{sw} = 10$ kHz).

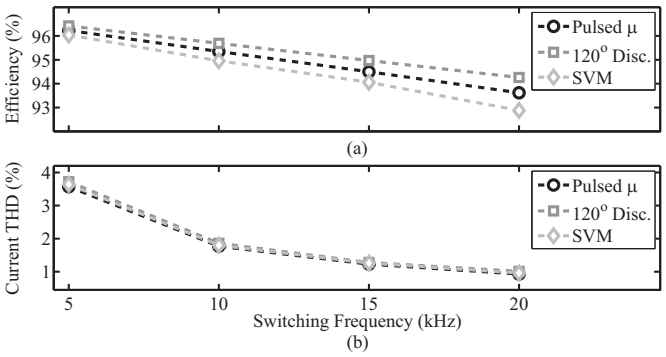

Fig. 10. Comparison results of (a) efficiency and (b) THD of the output currents as function of the switching frequency ($P_{out} = 40$ kW and LDF = 0.95).

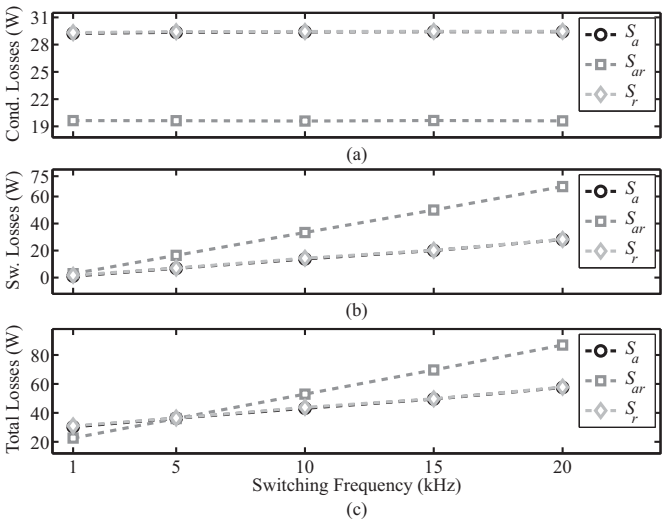

Fig. 11. Results of the conduction, switching and total losses of the inverter leg ar as function of the switching frequency ($P_{out} = 40$ kW and LDF = 0.95).

currents of the nine-switch inverter, considering harmonics up to order 51.

In order to evaluate the power loss distribution among the switches of the nine-switch inverter, the conduction, switching and total losses of all three switches of the inverter leg ar are shown in Figure 11, as function of the switching frequency. It is possible to see that the conduction losses of the middle switch (S_{ar}) are lower than the top and bottom switches (S_a and S_r). Observing Table I, if the switching state 1 is active, the top switch will handle both top and bottom unit currents ($i_a + i_r$), while the middle switch will handle only the bottom unit current (i_r). Similarly, if the switching state 3 is active, the bottom switch will handle both top and bottom unit currents ($i_a + i_r$), while the middle switch will handle only the top unit current (i_a). On the other hand, the switching losses of the middle switch (S_{ar}) are higher than the top and bottom switches (S_a and S_r). The explanation is straightforward: while the top and bottom switches present only two switchings per T_{sw}, the middle switch presents four switchings. Based on this analysis, the power loss distribution among the switches will depend mainly on the switching frequency, as can be seen in Figure 11(c). For low switching frequencies, the power loss will be concentrated in the top and bottom switches and, for high switching frequencies, it is the contrary.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The nine-switch inverter, modulated by the generalized scalar PWM, is tested both in MATLAB/Simulink and in a experimental test bench. The hardware platform used to control the nine-switch inverter is a dSPACE development modular system based on a DS1005 processor board and a DS5101 board for PWM generation. All boards are hosted in a dSpace PX10 expansion box that uses the DS817 board for bidirectional communication with a computer through optical fibers. The nine-switch inverter prototype has a nominal power of 40 kW and uses 50 A / 1200 V Semikron switches. The system parameters are given in Table III.

It is important to mention that all results are shown for the bottom unit since the results for the top unit are very similar. The simulation results for the output current and voltage of phase *r* are shown in Figure 12, considering the pulsed pattern for μ_{top} and μ_{bot} (Figure 12(a)) and the 120° discontinuous modulation with $\mu_{top} = 0$ and $\mu_{bot} = 1$ (Figure 12(b)). It is possible to note that, while the technique with the pulsed pattern for μ only presents 60° clamped voltage segments near the peak of the output current, the 120° discontinuous modulation 120° clamped voltage segments that include also the peak of the output current, since the load displacement angles are particularly small.

TABLE III
Simulation and Experimental Parameters

Parameter	Symbol	Value
Dc-link voltage	v_{dc}	60 V
Switching frequency	f_{sw}	10 kHz
Top load resistance	R_{top}	16.1 Ω
Bottom load resistance	R_{bot}	16.1 Ω
Top load inductance	L_{top}	9.1 mH
Bottom load inductance	L_{bot}	7 mH
Top load displacement angle	Φ_{V-I}^{top}	12°
Bottom load displacement angle	Φ_{V-I}^{bot}	9.3°
Top unit modulation index limit	M_{top}	0.5
Bottom unit modulation index limit	M_{bot}	0.5
Top unit modulation index	m_{top}	0.5
Bottom unit modulation index	m_{bot}	0.5
Top unit output frequency	ω_{top}	377 rad/s
Bottom unit output frequency	ω_{bot}	377 rad/s

Based on these results, it is expected that both techniques present low switching losses, being the 120° discontinuous modulation the lowest. For this reason, only the experimental results of the discontinuous modulation with $\mu_{top} = 0$ and $\mu_{bot} = 1$ are shown in Figure 13. It can be seen in Figure 13(a) that the bottom unit output currents are sinusoidal and perfectly balanced (the rms value of all three currents span from 598 mA to 600 mA). Figure 13(b) shows the output current and voltage of phase *r*, equivalent to Figure 12(b). It is possible to see the similarity in both results, proving the feasibility of the generalized technique.

The results presented in Figures 12 and 13 consider equal dc-link sharing. In order to prove the generalization for unequal dc-link sharing, an experimental result with a

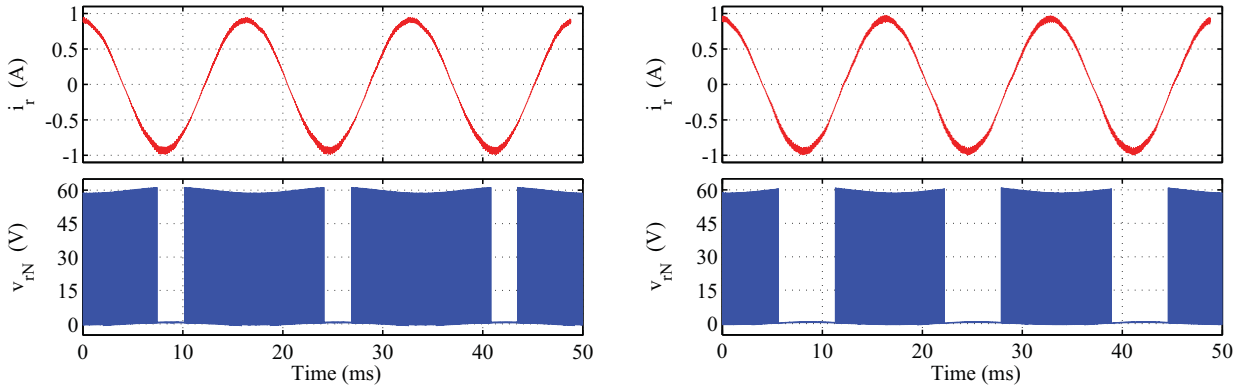

Fig. 12. Simulation results: current (i_r) and voltage (v_{rN}) with (a) $\mu_{top} = \mu_{bot} =$ pulsed and (b) $\mu_{top} = 0$, $\mu_{bot} = 1$.

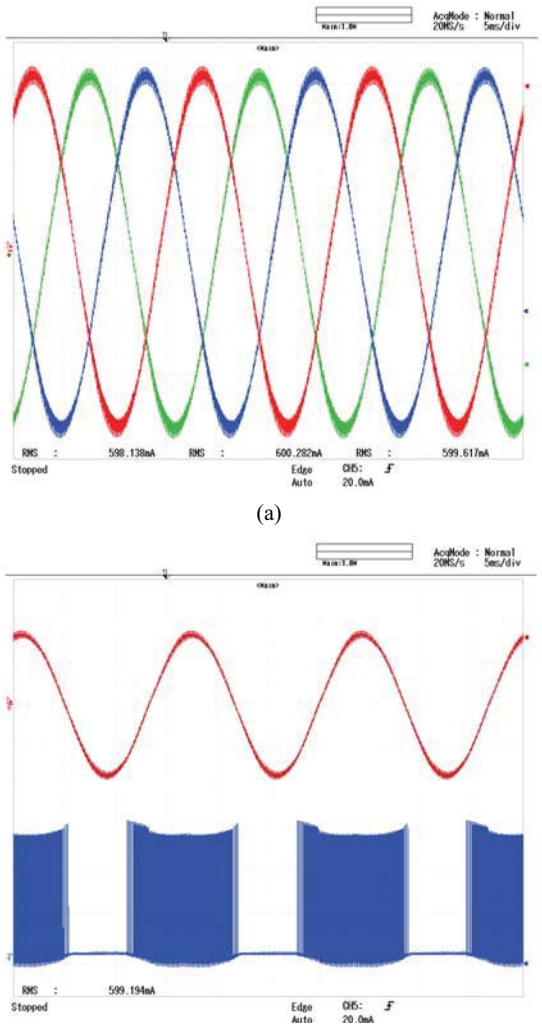

Fig. 13. Experimental results: (a) currents (i_r, i_s and i_t); (b) current (i_r) and voltage (v_{rN}) for $\mu_{top} = 0$, $\mu_{bot} = 1$. Scales: current (500 mA/div), voltage (20 V/div), time (5 ms/div).

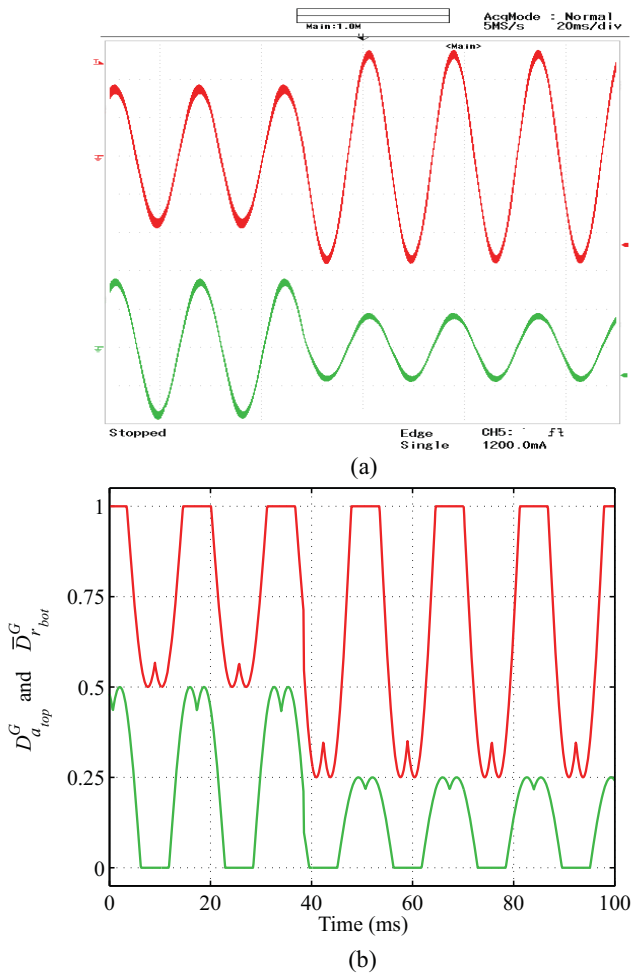

Fig. 14. Experimental results for a step change in the modulation index: $M_{top} = m_{top}$ from 0.50 to 0.75 ($\mu_{top} = 0$) and $M_{bot} = m_{bot}$ from 0.50 to 0.25 ($\mu_{bot} = 1$). (a) output currents (i_a - red; i_r - green) and (b) duty cycles of the switches of leg ar ($D^G_{a_{top}}$ - red; $\overline{D}^G_{r_{bot}}$ - green). Scales: current (500 mA/div), time (20 ms/div).

modulation index step change from 0.50 to 0.75 for $M_{top} = m_{top}$ and from 0.50 to 0.25 for $M_{bot} = m_{bot}$ is shown in Figure 14. It is possible to see that even with the step change in the duty cycles of the switches S_a and S_r, the inequality $D^G_{a_{top}} \geq \overline{D}^G_{r_{bot}}$ is respected. The step change in the output currents i_a and i_r confirm that both units work correctly, independently of the variations in the modulation index limits.

VII. CONCLUSION

This paper presents a generalized PWM strategy for the three-phase nine-switch inverter that allows choosing a PWM technique to reduce the power losses by two ways: decreasing the number of switchings in each switching period and/or clamping the output voltages of the inverter units synchronized with the peak of the corresponding currents avoid high switching losses. It has been shown that the implementation of such strategies by a generalized scalar modulation is an interesting alternative to the use of lookup tables of the space-vector modulation. Experimental results validate both the generalization and the proposed approach to reduce the power losses in nine-switch inverters.

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