A NEW CONTROL SOLUTION USING FCS-MPC FOR A BIDIRECTIONAL INTERLEAVED CONVERTER OPERATING AS A DC POWER-FLOW INTERFACE

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***Abstract* – This work proposes a control solution based on finite control set model predictive control (FCS-MPC) for interleaved converters with the features of maintaining phase currents balanced and reducing the output current ripple while presenting a voltage regulation with a high disturbance rejection capability even under constant power loads. Moreover, the proposed solution adds a penalty strategy in the cost function to prevent overcurrent. Further, this work provides a secondary contribution, consisting of a method to estimate the predictive control bandwidth based on the disturbance rejection capability. The control analysis and the simulation results carried out throughout the work confirm that the proposed strategy solves the main issues of the interleaved converter and ensures the operation for applications in power flow interfacing between dc links.**

***Keywords* – Dc Power-Flow Interface, Interleaved Converter, Model Predictive Control.**

I. INTRODUCTION

Applications in dc-systems grow each year, increasing the number of researches concerning dc converters topologies and their control solutions [1].

Among these topologies, interleaved converters, also known as multi-phase dc converters, present valuable features for applications as regulated voltage sources and power-flow interfaces between dc-links [2], [3].

These features include a lower ripple in the output current, demanding a smaller output capacitor, resulting in a lighter converter. The ripple reduction rises from the modulation strategy that produces a shifted ripple pattern in each phase, leading to a partial or total ripple cancellation, depending on the voltage ratio [4].

The controller of these converters typically falls into the main drawback of this class of converters: phase-current imbalance. The reasons for this problem include mismatches between the duty cycles of each phase, sampling issues, and impedance mismatch [4].

Some works [2], [3] intend to control this type of converter using linear control strategies; others, on the other hand, try to solve the previous issues using model predictive control [5]–[16].

This paper proposes a new MPC strategy for an N-phase bidirectional interleaved converter that solves the phase-current imbalance while regulates the converter's output voltage with a high-disturbance rejection capability and minimizes the output current ripple. Besides, this work also provides a secondary contribution: a method to estimate the closed-loop bandwidth of the proposed MPC strategy based on the disturbance rejection performance, the systems' parameters, and the control parameters.

The following sections discuss the state-of-the-art of MPC in interleaved converters (Section II), present its topology and model (Section III), introduce the novel control strategy (Section IV), analyze its design and performance (Sections V, VI and VII), and validate the solution in simulations (Section VIII and IX).

II. REVIEW ON MPC IN INTERLEAVED CONVERTERS

Model predictive control (MPC) viability has been increasing recently, due to advances in microcontroller technology, as a promising option for controlling power electronics converters and drives [17]. In particular, research on MPC applied to interleaved converters is a minority, and most of them focus only on low-power applications [5]–[10], [14], [16].

In 2008, [5] proposed a predictive control strategy based on penalties for a two-phase interleaved buck converter. The solution, however, requires the optimization problem to be solved offline for various system's parameters.

Based on penalty strategies, [6] and [7] proposed a predictive control to the unidirectional interleaved boost converter. [6] discuss only scenarios with resistive loads, and the results show a typical problem of the interleaved converter: phase current imbalance when the systems operate under light load. The penalty strategy of [7] behaves similarly to a hysteresis control, but it presents problems such as phase-currents oscillations.

In 2012, [8] compared the performance of different types of MPC in a battery system with an interleaved converter performing output voltage regulation. However, it does not address the tasks of phase currents balancing and output current ripple reduction.

In 2013, [9] used an E-MPC (Explicit Model Predictive Control) in an N-phase generic interleaved converter, and the solution reports better results regarding the previous issues of phase currents oscillations and imbalance. Nevertheless, its implementation is quite complex, as the cost function uses a matrix of penalties and makes online control impossible, according to the authors.

In 2014, [10] proposed an FCS-MPC to control the power of a bidirectional three-phase interleaved converter. However,

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the proposal demands an impedance estimator to calculate the current in the output capacitor. It discusses only a few results regarding disturbance rejection, besides neither addressing the current unbalancing nor the output current ripple issues.

In 2016, two works [11] and [12] used predictive control techniques with long prediction horizons for regulated dc voltage source applications. [11] applied FCS-MPC in a two-phase interleaved converter considering only the regulation of the dc output-voltage in the minimization of the cost function, and [12] studied a four-phase converter, and its control includes the output current in the cost function.

In 2017, [13] proposed a long-horizon solution based on penalties to control a two-phase bidirectional interleaved converter topology with coupled inductors for a photovoltaic application with an energy storage system, feeding low-power resistive loads.

Between 2018 and 2020, Three studies [14], [15], and [16] compared the performance of MPC against a typical linear control strategy applied to interleaved converters and conclude that predictive control presents the faster dynamical response. In [14] and [16], the techniques need a Kalman filter to estimate the load.

III. TOPOLOGY

Figure 1 depicts the topology of the bidirectional N-phases interleaved converter: it consists of N switch pairs in parallel ($[S_n, \overline{S_n}]$), each one with a commutation inductance (L_1,...,L_N) connected to an output dc-link composed by a capacitance (C) and its parallel resistance (R_c), which has the function of discharging this capacitor when necessary; v_{dc1} and i_{dc1} are, respectively, the input voltage and current of the converter, while v_{dc2} and i_{dc2} are the output ones.

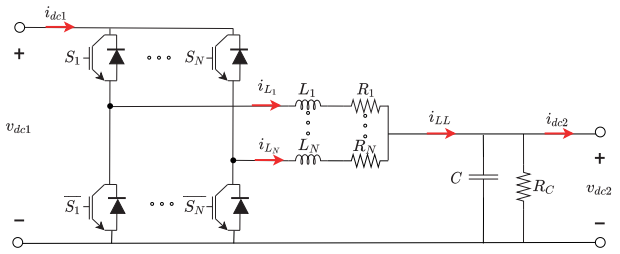

Fig. 1. Topology of the N-phase bidirectional interleaved converter.

Figure 2 shows the equivalent model of the converter, in which d_1,..., d_N are the duty cycles for each leg (phases) of the converter, and R_1,...,R_N and L_1,...,L_N are the resistances and inductances of the filter. This equivalent model leads to Equations (1) and (2).

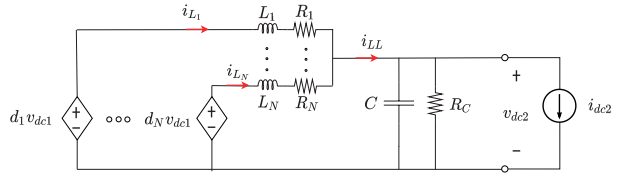

Fig. 2. Average model of the bidirectional interleaved converter.

The current source i_{dc2} represents the equivalent load and generation sources connected to the converter's output terminal.

Indeed, this resultant current works as a disturbance to the output voltage of the converter. Thus, the control must reject it by keeping the dc-link voltage regulated.

$$-d_n v_{dc1} + L_n \frac{\mathrm{d}i_{Ln}}{\mathrm{d}t} + R_n i_{Ln} + v_{dc2} = 0 \tag{1}$$

$$\sum_{n=1}^{N} i_{Ln} - i_{dc2} - C\frac{\mathrm{d}v_{dc2}}{\mathrm{d}t} - \frac{v_{dc2}}{R_c} = 0\,. \tag{2}$$

IV. PROPOSED CONTROL: IC-MPC

The proposed IC-MPC (Interleaved Current - Model Predictive Control) can be classified as an FCS-MPC since it applies the control actions directly to the converter's switches, without the need for a modulation stage.

Figure 3 shows the proposed control strategy providing the switching pulses to the interleaved converter, which performs a power-flow interface between dc links.

The proposed control must accomplish three main objectives to make the converter operate as a robust dc-dc interface:

- to keep the phase-currents balanced in steady-state;
- to provide a switching pattern that makes the interleaved converter operate with a low-ripple output current;
- to regulate the output voltage with a high disturbance rejection capability, i.e., the control must keep the voltage within a small range, even if facing high power variations.

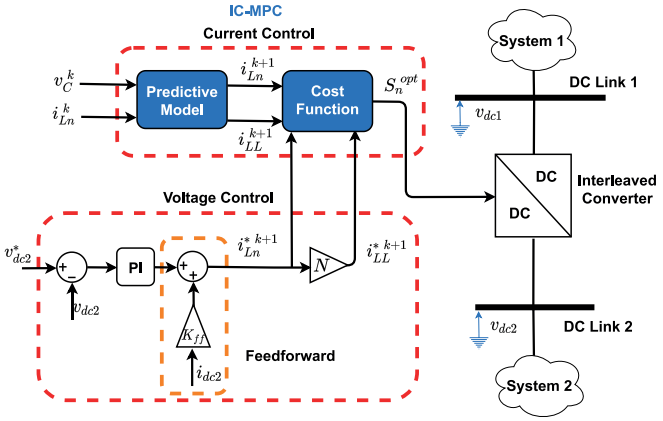

Fig. 3. Block Diagram of IC-MPC performing a dc power-flow interface between dc-links.

The proposed strategy addresses the first two objectives in the cost function of the IC-MPC and the third objective by adding a current feedforward in the voltage control loop.

The IC-MPC relies on two key elements, the predictive model and the cost function, being the latter part of the novelty of this paper.

The outer dc-voltage controller calculates the phase-current reference, $i_{Ln}^{*\,k+1}$, and the output current reference, $i_{LL}^{*\,k+1}$, which is obtained by multiplying $i_{Ln}^{*\,k+1}$ by the number of phases N.

The IC-MPC uses $i_{Ln}^{*\,k+1}$ to balance the phase currents and $i_{LL}^{*\,k+1}$ to shift the switching pulses to achieve the pattern that

accomplishes the ripple reduction goal in the output current (i_{LL}).

A. Predictive Model

The discretization of (1) and (2), using the forward Euler method, results in the predictive model of (3) and (4), in which T_s is the sampling period.

The IC-MPC evaluates the predictions of the phase currents i_{Ln}^{k+1} and the output currents i_{LL}^{k+1}, based on (3) and (4), for each one of the switching states (S_n).

$$i_{Ln}^{k+1} = i_{Ln}^{k} + \frac{T_s}{L_n}(S_n v_{dc1}^{k} - v_{dc2}^{k} - R_n i_{Ln}^{k}) \tag{3}$$

$$i_{LL}^{k+1} = \sum_{n=1}^{N} i_{Ln}^{k+1}\,. \tag{4}$$

The allowed switching-states of the converter consists of the combination of the states (*on* or *off*) of the switches of each one of the converter's phases (legs), $\{S_1,\ldots,S_N\}$, resulting in a total of 2^N states.

For instance, if the number of phases (N) is equal to 3, the total number of allowed switching states equals 8, as presented in Table I.

TABLE I
Interleaved Converter Switching States $(N = 3)$

Switching State	S_1	S_2	S_3
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

B. Cost Function

The cost function groups the MPC control objectives, which is keeping the dc currents of each phase $(i_{L1}\ldots i_{LN})$ balanced, given the reference i_{Ln}^{*}, while minimizing the ripple of the output current, i_{LL}.

Hence, the cost function must be a composition of these two objectives represented by g_1 and g_2 in (5) and (6), respectively.

Equation (5) implements the objective of regulation each phase current, given the reference i_{Ln}^{*}, while (6) aims at minimizing the ripple of i_{LL}.

$$g_1 = \sum_{n=1}^{N} ||i_{Ln}^{*} - i_{Ln}^{k+1}||^2 \tag{5}$$

$$g_2 = ||N i_{Ln}^{*} - i_{LL}^{k+1}||^2\,. \tag{6}$$

Indeed, g_2 intends to produce a switching pattern (over time) that minimizes the output current ripple by emulating the behavior of a typical interleaved modulation profile since this control dismisses the use of a modulator block.

Besides g_1 and g_2, the cost function takes advantage of a penalty strategy to protect the system from overcurrent, i.e., the IC-MPC dynamically controls the dc-currents during the standard operation but, when a high power variation occurs, it chooses the best control action to avoid overcurrent.

Another penalty included in the cost function considers the number of switch transitions during one sampling period.

Figure 4 depicts the flowchart of the penalty strategy adopted in the IC-MPC: for each of the converter's phases, if the predicted current overshoots a limit value, it adds a penalty value equal to P to the penalty function (H_n) – in this work. After that, the algorithm calculates the number of switch transitions, adding it to the penalty function.

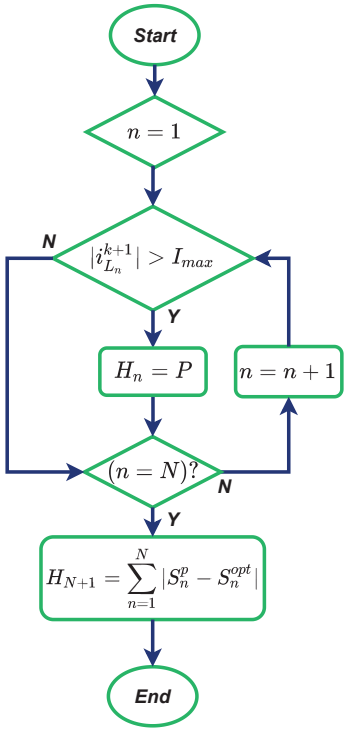

Fig. 4. Flowchart of the penalty strategy, including the overcurrent protection and the reduction of switching transitions.

The combination of g_1, g_2 and the penalty functions, H_n, lead to the cost function of (7), in which α and β are the respective weights of g_1 and g_2.

$$g^p = \alpha \sum_{n=1}^{N} ||i_{Ln}^{*} - i_{Ln}^{k+1}||^2 + \beta ||N i_{Ln}^{*} - i_{LL}^{k+1}||^2 + \sum_{n=1}^{N+1} H_n\,. \tag{7}$$

If α is greater than β, the control prioritizes the phase-current regulation, related to g_1, instead of the output-current ripple minimization, related to g_2. On the other hand, if β is greater than α, the control minimizes the output-current ripple at the cost of poor phase-current regulation, leading to undesired phase-currents unbalancing.

Although the design of these two parameters seems hard, leading to a trade-off between α, β, and the control objectives, the simple solution $\alpha = \beta = 1$ is enough to achieve both objectives. This discussion will be clarified by the results of the analysis presented in Section VIII, which compares the performance of these cost functions and demonstrates the effectiveness of using (8).

Hence, (7) turns into (8), which is a simpler solution that combine both objectives equally.

$$g^p = \sum_{n=1}^{N} ||i^*_{Ln} - i^{k+1}_{Ln}||^2 + ||Ni^*_{Ln} - i^{k+1}_{LL}||^2 + \sum_{n=1}^{N+1} H_n \,. \qquad (8)$$

Then, the IC-MPC algorithm evaluates the cost-function, g^p, for each prediction (p) — associated to each switching-state (see Table I) —, to select the optimal switching vector (S^{opt}) and apply it to the converter, as depicted in the flowchart of Figure 5, in which T_s is the sampling period; p is the prediction index; n_s is the number of switching states; g_{min} is the minimum value of the cost function; S^p is the switching state of the prediction p; and S^{opt} is the optimal switching state.

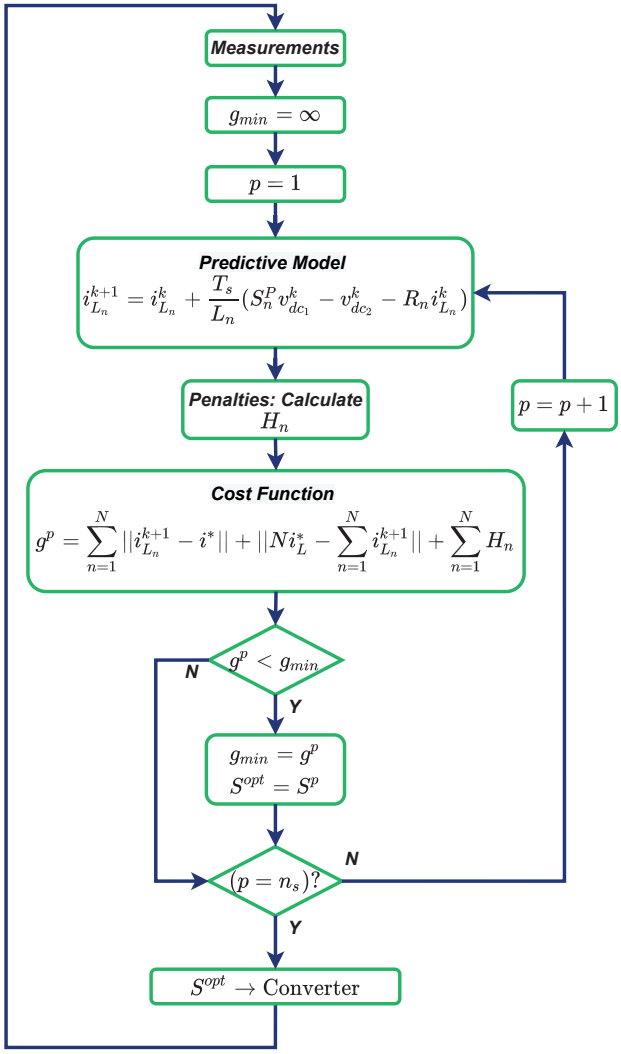

Fig. 5. Flowchart of the proposed IC-MPC algorithm.

V. VOLTAGE CONTROL

The outer voltage controller of Figure 3 provides the control references to the IC-MPC and consists of a PI regulator that tracks the control effort to be added to the feedforward signal to keep the dc voltage regulated. In other words, the feedforward rejects the load current disturbances, while the PI tracks the dc voltage reference.

A. Design of Voltage Regulator Gains

As previously stated, the IC-MPC has a fast dynamic response, which means its bandwidth is large enough to be neglected in the voltage control design, i.e., the IC-MPC tracks the current reference much faster than the outer controller (the voltage regulator), which is a common characteristic of cascade controllers.

Thus, in Figure 6 the methodology to design the voltage PI gains approximates the IC-MPC dynamics by a unitary gain block.

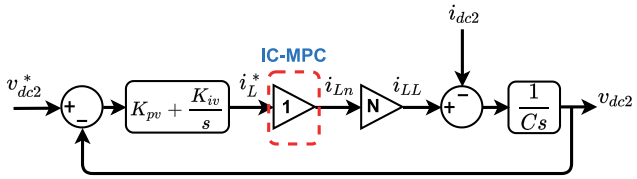

Fig. 6. Simplified block diagram for designing the gains of the voltage control closed-loop.

Based on this closed-loop and using Gao's Method [18], one can size the proportional and integral gains (K_{pv} and K_{iv}) as follows:

$$K_{pv} = \frac{\omega_v C}{N} \qquad (9)$$

$$K_{iv} = \frac{\omega_v}{R_c N} \,. \qquad (10)$$

Where ω_v is the desired voltage loop bandwidth, in rad/s.

The Gao's method applied to this system ensures the desired voltage loop bandwidth (ω_v) and an elevated phase-margin of almost 90º if $\omega_v << \omega_c$.

However, ω_c is unknown, which makes it necessary to estimate it. This work also addresses this matter — in the following sections — by proposing a method to estimate ω_c.

B. Current Feedforward

Although (9) and (10) provide a desired reference tracking dynamics, i.e., a desired voltage-control bandwidth, their disturbance rejection capability is poor.

Elevating the integral gain (K_{iv}) increases the overall stiffness, leading to a better disturbance rejection response, but at the cost of phase margin reduction. However, the simple addition of the current feedforward bypasses this problem, increasing the disturbance rejection capability while keeping the phase margin near 90º.

The block diagram of Figure 7 includes this addition, i.e., the feedforward loop, and the dynamics of the IC-MPC as a low-pass filter with unity gain and bandwidth equals ω_c, which yet needs to be estimated.

Since the voltage control loop generates the current reference for each phase of the interleaved converter, its value is exactly equal to the load current (i_{dc2}) divided by N.

This approach removes the burden of tracking the load disturbance control effort from the voltage controller; the outer loop only evaluates the control effort to keep the dc-link regulated, enabling a significant improvement in the system's dynamic response when subjected to load disturbances.

The transfer function presented in (11) gives the frequency response of the effect of the load disturbance $I_{dc2}(s)$ in the dc-

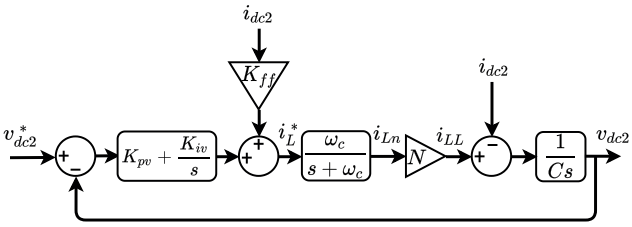

Fig. 7. Block diagram of the voltage control closed-loop with the current feedforward and considering the dynamical response of the IC-MPC.

link voltage $V_{dc2}(s)$.

$$\frac{V_{dc2}(s)}{I_{dc2}(s)} = \frac{-s^2 + s\omega_c(K_{ff}N - 1)}{Cs^3 + C\omega_c s^2 + N\omega_c K_{pv} s + N\omega_c K_{iv}}. \qquad (11)$$

By replacing the gains K_{pv} and K_{iv} with the values calculated by Gao's method in (9) and (10), and considering $K_{ff} = 1/N$, the disturbance transfer function can be rewritten as:

$$\frac{V_{dc2}(s)}{I_{dc2}(s)} = -\frac{s^2}{Cs^3 + C\omega_c s^2 + C\omega_c\omega_v s + \omega_c\omega_v R_c^{-1}}. \qquad (12)$$

Figure 8 demonstrates the elevated improvement in the disturbance rejection by using the feedforward, which results in a frequency response with reduced sensibility, i.e., the dc-link voltage ($V_{dc2}(s)$) suffers a lower effect (lower gain in dB) given the load or generation disturbances ($I_{dc2}(s)$).

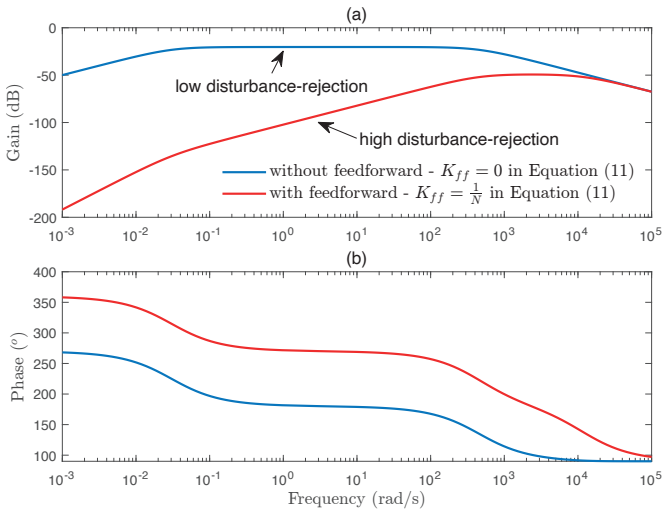

Fig. 8. Frequency response of the load disturbance rejection of Equation (11) with $\left(K_{ff} = \frac{1}{N}\right)$ and without $\left(K_{ff} = 0\right)$ the current feedforward.

VI. CONTROL ANALYSIS

The scope of the following analyses consists of simulating the system's response for different values of ω_v, within the range of $40\pi\ rad/s$ and $200\pi\ rad/s$ (20 Hz-100 Hz). The remaining sections of this work present the results of several analyses regarding the IC-MPC performance. The system of Figure 3 was simulated in PSCAD/EMTDC with the interleaved converter of Figure 1. Table II shows the filter parameters and the system rated values; in all analyses, the sampling frequency is 20 kHz, resulting in an average switching frequency is 9.35 kHz in steady-state.

Figure 9 shows that the proposed control regulates the output voltage with no overshoot, independently of the value of ω_v. In other words, the design of the control gains ensures a phase margin of approximately 90º.

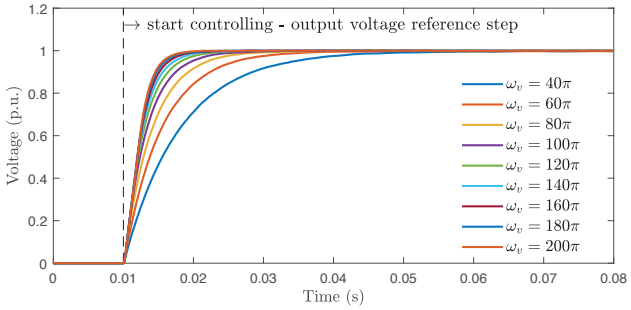

Fig. 9. Step response of the voltage regulator, varying ω_v.

A. Disturbance Rejection And Reference Tracking

Figure 10.a shows the fast and low-sensitivity disturbance rejection response of the proposed control, keeping the dc-link within the range of 2%, for values of ω_v between $40\pi\ rad/s$ and $140\pi\ rad/s$, during a load disturbance of 1 p.u.; (b) and (c) depicts the fast reference tracking dynamics that, along with the feedforward, ensures this performance.

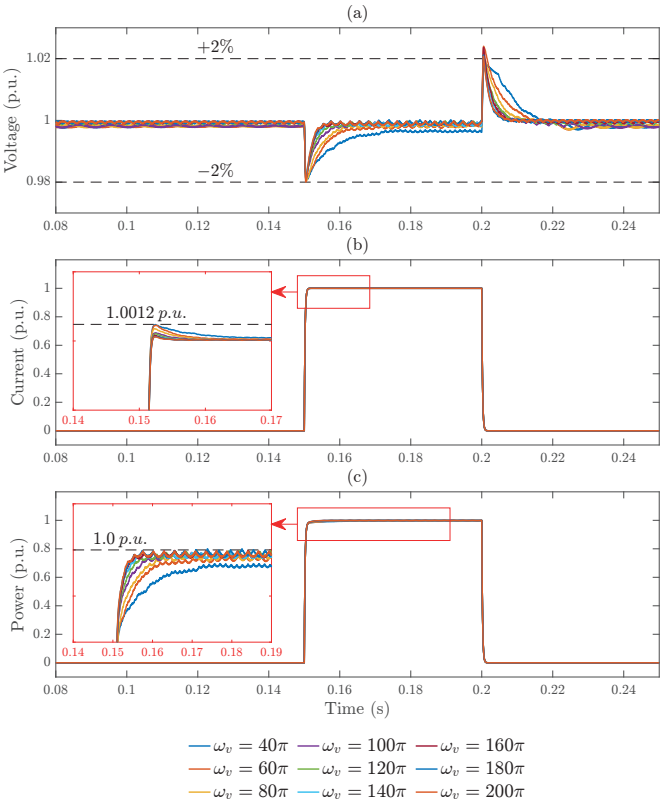

Fig. 10. IC-MPC load disturbance rejection performance: output voltage (v_{dc2}) (a), load current (i_{dc2}) (b), and power (p_{dc}) (c).

The non-overshooting response remains even in a total power reversing (see Figure 11.b), i.e., a power variation of

2 p.u. However, the voltage swell overs 10 % (see Figure 11.a), independent of ω_v, but the voltage profiles present no oscillations.

Figure 12.b shows the high disturbance rejection capability of the IC-MPC, with a voltage variation lower than 1%, when facing a scenario of input voltage steps of 20% (a). This performance upraises from the fast response of the IC-MPC and the evaluation of the input voltage in the predictive model (see (3)).

TABLE II
System Parameters

Filter Parameters	
L_n	$2\,mH$
C	$3.3\,mF$
R_C	$10\,k\Omega$
N	3
Electrical Parameters	
Rated Input Dc Voltage	$980\,V_{dc}$
Rated Output Voltage	$450\,V_{dc}$
Rated Power	$150\,kW$
IC-MPC	
Sampling Frequency - F_s	$20\,kHz$
Penalty Value - P	100
Average Switching Frequency	$9.35kHz$

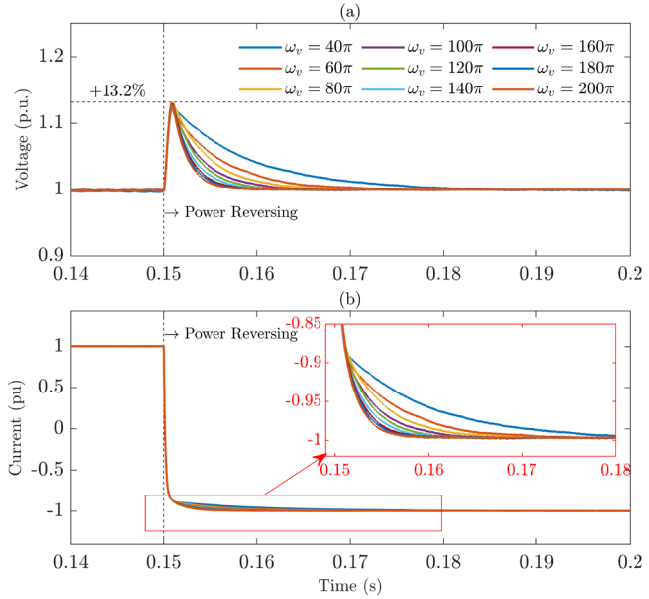

Fig. 11. IC-MPC disturbance rejection performance under total power reversing scenario: (a)output voltage (v_{dc2}) and (b) load current.

VII. IC-MPC BANDWIDTH ESTIMATION

Despite the unknown value of ω_c in Figure 7, one can design the voltage regulator gains through (9) and (10), which ensures a desired voltage control bandwidth equals to ω_v and makes it possible to estimate the value of ω_c by measuring the disturbance rejection capability of the system, i.e., the value of the dc-voltage sag ($A_{p.u.}$) after a load step of 1 p.u.

The sensibility of the dc voltage towards a load step depends on three variables: the dc-link capacitance (C) and the bandwidths of both IC-MPC (ω_c) and voltage control (ω_v).

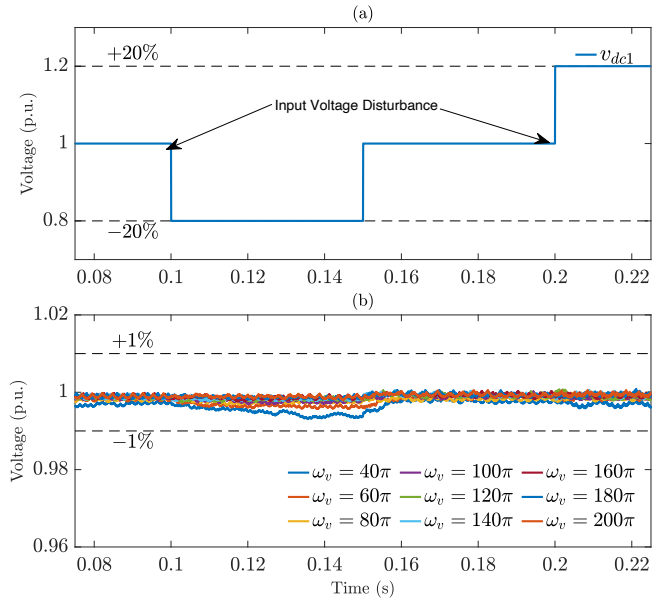

Fig. 12. IC-MPC disturbance rejection performance under input voltage disturbance scenario: (a) input voltage (v_{dc1})(b) and output voltage (v_{dc2}).

Figure 13 depicts the percent value of dc-voltage Sag ($A(\%)$) for different values of the ω_v simulated in the software PSCAD/EMTDC and the estimated IC-MPC bandwidth for each case; the analysis evaluates an optimization over a mean square error function using (13), which leads to an average IC-MPC bandwidth (ω_c) of $1795\,Hz$.

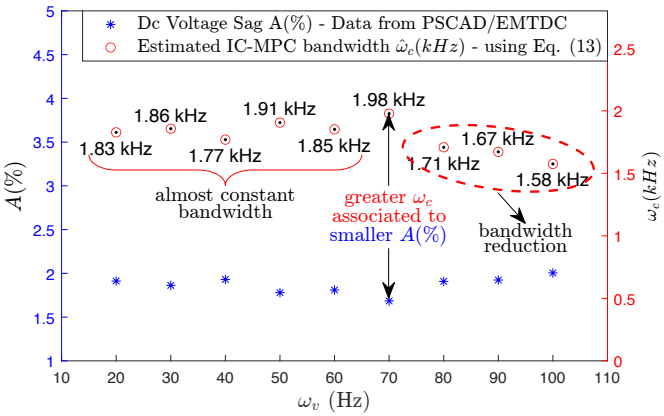

Fig. 13. Estimation of the IC-MPC bandwidth, ω_c, based on (13) and the data of voltage sags ($A(\%)$).

The higher the value of C, the lower the dc-voltage sag ($A_{p.u.}$), given a load step, because of the increased voltage inertia of the dc-link. Moreover, the higher the values of ω_c and ω_v, the lower the dc-voltage sag ($A_{p.u.}$), since both control-loops will reject the disturbance faster, therefore leading to a reduced sensibility.

Equation (13) quantifies the value of the dc-voltage sag ($A_{p.u.}$) of the system of Figure 7 (given a load step of 1 p.u.) as a function of C, ω_c, ω_v, and the dc voltage (V_{base}) and the dc current (I_{base}) bases. Thus, based on the knowledge of C and ω_v, one can estimate the value of IC-MPC bandwidth.

$$A^{pu}(\omega_c) = \frac{I_{\text{base}}}{V_{\text{base}}} \frac{\omega_c}{C(\omega_c + \omega_v)^2}. \quad (13)$$

If we assess the same method for each value of ω_v, it leads to two conclusions: IC-MPC bandwidth varies with ω_v and achieves the fast response when $\omega_v = 70\,Hz$.

In Figure 13, the data show that ω_c presents few variations until the value of $\omega_v = 60\,Hz$. After that, ω_c reaches a maximum value of $1.98\,kHz$, when $\omega_v = 70\,Hz$ — which agrees with the result of Figure 10.a —, and starts to decrease for values of voltage control bandwidth (ω_v) greater than $70\,Hz$, as highlighted in Figure 13; this behavior leads to a reduction in the disturbance rejection capability, i.e., a rise in the voltage sag ($A(\%)$). Based on these findings, the analyses the following sections use $\omega_v = 70\,Hz$.

VIII. RIPPLE REDUCTION AND CURRENTS BALANCING

Figure 14 shows two different scenarios with the inclusion of only g_1 or g_2 in the cost function g^p; (a) and (b) depicts the phase planes of the phase currents (i_{Ln}) vs. the output voltage (v_{dc2}), while (c) shows the waveform of the output current for both scenarios.

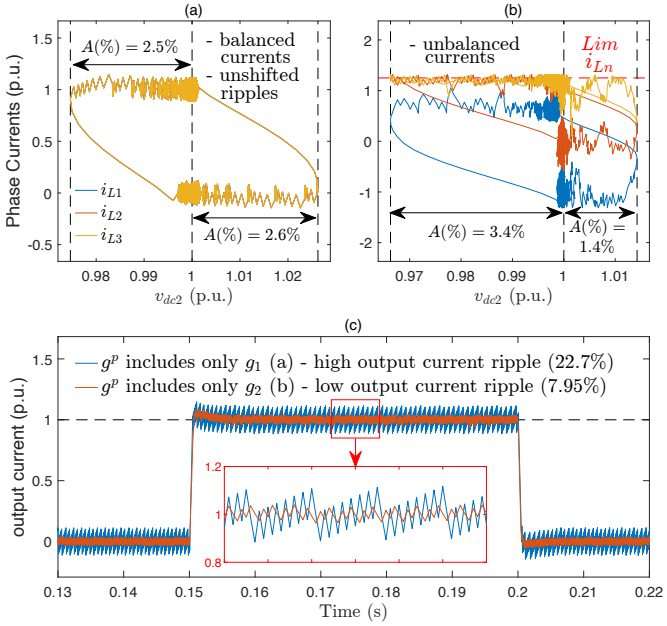

Fig. 14. Analysis of the effect of including only g_1 or g_2 in the cost function g^p: phase-planes of the phase currents vs. the output voltage with only g_1 ($\alpha = 0.0$ and $\beta = 1.0$) (a) and with only g_2 ($\alpha = 1.0$ and $\beta = 0.0$) (b); waveform of the output current (c) for both cases.

In (a), the scenario with the inclusion of only g_1 in the cost function results in balanced currents, but with non-shifted ripples, resulting in an output current waveform (see (c)) with a non-reduced ripple profile. Also, this scenario presents symmetrical values of $A(\%)$ in the phase-plane.

On the other hand, using only g_2 in the cost functions leads to ripple reduction in the output current (see (c)), but at the cost of unbalanced phase currents and unsymmetrical step response in the value $A(\%)$, as seen in the phase-plane of (b). Still in the case of the cost function that includes only g_2, the penalty strategy contributes to unbalancing reduction problem in the heavy load scenario (see (b)) but does not affect the case of light load.

Figure 15.a exemplifies the phase current unbalancing problem in interleaved converters in both light and heavy load scenarios; in this case, the control does not include the current balancing in the cost function. On the other hand, (b) and (c) show the results of the proposed controller with both g_1 and g_2 in the cost function, i.e., using (8): (c) demonstrates that the IC-MPC balances the phase currents (these with high ripple) in light and heavy load scenarios, while (b) depicts the output current with reduced ripple.

The contrast between the results of Figure 15.a against 15.b and 15.c confirms that the IC-MPC accomplishes the remaining control objectives of balancing phase currents and reducing the output current ripple.

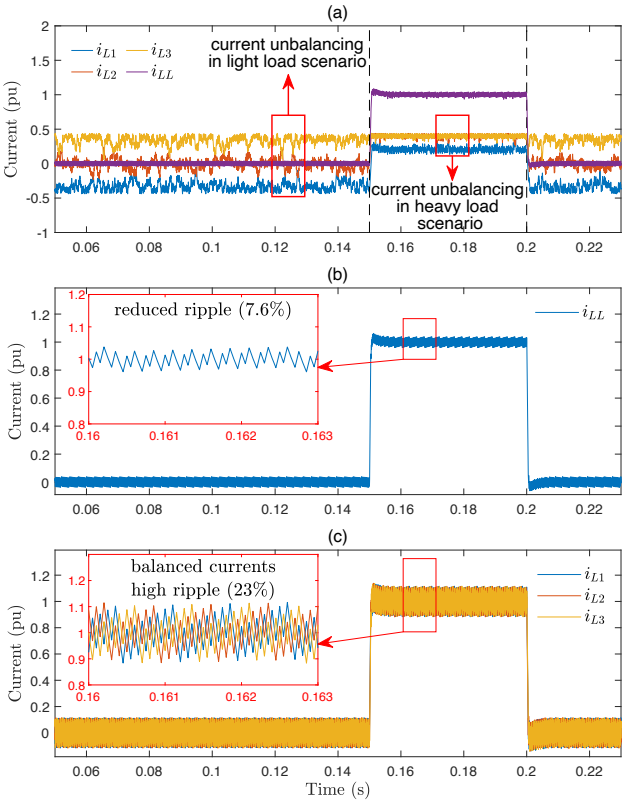

Fig. 15. Analysis of the current balancing: typical unbalanced phase currents in interleaved converters (a), output-current with reduced ripple (b) and balanced phase-currents (c) — both (b) and (c) use the cost function (8) ($\alpha = \beta = 1.0$).

IX. ANALYSIS UNDER RIP LOADS AND GENERATIONS

The results of Figure 16 reinforces the finding of the accomplishment of the three control objectives even when the converter is under a RIP load-and-generation profile with random nonlinear characteristics.

The RIP profile consists of a set of resistive loads (R-type), current sources (I-type), and constant power sources (P-type), with their power ratios changing randomly every 50ms; the RIP load-and-generation units are connected to the terminals

of the dc-link 2 (see Figure 3).

Figure 16.a shows the high stiffness of the IC-MPC, rejecting the load and generation disturbances caused by the RIP Power variation (P_R,P_I,P_P) shown in (b). Even in the worst cases, in which the output voltage sag reaches values below than 2%, the recovery time is less than 3 ms.

These results confirm that the proposed control provides a solution with a low sensibility and no overshot in power steps; during the operation of the converter, the proposed control strategy keeps the phase currents balanced while producing a reduced output current ripple solution (see (c)), independent of the values of RIP.

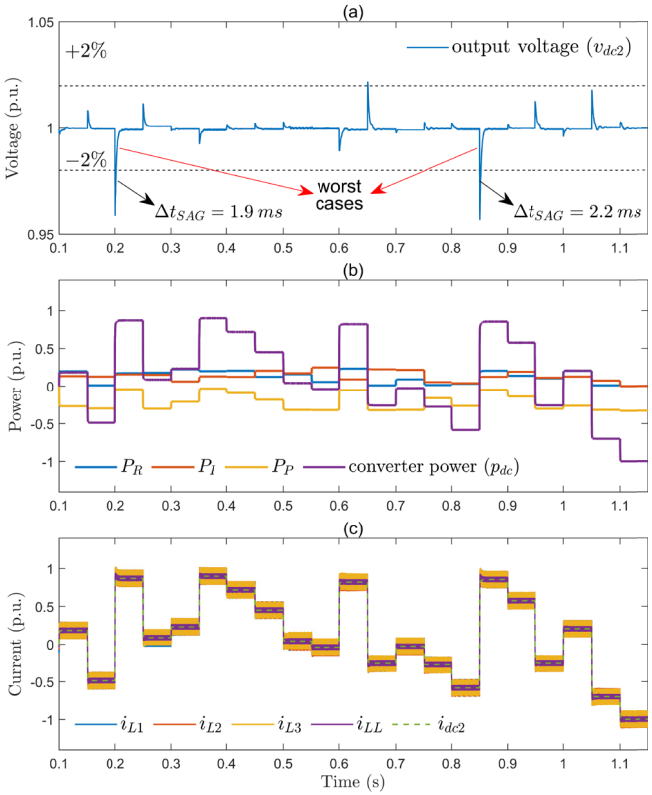

Fig. 16. Operation of the interleaved converter under a RIP random profile: output voltage (a); converter's power (b); phase currents, output current, and dc-system 2 current (c).

X. CONCLUSIONS

The findings of this work demonstrate that the proposed IC-MPC achieves three goals for the interleaved converter operating as a dc power-flow interface: i.) phase-current balancing, ii.) output current ripple reduction — both features proved by the analysis of section VIII and the results of section IX —, and iii.) high disturbance rejection capability, confirmed by the analysis and results of section VI, and supported by the data of section VII and the simulations of section IX.

In summary, the voltage control design ensures the desired reference-tracking response, and the feedforward, with the proper selection of voltage-control bandwidth, leads to an overall control solution with high disturbance rejection capability.

Indeed, the proposed solution operates with high stiffness even under a constant power load and generation profile.

Moreover, the penalty strategy successfully prevents overcurrent in the converter's phase without producing any imbalance.

This work further introduced a method to estimate the bandwidth of the predictive control loop. The outcomes of this analysis confirm that this class of predictive control presents variable bandwidth. However, a proper selection of ω_v ensures a high value of (ω_c), thus a stiff rejection capability.

Future investigations can extend the bandwidth estimation method for other MPC applications and analyze the impact of switching states' transitions in the cost function on both the estimated bandwidth and switching frequency profile.

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