ANALYSIS, DESIGN, AND EXPERIMENTATION OF A BUCK CONVERTER BASED ON THE THREE-STATE SWITCHING CELL OPERATING IN OVERLAPPING MODE

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***Abstract* - This work presents the detailed analysis of the dc-dc nonisolated buck converter based on the three-state switching cell operating in overlapping mode, which occurs when the duty cycle of the active switches is higher than 0.5. Only part of the load power is processed by the active switches due to the use of the autotransformer, thus reducing the peak current through the switches to half of the load current, as higher power levels can then be achieved by the proposed topology. The volume of reactive elements i.e. inductors and capacitors is also decreased since the ripple frequency of the output voltage is twice the switching frequency. Due to the intrinsic characteristics of the topology, total losses are distributed among all semiconductors. Another advantage of this converter is the reduced region for discontinuous conduction mode when compared to the conventional buck converter as demonstrated by the static gain plot. Besides, the input current is continuous and the ripple current is reduced, what is not verified in the classical buck converter. The theoretical approach is detailed through qualitative and quantitative analyses, design procedure, and a comparison with similar topologies. Finally, an experimental prototype rated at 1 kW is implemented, while the main experimental results are presented and adequately discussed to clearly identify its claimed advantages.**

***Keywords* - Buck Converter, DC-DC Converters, Three-State Switching Cell, 3SSC.**

I. INTRODUCTION

PWM (Pulse Width Modulation) DC-DC converters are widely employed in numerous applications e.g. audio amplifiers [1], UPSs (Uninterruptible Power Supplies) [2], fuel cell powered systems [3], and fork lift vehicles [4], although many other ones can be easily found. Conventional hard switching converters with a single active switch such as buck, boost, buck-boost, Ćuk, SEPIC (Single Ended Primary Inductance Converter), and zeta typically present low power density, while attempts to further minimize the size of filter elements lead to increased switching losses, compromising the efficiency of the converters.

In order to overcome such limitation, several soft switching approaches have been introduced in literature. Soft switching is supposed to reduce the overlap between voltage and current during the commutation, and can be classified in either active or passive methods, as one must choose between the aforementioned snubbers for a given application.

Active methods can reduce the switching losses by using auxiliary switches. Unfortunately, an auxiliary switch increases the complexity of both power and control circuits. Synchronization problems between control signals of the switches during transient also complicate the control strategy. Circuit cost is increased and reliability is affected by using active snubbers [5].

A passive lossless snubber can effectively restrict switching losses and EMI noise using no active components and no power dissipative components. No additional control is needed and no circulating energy is generated. Circuit structure is as simple as RCD (resistor-capacitor-diode) snubbers while circuit efficiency is as high as active snubbers and resonant converters [6] [7]. Low cost, high performance, and high reliability are the distinct advantages of a passive lossless snubber [8]. However, soft switching may not be achieved for the entire load range, and besides the accurate design of the resonant tank is not a trivial task, what is also valid when active snubbers are considered [9].

Significant effort has then been made to improve the characteristics of the traditional nonisolated dc-dc converters in the last few years. For instance, the study of a dc–dc buck converter with three-level buck clamping, zero voltage switching (ZVS), active clamping, and constant-frequency pulse width modulation (PWM) is proposed in [10]. A family of converters is also derived, which combines the advantages of reduced voltage across the switches using a three-level commutation cell, and decreased switching losses obtained from a soft switching technique.

As the power rating increases, it is often required to associate converters in series or in parallel. By using interleaving techniques in high current applications, the currents through the switches become just fractions of the input current [11]. Interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, as the size of the energy storage inductors and

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differential-mode electromagnetic interference (EMI) filter in resulting implementations can be reduced [12].

The three-state switching cell (3SSC), which can be obtained by the association of two two-state PWM cells (2SSC) interconnected to a center tap autotransformer, was initially proposed in [13]. The aforementioned work introduced a novel family of nonisolated dc-dc converters for high-power high-current applications, which are the buck, boost, buck-boost, Ćuk, SEPIC, and Zeta topologies. The approach is similar to the interleaving technique and current sharing is maintained to the use of the autotransformer with unity turns ratio, which is responsible for balancing the currents through each one of the main switches. Considering low current applications, the effect of low frequency content in the current balance is negligible because the resistances of the semiconductors, windings, and associated elements are relatively large. However, higher currents are supposed to be measured to avoid unbalance and assure proper current sharing, similarly to the interleaved approach.

General advantages over conventional topologies can be achieved e.g. the inductor is designed for twice the switching frequency, with consequent reduction of size and weight; the current through the switches is half of the input current; part of the input power is delivered to the load by the transformer instead of the main switches, consequently reducing conduction and commutation losses; lower cost switches can be used. However, high component count results if the topologies presented in [13] are compared with the classical nonisolated dc-dc converters.

Many converters based on the concept of the 3SSC have been proposed so far [14]-[18]. However, most of the works are basically concerned with high voltage gain boost-based topologies dedicated to dc voltage step-up applications. The 3SSC-based buck converter initially mentioned in [13] is thoroughly analyzed in [19], where an extensive comparison with the conventional interleaved buck converter and other similar topologies is properly established. The analysis shows that the buck converter based on the 3SSC presents improved performance, making it a proper choice for high-power high-current applications [19].

The buck, boost, buck-boost, Ćuk, SEPIC, and zeta topologies based on the 3SSC are able to operate under two modes regarding the main switches. If the duty cycle D is higher than 0.5, overlapping mode (OM) occurs, where two switches remain turned on at the same time [13]. Otherwise, if D<0.5, the converter operates in nonoverlapping mode (NOM), while only one switch remains turned on [13].

The study carried out in [19] has been focused in NOM only, as the analysis of the converter operating in both modes has not yet been presented. Even though the 3SSC-based buck converter itself is not new, this paper is dedicated to the detailed analysis of the aforementioned topology considering the OM. Analogously to the conventional buck converter, the structure is also able to operate in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM). The design procedure of the converter will be presented in detail, so that an experimental prototype can be implemented. The discussion of experimental results is supposed to validate the theoretical assumptions and also demonstrate the merit of the proposal.

II. 3SSC-BASED BUCK CONVERTER OPERATING IN OM

The canonical switching cell is an approach that allows obtaining and classifying the classical dc-dc converters, from which some families of converters can be derived [20]. Buck, boost, and buck-boost converters, which are second order systems, as well as Cúk, SEPIC, and zeta, which are fourth other systems, have a single switching cell that is part of their respective power stages. Literature has also shown appreciable effort to improve the characteristics of the original structures, even though the novel resulting topologies are more complex approaches with higher component count.

The 3SSC comes as an effort that allows the conception of novel converters adequate for high-current applications. This approach is not supposed to be confused with the well-known interleaving technique, where current sharing may be compromised due to eventual inherent differences regarding the active switches and inductors used in the multiple phases.

According to the explanation given in [13] and [19], the 3SSC is formed by two controlled switches S_1 and S_2, two diodes D_1 and D_2, one autotransformer $T_1||T_2$, and one inductor L. Even though the resulting cell seems more complex with higher component count than the conventional 2SSC, the advantages over its counterpart have been clearly demonstrated in literature [14]-[19] [21]. Besides, current sharing is ensured by the autotransformer.

As it was mentioned before, and considering that the operation of the switch and the diode of a same leg is complementary, two modes regarding the main switches result for the proposed topology. If the duty cycle D is higher than 0.5, the converter operates in OM, while two switches remain turned on simultaneously. In the other hand, a single active switch is responsible for conducting the load current in a given operating stage if the converter operates in NOM.

Of course, depending on the conversion ratio involving the input voltage and the output voltage, the duty cycle may assume several values. In the case of the conventional buck converter, the analysis of the operating stages in CCM, DCM, and CRM is valid for 0<D<1. However, the study of the 3SSC-based buck converter proposed in [13] and [19] involves two distinct analyses for D<0.5 (NOM) and D>0.5 (OM), as the latter one has not yet been presented and is the scope of this paper.

A. Operation of The Converter in OM

Initially, let us consider the structure represented in Figure 1, whose operation in NOM was analyzed in [19]. For the detailed description of the dc-dc buck converter using the 3SSC in OM, the following assumptions are made:

- the converter operates in steady state;
- switching frequency is constant and PWM is employed to drive the switches;
- the gating signals of the switches are 180° displaced;
- the turns ratio of the autotransformer is unity;
- the magnetizing current is much lower than the load current;
- all semiconductor and passive elements are ideal.

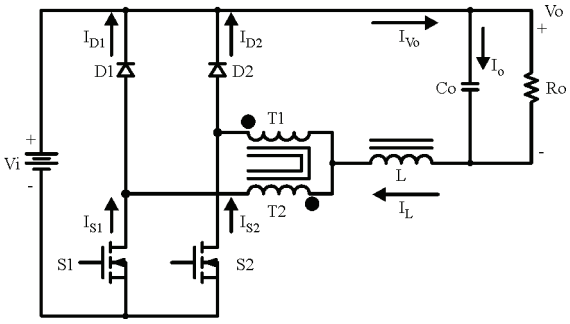


Fig. 1. Buck converter based on the 3SSC.

The following variables will be employed in the forthcoming analysis and are defined as follows:

$V_{g(S1)}$, $V_{g(S2)}$: gating signals applied to switches S_1 and S_2, respectively;

I_L: current through inductor L, while the maximum and minimum values assumed by this quantity are I_M and I_m, respectively;

I_{S1}, I_{S2}: currents through switch S_1 and S_2, respectively;

I_{D1}, I_{D2}: currents through diodes D_1 and D_2, respectively;

I_o: load current;

I_{T1}, I_{T2}: currents through the windings of the autotransformer;

I_{Vo}: current through the output stage, which is the sum of the currents through the capacitor (I_{Co}) and the load (I_o);

V_{S1}, V_{S2}: voltages across switches S_1 and S_2, respectively;

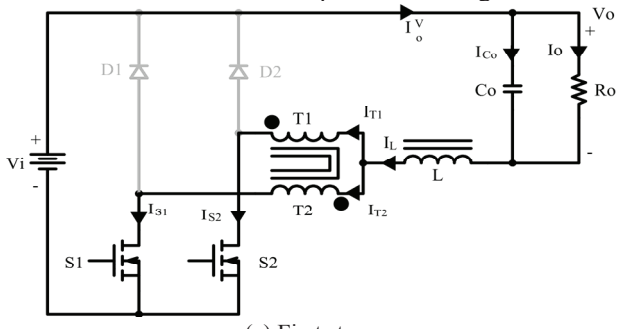
V_{D1}, V_{D2}: voltage across diode D_1 and D_2, respectively;

V_L: voltage across inductor L.

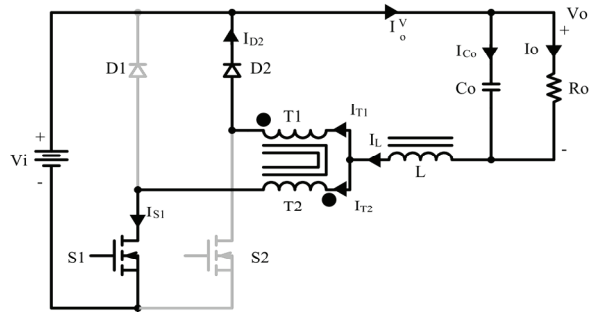
The operation of the converter in OM considering the CCM, DCM, and CRM is presented as follows.

1) CCM

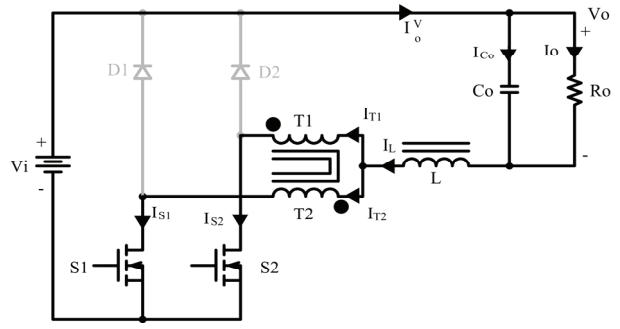
The converter operation can be defined according to four operating stages as shown in Figure 2, while the respective main theoretical waveforms are presented in Figure 3.



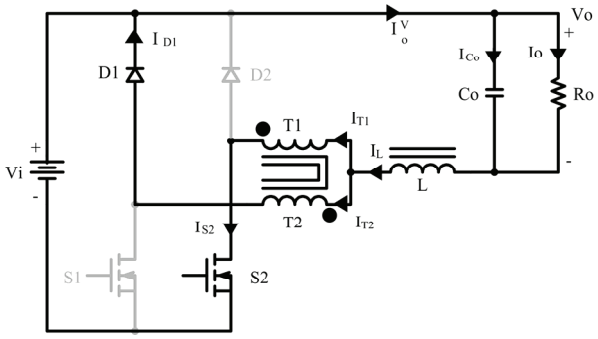
(a) First stage



(b) Second stage



(c) Third stage



(d) Fourth stage

Fig. 2. Operating stages of the proposed converter in OM-CCM.

First stage $[t_0, t_1]$ (Figure 2 (a)): Initially, switch S_1 is turned on, while switch S_2 also remains turned on. Diodes D_1 and D_2 are reverse biased. One part of the inductor current flows through T_1 and S_1, and the remaining one flows through T_2 and S_2. By adopting the same number of turns for T_1 and T_2, current sharing is maintained. The opposite polarity between the windings causes the voltage across the windings to be null, what represents a short-circuit. Moreover, inductor L stores energy and the current through it increases linearly. During this stage, only the output capacitor C_o provides power to the load, and it finishes when S_2 is turned off.

Second stage $[t_1, t_2]$ (Figure 2 (b)): Switch S_2 is turned off and S_1 remains turned on. The voltage across the inductor is inverted. Diode D_2 is forward biased while D_1 is reverse biased. The inductor current is divided into two parts. Energy transfer then occurs from T_1-S_1 and T_2-D_2 to the load, what means that only part of the load power is processed by the active switch, thus reducing the peak current through it. Moreover, the current decreases linearly, transferring the energy previously stored in inductor L and also energy from the source to the load. Since T_1 and T_2 have the same number of turns, current sharing is maintained. Analogously to the first stage, the current returns to the source. This stage finishes when switch S_2 is turned on.

Third stage $[t_2, t_3]$ (Figure 2 (c)): This stage is similar to the first one, although switch S_2 will be turned on while switch S_1 remains also turned on. Diodes D_1 and D_2 are also reverse biased. Similarly to the first stage, only the output capacitor provides energy to the load.

Fourth stage $[t_3, t_4]$ (Figure 2 (d)): This stage is similar to the second one, although switch S_1 is turned off while switch S_2 remains turned on. Diode D_1 is forward biased whereas D_2 is reverse biased. This way, energy is transferred from the input source and the inductor to the load.

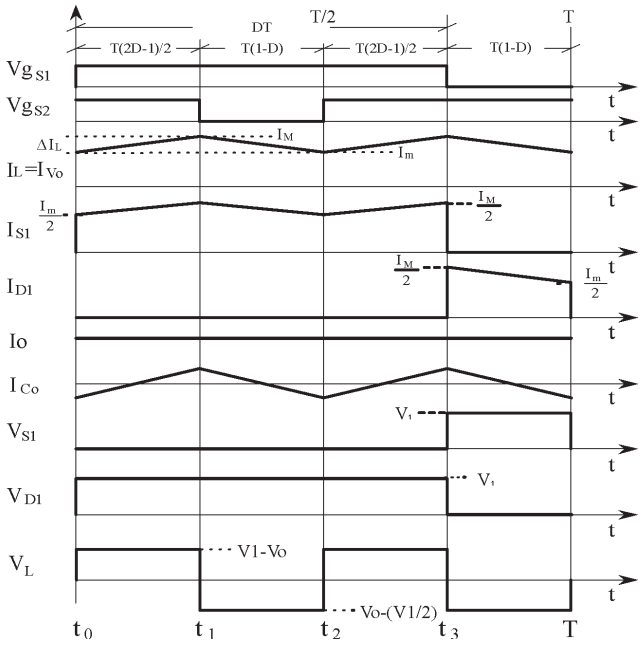


Fig. 3. Main theoretical waveforms for OM-CCM.

2) DCM

This conduction mode occurs when the current through inductor *L* becomes null during half of the switching period. The converter operation can be defined according to six operating stages, including Figure 4, while the respective main theoretical waveforms are presented in Figure 5. It must be mentioned that some of the equivalent circuits are identical to those previously described in Section II.1) and will not be discussed in detail once again.

First stage [t_0, t_1] (Figure 2 (a)) and second stage [t_1, t_2] (Figure 2 (b)): they are identical to the first and second stages in OM-CCM, respectively.

Third stage [t_2, t_3] (Figure 4): At the beginning of this stage, diode D_2 is reverse biased, and diode D_1 also is. Even though a gating signal is applied to switch S_1, there is no current flowing through it. Switch S_1 remains turned off as well. Thus, the current through *L* becomes null and there is no power transfer from the input source to the load. Output capacitor C_o provides energy to the load instead. This stage finishes when switch S_2 is turned on.

Fourth stage [t_3, t_4] (Figure 2 (c)) and fifth stage [t_4, t_5] (Figure 2 (d)): they are identical to the third and fourth stages in OM-CCM, respectively.

Sixth stage [t_5, t_6] (Figure 4): This stage is identical to the third one.

3) CRM

The analysis of the CRM is based on the study developed for the previous conduction modes and is required so that the static characteristic of the converter operating in OM is determined. The current and voltage waveforms regarding the inductor are presented in Figure 6. In this case, the minimum current through *L* is null, that is, it is equal to zero for a single time instant. The current ripple through *L* is then equal to the maximum current I_M.

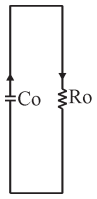


Fig. 4. Third and sixth stages of the proposed converter in OM-DCM.

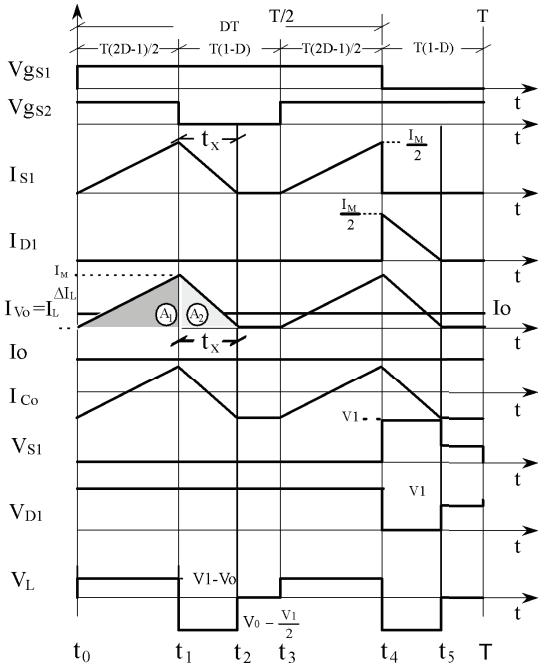


Fig. 5. Main theoretical waveforms for OM-DCM.

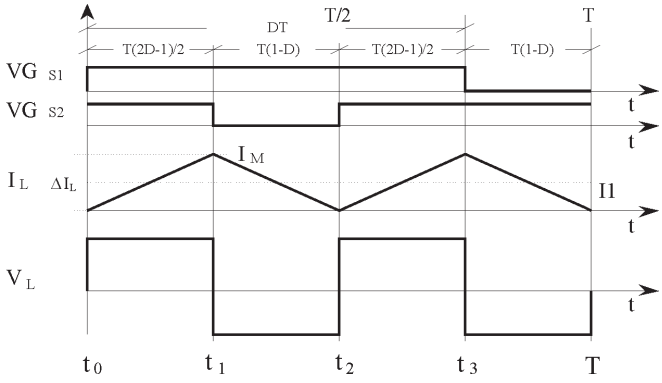


Fig. 6. Main theoretical waveforms for OM-CRM.

B. Output Characteristic of the Converter in OM

The static gain expressions for the converter operating in CCM, DCM, and CRM are given by (1), (2), and (3), respectively. Analogously to the NOM [19], the static gain in CCM is the same as that of the conventional buck converter.

$$G_{CCM\_OM} = \frac{V_0}{V_i} = D \tag{1}$$

$$G_{DCM\_OM} = \frac{\gamma' + (2 \cdot D - 1)}{2 \cdot \gamma' + (2 \cdot D - 1)} \tag{2}$$

$$G_{CRM\_OM} = \frac{3}{4} \pm \frac{1}{4} \cdot \sqrt{1 - 8 \cdot \gamma'} \quad (3)$$

Where:

$$\gamma' = \frac{4 \cdot L_b \cdot I_o}{V_i \cdot T_s} \quad (4)$$

Where T_s is the switching period.

From expressions (1) to (3), it is possible to determine the static gain of the proposed converter operating at D>0.5, as the generic curves are presented in Figure 7.

Analogously to the conventional buck converter, the output voltage is dependent on the load current in DCM. Besides, the EMI levels tend to increase in this mode. However, soft switching of the main switches can be achieved, at the cost of higher current stresses. It is worth to mention that the maximum static gain in CRM occurs at γ=0.0625 and D=0.75 for the proposed topology (Figure 7). Considering the classic buck converter, the maximum gain in CRM is verified when γ=0.25 and D=0.5. In practical terms, it means that the CCM region is wider for the analyzed converter. Besides, for a given operating point, the inductance becomes one fourth of that required for the conventional buck converter. Therefore, these are distinct advantages of the 3SSC buck topology operating in OM.

C. Filter Elements

The ripple current through the inductor (ΔI_L) is given as:

$$\Delta I_L = \frac{(1-D) \cdot (2 \cdot D - 1)}{2} \cdot \frac{T_s \cdot V_i}{L} \quad (5)$$

Expression (5) can be normalized so that the maximum ripple current is obtained as:

$$\beta = \frac{L \cdot \Delta I_L}{T_s \cdot V_i} = \frac{(2 \cdot D - 1) \cdot (1 - D)}{2} \quad (6)$$

Expression (6) is plotted in Figure 8, where one can see that the maximum ripple current occurs at D=0.75 and β=0.125.

By choosing arbitrarily the ripple current, the inductance can be determined as:

$$L = \frac{(2 \cdot D - 1) \cdot (1 - D) \cdot T_s \cdot V_i}{2 \cdot \Delta I_L} = \beta \cdot \frac{T_s \cdot V_i}{\Delta I_L} \quad (7)$$

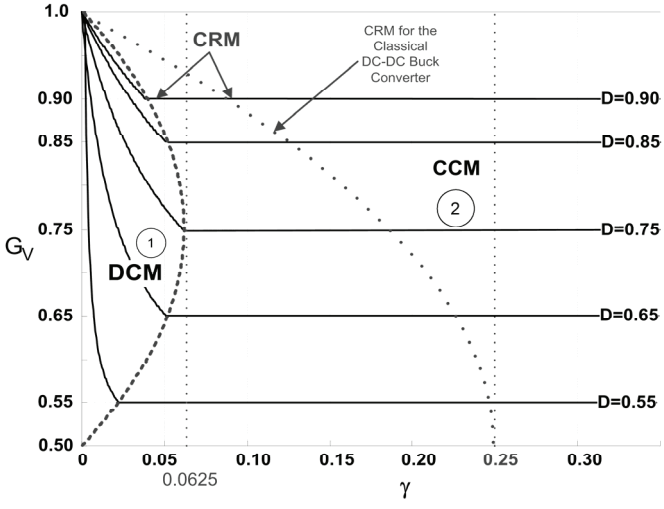


Fig. 7. Comparison between static gain curves of the classic approach and the 3SSC-based buck converter in OM.

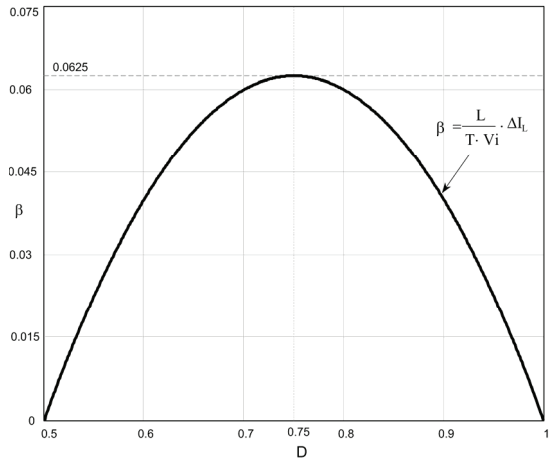


Fig. 8. Ripple current through the inductor in OM.

For the maximum ripple current, the inductance can be obtained by:

$$L = \frac{T_s \cdot V_i}{16 \cdot \Delta I_L} \quad (8)$$

The critical inductance, whose value assures operation in CCM, is given by:

$$L_{crit} = \frac{V_i \cdot T_s}{32 \cdot I_o} \quad (9)$$

The output capacitor can be determined as:

$$C \geq \frac{1}{2} \cdot \frac{I_o \cdot (2 \cdot D - 1)}{\Delta V_o \cdot f_s} \quad (10)$$

III. DESIGN PROCEDURE

A design example for the 3SSC buck converter in OM is presented as follows. The specifications are listed in TABLE I and were used in the implementation of an experimental prototype. Some important calculations are performed in order to show the loss mechanism. It is also worth to mention that both conduction and commutation losses are estimated under rated load condition.

A. Preliminary Calculation

Considering the operation in CCM, the static gain is:

$$G = D = \frac{150}{200} = 0.75 \quad (11)$$

The output current is:

$$I_o = \frac{P_o}{V_o} = \frac{1000}{60} = 6.667 \text{ A} \quad (12)$$

TABLE I
Design specifications

Parameter	Value
Input voltage	V_i=200 V
Inductor current ripple (20% of the input current)	ΔI_L=3.33 A
Switching frequency	f_s=30 kHz
Rated output power	P_o=1 kW
Output voltage	V_o=150 V
Output voltage ripple	ΔV_o=1.5 V

B. Inductor

The inductance is given by (7) as:

$$L=\frac{(2\cdot 0.75-1)\cdot(1-0.75)\cdot 33.33\cdot 10^{-6}\cdot 200}{2\cdot 3.33}=125\ \mu\text{H} \quad (13)$$

The rms and peak currents through the inductor are given by (14) and (15), respectively

$$I_{L(rms)}=\sqrt{\frac{2}{T_s}\cdot\int_0^{\frac{T_s\cdot(2\cdot D-1)}{2}}\left[I_m+\frac{V_i\cdot(1-D)\cdot t}{L}\right]^2 dt+\frac{2}{T_s}\cdot\int_0^{(1-D)\cdot T_s}\left[I_M-\frac{V_i\cdot(2\cdot D-1)\cdot t}{2\cdot L}\right]^2 dt} \quad (14)$$

$$I_{L(rms)}=6.74\ \text{A}$$

$$I_{L(pk)}=I_o+\frac{V_i\cdot(1-D)\cdot T_s\cdot(2\cdot D-1)}{4\cdot L_b}=8.33\ \text{A} \quad (15)$$

The core can be obtained according to the following expression:

$$A_e\cdot A_w=\frac{L\cdot I_{L(rms)}\cdot I_{L(pk)}\cdot 10^4}{k_w\cdot J_{\max}\cdot B_{\max}}=0.836\ \text{cm}^4 \quad (16)$$

where A_e is the effective core area, A_w is the window area, k_w=0.7 is the utilization factor of the window, J_{max}=400 A/cm^2 is the maximum current density, and B_{max}=0.3 T is the maximum variation of the magnetic flux. Considering the value given by (16), core NEE 42/20/21 manufactured by Thornton is chosen.

The core loss in the inductor can be obtained from:

$$P_{Lb(core)}=\Delta B^{2.4}\cdot\left(K_H\cdot f_L+K_E\cdot f_L^{\,2}\right)\cdot V_e=1.004\ \text{W} \quad (17)$$

where ΔB=0.04 is the magnetic flux variation, K_H=4·10^{-5} is the hysteresis loss coefficient, f_L=2·f_s=60 kHz is the operating frequency of the inductor, K_E=4·10^{-10} is the eddy-current loss coefficient, and V_e=42.5 cm^3 is the core volume [22, 23].

The copper loss in the inductor is given by:

$$P_{Lb(copper)}=\frac{\rho\cdot l_L\cdot N_L\cdot I_{L(rms)}^{\,2}}{n_L\cdot S_f}=0.909\ \text{W} \quad (18)$$

where ρ=2.078·10^{-6} Ω·m is the copper resistivity @70 °C; l_L=11.6 cm is the average length of one turn; N_L=15 is the number of turns of the inductor; n_L=7 is the number of wires in parallel; S_f=0.0025782 cm is the cross section area of copper wire AWG23.

C. Autotransformer

The active power processed by the high frequency autotransformer can be obtained similarly to that processed by its low frequency counterpart, as demonstrated in [13]. Besides, it has been shown that it corresponds to half of the total output power.

The autotransformer can be designed analogously to that of a full-bridge converter, while the following expression is valid:

$$A_e\cdot A_w=\frac{\frac{P_o}{2}}{k_t\cdot k_u\cdot k_p\cdot J_{\max}\cdot\Delta B_{\max}\cdot(2\cdot f_s)}\cdot 10^4=1.74\ \text{cm}^4 \quad (19)$$

where:

A_e is the effective core area, A_w is the window area, k_t=1 is the topology factor, k_u=0.4 utilization factor of the window, k_p=0.41 is the utilization factor of the primary winding, J_{max}=400 A/cm^2 is the maximum current density (typical value), and ΔB_{max}=0.3 T is the maximum variation of the magnetic flux for a ferrite core. Considering the value given by (19), core NEE 42/20/21 manufactured by Thornton is chosen.

The leakage inductance of the autotransformer is quite small and rated at the order of some microhenries for the specifications in TABLE I, what is also verified in several topologies based on the 3SSC reported in literature that use NEE ferrite cores [14] [19] [24]. The aforementioned works have also shown that such parasitic element is not supposed to influence the converter operation significantly. The windings are symmetrically displaced in the core i.e. with the same number of turns and parallel-connected wires. The autotransformer is designed according to guidelines used in conventional high frequency counterparts, with the same typical values used to represent the magnetizing inductance. The currents through the windings are balanced and the number of turns does not compromise the converter efficiency significantly. It is important to mention that if the magnetizing inductance of the autotransformer is small enough, then there would be an operation mode where the currents of the windings would be discontinuous.

The maximum voltage across the windings is:

$$V_{T1}=\frac{V_i}{2}=100\ \text{V} \quad (20)$$

The rms and peak currents through transformer T_1 are given by (21) and (22), respectively.

$$I_{T(rms)}=\sqrt{\frac{2}{T_s}\cdot\int_0^{\frac{T_s\cdot(2\cdot D-1)}{2}}\left(\frac{I_m}{2}+\frac{V_i\cdot(1-D)\cdot t}{2\cdot L}\right)^2 dt+\frac{2}{T_s}\cdot\int_0^{\frac{(1-D)\cdot T_s}{2}}\left(\frac{I_M}{2}+\frac{V_i\cdot(2\cdot D-1)\cdot t}{4\cdot L_b}\right)^2 dt} \quad (21)$$

$$I_{T(rms)}=3.37\ \text{A}$$

$$I_{T(pk)}=\frac{I_o}{2}+\frac{V_i\cdot(1-D)\cdot T_s\cdot(2\cdot D-1)}{8\cdot L}=4.16\ \text{A} \quad (22)$$

The core loss in the autotransformer can be obtained from:

$$P_{T(core)}=\Delta B^{2.4}\cdot\left(K_H\cdot f_T+K_E\cdot f_T^{\,2}\right)\cdot V_e=1.719\ \text{W} \quad (23)$$

where ΔB=0.15 is the magnetic flux variation; K_H=4·10^{-5} is the hysteresis loss coefficient; f_T=2·f_s=60 kHz is the operating frequency of the transformer; K_E=4·10^{-10} is the eddy-current loss coefficient; and V_e=42.5 cm^3 is the core volume.

The copper loss in the windings of the transformer is given by:

$$P_{T(copper)}=\frac{2\cdot\rho\cdot l_T\cdot N_T\cdot I_{T(rms)}^{\,2}}{n_T\cdot S_f}=0.317\ \text{W} \quad (24)$$

where ρ=2.078·10^{-6} Ω·m is the copper resistivity @70 °C; l_T=11.6 cm is the average length of one turn; N_T=12 is the number of turns of the 1:1 autotransformer; n_T=2 is the number of wires in parallel; S_f=0.005176 cm is the cross section area of copper wire AWG20.

D. Main Switches

The threshold voltage across one main switch is:

$$V_{S1} = V_i = 200 \text{ V} \tag{25}$$

The average current $I_{SI(avg)}$ and the rms current $I_{SI(rms)}$ through the switch are given by (26) and (27), respectively.

$$I_{S1(avg)} = \frac{2}{T_s}\cdot\int_0^{\frac{T_s\cdot(2\cdot D-1)}{2}}\left(\frac{I_m}{2}+\frac{V1\cdot(1-D)\cdot t}{2\cdot L}\right)dt + \frac{1}{T}\cdot\int_0^{(1-D)\cdot T_s}\left(\frac{I_M}{2}-\frac{V_i\cdot(1-2\cdot D)\cdot t}{4\cdot L}\right)dt = 2.916\,\text{A} \tag{26}$$

$$I_{S1(rms)} = \sqrt{\frac{2}{T_s}\cdot\int_0^{\frac{T_s\cdot(2\cdot D-1)}{2}}\left(\frac{I_m}{2}+\frac{V_i\cdot(1-D)\cdot t}{2\cdot L}\right)^2 dt + \frac{1}{T_s}\cdot\int_0^{(1-D)\cdot T_s}\left(\frac{I_M}{2}-\frac{V_i\cdot(2\cdot D-1)\cdot t}{4\cdot L}\right)^2 dt} \tag{27}$$

$$I_{S1(rms)} = 2.92 \text{ A}$$

MOSFET 5015VBR manufactured by APT was then chosen as the main switch, whose characteristics are: drain to source voltage V_{DS}=500 V; diode forward voltage $V_{S(F)}$=1.3 V; drain current I_D=32 A; on resistance $R_{DS(on)}$=0.15 Ω; rise time t_r=14 ns; fall time t_f=11 ns.

The conduction loss regarding each main switch is:

$$P_{S1(cond.)} = V_{S1(F)}\cdot I_{S1(avg)} + R_{DS(on)}\cdot {I_{S1(rms)}}^2 = 5.067 \text{ W} \tag{28}$$

The switching loss during turn on and turn off for a single switch is:

$$P_{S1(sw.)} = \frac{f_s}{2}\cdot(t_r + t_f)\cdot I_{S1(avg)}\cdot V_{S1} = 0.219 \text{ W} \tag{29}$$

E. Main Diodes

The reverse voltage across one diode is:

$$V_{D1} = V_i = 200 \text{ V} \tag{30}$$

The average current $I_{D1(avg)}$ and the rms current $I_{D1(rms)}$ through the diode are given by (31) and (32), respectively.

$$I_{D1(avg)}\,\frac{1}{T_s}\cdot\int_0^{(1-D)\cdot T_s}\left(\frac{I_M}{2}-\frac{V_i\cdot(2\cdot D-1)\cdot t}{4\cdot L}\right)dt = 0.83 \text{ A} \tag{31}$$

$$I_{D1(rms)} = \sqrt{\frac{1}{T_s}\cdot\int_0^{(1-D)\cdot T_s}\left[\frac{I_M}{2}-\frac{V_i\cdot(2\cdot D-1)\cdot t}{4\cdot L}\right]^2 dt} = 1.684 \text{ A} \tag{32}$$

Ultrafast diode RHRP840 was then chosen, whose characteristics are: reverse voltage $V_{D(rev.)}$=400 V; forward voltage $V_{D(F)}$=1.7 V; average forward current I_F=8 A; reverse recovery time t_{rr}=30 ns.

Estimating the intrinsic resistance of the diode from the curves given in the datasheet as R_D=50 mΩ, conduction loss regarding each diode becomes:

$$P_{D1} = V_{D1(F)}\cdot I_{D1(avg)} + R_{D1}\cdot {I_{D1(rms)}}^2 = 1.118 \text{ W} \tag{33}$$

Switching losses regarding the diodes are given as:

$$P_{S1(sw.)} = \frac{1}{2}\left(V_{D(F)P} - V_{D(F)}\right)\cdot I_{D1(avg)}\cdot t_{rise}\cdot f_s + V_{D1}\cdot Q_{rr}\cdot f_s = 0.336 \text{ W} \tag{34}$$

where $V_{D(F)P}$=2.1 V is the maximum value assumed by the forward voltage, t_{rise}=18 ns is the rise time of the current through the diode, and Q_{rr}=56 nC is the amount of charge stored in the intrinsic capacitance of the diode.

F. Comparison with Other Similar Approaches

The work presented in [19] presented an extensive comparison of the topology shown in Figure 1 with the classical and the interleaved buck converters. The 3SSC-based buck converter presents improved performance over the entire load range. Besides, current sharing between the semiconductors is maintained by the autotransformer, making this topology attractive for high-power high-current applications.

As it was mentioned before, the converter studied in [19] is the only structure found in literature that uses the 3SSC and is adequate for step-down operation. A brief comparison with similar topologies is presented as follows.

The so-called double-frequency buck converter is studied in [25], where two cells operating at low and high frequencies are used. The proposal is similar to the interleaved buck converter, but the circulating current problem is eliminated at the cost of a third active switch [25] [26].

An interleaved coupled-buck converter (ICBC) with active clamping is proposed in [27]. The static gain of the structure allows wider conversion ratios than that achieved by the classical buck converter. However, operation is restricted to D<0.5. Besides, there is high component count and the voltage stress across the power switches is increased due to the active clamping circuits. Consequently, the cost is significantly raised.

An ICBC with passive-clamp circuits is also proposed in [28] to further improve the conversion ratio. However, component count is also of major concern, with consequent increase of complexity, cost, and losses involving the elements such as switches, diodes, and inductors.

IV. EXPERIMENTAL RESULTS

According to the design procedure developed in the last section for the proposed 3SSC buck converter, which is supposed to operate in OM, an experimental prototype was implemented. The structure operating in open loop is shown in Figure 9.

Figure 10 shows the voltages across diodes D_1 and D_2, the current though diode D_1 and the current though switch S_2, where it can be seen that the aforementioned waveforms are in perfect accordance with the theoretical analysis. It is worth to mention that voltage and current stresses for diode D_1 are the same ones for D_2. It can be observed that diode D_2 is reverse biased when switch S_2 is turned on.

Figure 11 presents the voltages across switches S_1 and S_2, as well as the currents though diodes D_1 and D_2. When switch S_1 is turned off, diode D_1 is forward biased, what also happens to S_2 and D_2.

Figure 12 shows the voltages across switches S_1 and S_2, as well as the currents through inductor L and switch S_1. It becomes evident that the switching frequency is half of the ripple current frequency, what leads to the reduction of magnetic elements.

Figure 13 represents the output voltage, the input current, and the current through the filter inductor. The input current is continuous and the ripple current is reduced. It does not

happen with the classical buck converter, where the input current is discontinuous. This a prominent advantage over the traditional step-down topology, while the eventual use of an input filter inductor in this case may lead to reduced volume.

Figure 14 presents the variation of the static gain plotted as a function of the output current. Experimental results seem to be very close to those predicted in the theoretical analysis.

The experimental prototype was evaluated over a wide load range and the efficiency curve of the converter operating at 30 kHz is presented in Figure 15. The rated duty cycle is maintained in this case, while the load resistance is varied. The efficiency is about 98% over the entire load range, thus demonstrating the merit of the proposed converter. This is not observed in typical buck topologies that are not based on the 3SSC. Energy transfer from the source to the load occurs during almost the entire switching period for the 3SSC topology. On the other hand, in the conventional buck converter, it does only occur during part of the switching period, namely when the main switch is off and the output capacitor is charged. It certainly contributes for the reduction of the current peak in the switches causing efficiency to increase.

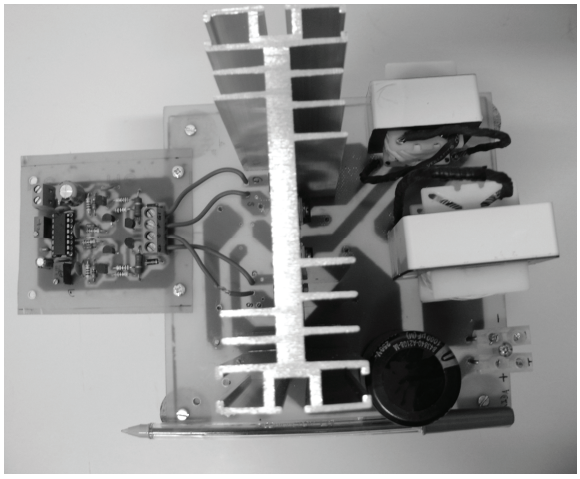


Fig. 9. Experimental prototype.

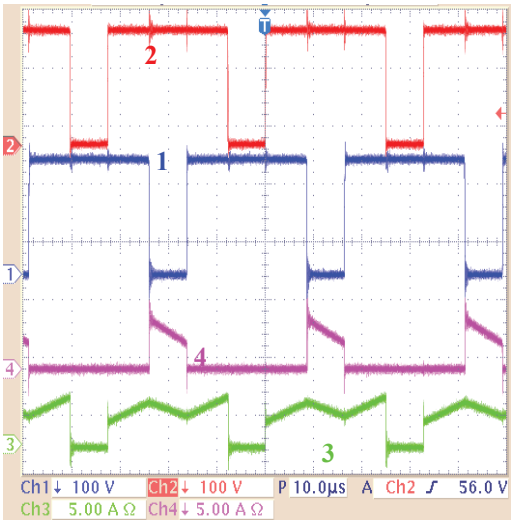


Fig. 10. Voltages across diodes D_1 (CH1) and D_2 (CH2), current though diodes D_1 (CH4), and current though switch S_2 (CH3).

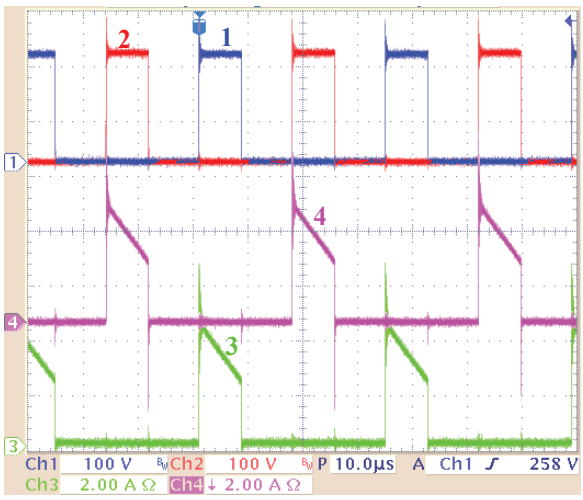


Fig. 11. Voltages across switches S_1 (CH1) and S_2 (CH2) and currents though diodes D_1 (CH4) and D_2 (CH3).

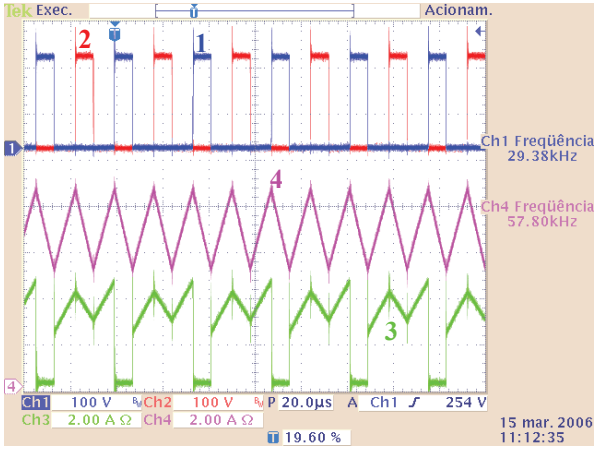


Fig. 12. Voltages across switches S_1 (CH1) and S_2 (CH2), current through inductor L (CH4), and current through switch S_1 (CH3).

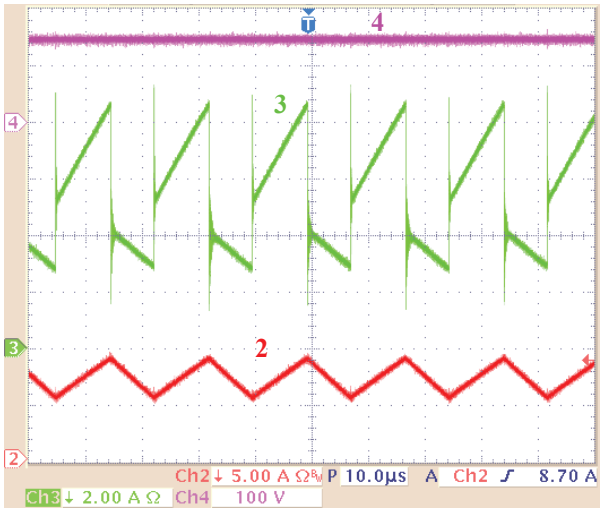


Fig. 13. Output voltage (CH4), the input current (CH3), and current through the inductor (CH2).

Besides, efficiency in this case (OM – D>0.5) is expected to be higher than that obtained for the converter operating in NOM (D<0.5) [19], mainly because energy is processed by the main switches simultaneously with the inductor charge, as it was presented in the theoretical analysis.

Of course, if all the converter's specifications mentioned in TABLE I are maintained constant, except for the output voltage, which is supposed to increase tending to the input voltage value, the current stresses through the switches are reduced. By comparing the efficiency curves in Figure 15 and [19], it is reasonable to assume that the 3SSC-based buck converter is an interesting choice for low conversion rates i.e. when D>0.5.

V. CONCLUSION

A dc-dc buck converter based on the 3SSC operating in OM has been presented in this paper. When the 3SSC is employed, the load current is distributed among the semiconductors. Furthermore, only part of the energy from the input source flows through the active switches, while the remaining part is directly transferred to the load without being processed by these switches, i.e. this energy is delivered to the load through passive components, such as the diodes and the transformer windings.

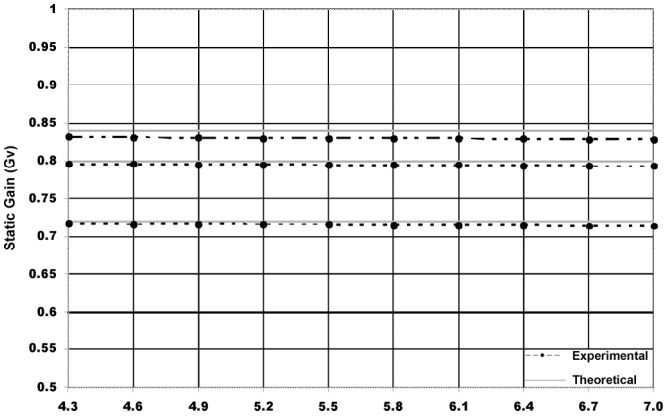


Fig. 14. Static gain as a function of the output current.

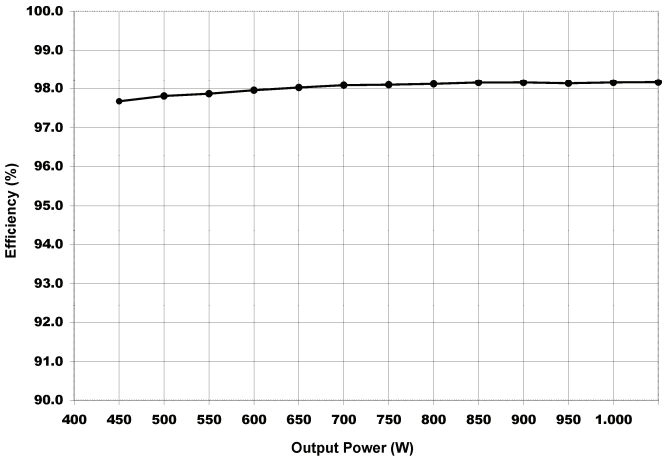


Fig. 15. Efficiency as a function of the output power.

Despite the increase in the number of semiconductors, the current levels on these devices are reduced, enabling the use of inexpensive switches and simplified command circuits because the isolated drive is not required like in the interleaved buck converter. In front of these characteristics, its use is recommended for high-power high-current applications the where traditional approach may be inadequate, while good current sharing is achieved.

The use of low side switches in the 3SSC-based buck converter may bring some complexity to the closed loop operation because there is no common ground for the input and output sides. High-side switches can be used as an alternative in this case considering the bilateral inversion proposed in [13].

In addition, the overall losses are distributed among all semiconductors, reducing the heat sink efforts. The reactive components operate with twice the switching frequency, with significant reduction in weight and volume of such components.

Considering the operation in OM (D>0.5) and the same ratings, the following characteristics can be addressed to the 3SSC-based converter if compared with the conventional buck topology:
- increased number of semiconductor elements;
- the operating area in CCM is wider;
- the ripple current through the inductor is reduced, as well as the currents through the switches;
- reactive elements are designed for twice the switching frequency, causing the required critical inductance to be smaller, for instance;

Besides, an important advantage of the proposed converter operating in OM (D>0.5) is the continuous nature of the input current, which is inherently discontinuous in the conventional buck converter, what may lead to the use of an input filter in some applications.

The main contribution of this work can be stated as the thorough analysis of the 3SSC-buck converter in OM, which was previously proposed in [19] and studied in terms of the operation in NOM. The study of the topology in OM leads to a novel analysis considering the quantitative and qualitative studies, design procedure, and experimental implementation that validates the concept of the 3SSC as a prominent solution for high-power high-current applications.

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REFERENCES

[1] M. Berkhout L. Dooper, "Class-D Audio Amplifiers in Mobile Applications", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 5, pp. 992–1002, May 2010.

[2] E. K. Sato, M. Kinoshita, Y. Yamamoto, T. Amboh, "Redundant high-Density High-Efficiency Double-Conversion Uninterruptible Power System", *IEEE Transactions on Industry. Applications.*, vol. 46, no. 4, pp. 1525–1533, July-August. 2010.

[3] S. V. Araujo, R. P. Torrico-Bascopé, G. V. Torrico-Bascopé, "Highly Efficient High Step-Up Converter For Fuel-Cell Power Processing Based on Three-State Commutation Cell", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 6, pp. 1987–1997, June 2010.

[4] Z. Amjadi S. S. Williamson, "Power-Electronics-Based Solutions for Plug-In Hybrid Electric Vehicle Energy Storage and Management Systems", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 608–616, February 2010.

[5] G. Yao, Y. Shen, W. Li, X. He, "A New Soft Switching Snubber for The Interleaved Boost Converters", in *Proc. 35th Annual IEEE Power Electronics Specialists Conference*, 2004, pp. 3765–3769.

[6] I. Matsuura, K. M. Smith Jr., K. M. Smedley, "A Comparison of Active and Passive Switching Methods For PWM Converters", in *Proc. 29th Annual IEEE Power Electronics Specialists Conference*, 1998, vol. 1, pp. 94–100.

[7] G. Hua, F. C. Lee, "Soft-Switching Techniques in PWM Converters", *IEEE Transactions on Industrial Electronics*, vol. 42, no. 6, pp. 595–603, December 1995.

[8] K. Fujiwara, H. Nomura, "A Novel Lossless Passive Snubber for Soft-Switching Boost-Type Converters", *IEEE Transactions on Power Electronics*, vol. 14, no. 6, pp. 1065–1069, November 1999.

[9] D. S. Oliveira Jr., C. E. A. Silva, R. P. Torrico-Bascopé, F. L. Tofoli, C. A. Bissochi Jr., J. B. Vieira Jr., V. J. Farias, L. C. de Freitas, "Analysis, Design, and Experimentation of A Double Forward Converter with Soft Switching Characteristics for All Switches", *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2137–2148, August 2011.

[10] J. P. Rodrigues, S. A. Mussa, M. L. Heldwein, A. J. Perin, "Three-Level ZVS Active Clamping PWM for the DC–DC Buck Converter", *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2249–2258, August 2009.

[11] Y. Jang, M. M. Jovanovic, "Interleaved Boost Converter With Intrinsic Voltage-Doubler Characteristic for Universal-Line PFC Front End", *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1394–1401, July 2007.

[12] D. J. Perreault, J. G. Kassakian, "Distributed Interleaving of Paralleled Power Converters", *IEEE Transactions on Circuits and Systems I: Fundamental Theory Application*, vol. 44, no. 8, pp. 728–734, August 1997.

[13] G. V. Torrico-Bascopé, I. Barbi, "Generation of A Family of Non-Isolated DC-DC PWM Converters Using New Three-State Switching Cell", in Proc. *IEEE Power Electronics Specialists Conference*, 2000, vol. 2, pp. 858–863.

[14] S. V. Araujo, R. P. Torrico-Bascopé, G. V. Torrico-Bascopé, L. Menezes, "Step-up Converter with High Voltage Gain Employing Three-State Switching Cell and Voltage Multiplier", in *Proc. Power Electronics Specialists Conference*, 2008, pp. 2271–2277.

[15] R. A. da Camara, C. M. T. Cruz, R. P. Torrico-Bascopé, "Boost Based on Three-State Switching Cell for UPS Applications", in *Proc. Brazilian Power Electronics Conference*, 2009, pp. 313–318.

[16] G. V. Torrico-Bascopé, R. P. Torrico-Bascopé, D. S. Oliveira Jr., S. V. Araújo, F. L. M. Antunes, C. G. C. Branco, "A Generalized High Voltage Gain Boost Converter Based on Three-State Switching Cell", in *Proc. IEEE International Symposium on Industrial Electronics*, 2006, pp. 1927–1932.

[17] G. V. Torrico- Bascopé, R. P. Torrico- Bascopé, D. S. Oliveira Jr., S. V. Araújo, F. L. M. Antunes, C. G. C. Branco, "A High Step-Up Converter Based on Three-State Switching Cell", in *Proc. IEEE International Symposium on Industrial Electronics*, 2006, pp. 998–1003.

[18] R. P. Torrico-Bascopé, C. G. C. Branco, G. V. Torrico-Bascopé, C. M. T. Cruz, F. A. A. de Souza, L. H. S. C. Barreto, "A New Isolated DC-DC Boost Converter Using Three-State Switching Cell", in *Proc. Applied Power Electronics Conference and Exposition*, 2008, pp. 607–613.

[19] J. P. R. Balestero, F. L. Tofoli, G. V. Torrico-Bascopé, F. J. M. de Seixas, "A DC–DC Converter Based On The Three-State Switching Cell for High Current and Voltage Step-Down Applications", *IEEE Transactions on Power Electronics*, vol. 28 , no. 1, pp. 398–407, January 2013.

[20] E. E. Landsman, "A Unifying Derivation of Switching Regulator Topologies," in *Proc. IEEE Power Electronics Specialists Conference*, 1979, pp. 239–243.

[21] J. P. R. Balestero, F. L. Tofoli, R. C. Fernandes, G. V. Torrico-Bascopé, and F. J. M. Seixas "Power Factor Correction Boost Converter Based on The Three-State Switching Cell", *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1565–1577, March 2012.

[22] UNITRODE. "Switching Regulated Power Supply Design Seminar Manual", *SEM900*. 1993, pp. M6-1 – M6-0.

[23] Barbi, I. Projeto de Fontes Chaveadas. *Edição do autor*, Florianópolis, 2001.

[24] F. L. Tofoli, D. S. Oliveira, Jr., R. P. Torrico-Bascopé, Y. J. A. Alcazar, "Novel Nonisolated High-Voltage Gain DC–DC Converters Based on 3SSC and VMC," *IEEE Transactions on Power Electronics*, vol. 27 , no. 9, pp. 3897–3907.

[25] Xiong Du, Luowei Zhou, Heng-Ming Tai, "Double-Frequency Buck Converter", *IEEE Transactions on Industrial Electronics*, vol. 56, no. 5, pp. 1690–1698, May 2009.

[26] Z. Ye, P. K. Jain, and P. C. Sen, "Circulating Current Minimization in High-Frequency AC Power Distribution Architecture with Multiple Inverter Modules Operated in Parallel," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2673–2687, October 2007.

[27] Cheng-Tao Tsai and Chih-Lung Shen, "Interleaved Soft-Switching Coupled-Buck Converter with Active-Clamp Circuits", in *Proc. International Conference on Power Electronics and Drive Systems*, 2009, pp. 1113–1118.

[28] Cheng-Tao Tsai, Chih-Lung Shen, Jyh-Chau Su, Ying-Che Kuo, "Analysis and Implementation of an Interleaved ZVS Buck Converter with Coupled-Inductors," in *Proc. 6th IEEE Conference on Industrial Electronics and Applications (ICIEA),* 2011, pp. 1392–1397.

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