A NOVEL SINGLE-SWITCH HIGH POWER FACTOR LED DRIVER TOPOLOGY WITH HIGH-FREQUENCY PWM DIMMING CAPABILITY

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***Abstract* – In this work, a novel off-line converter with power factor correction (PFC) and pulse-width modulated (PWM) dimming function employing a single active power switch is proposed for LED lighting. The proposed converter is a slightly modified flyback topology which enables the main switch to be used both for power factor correction and PWM high-frequency dimming with a constant peak on the current through the LEDs, thus conserving chromatic characteristics of emitted light. The proposed control scheme uses duty-cycle to control the light level, while switching frequency is varied along to adjust the input power and keep a constant LED peak current. The converter is able to dim LEDs without losing its PFC characteristics. Mathematical description and experimental results of a prototype with 100 W of peak power fed from 127 V mains voltage are presented in this paper to show feasibility of the novel single-switch driver proposal.**

***Keywords* – LED Dimming, Off-line LED Drivers, Power Factor Correction, Single-switch LED Driver.**

I. INTRODUCTION

Though fairly recent, lighting systems based on light-emitting diode (LED) technology are rapidly becoming popular; indeed, recent works address various LED lighting applications [1], [2]. Promises of high luminous efficacy, long life, good color rendering and high flexibility (easy dimming, small-sized sources) come along with the technology [3]-[5]. In this sense, one of the main engineering research interests for LED lighting is the driving of the devices, providing regulated current for the load and, when mandatory, power factor correction for the fixture. Advanced capabilities can be incorporated in the electronic driver if desired, such as light dimming and digital control, which can provide flexible means of reducing electrical power demand when the full light level is not needed or desired.

One of the best and most flexible ways of changing the light level in LED-based luminaires is to feed the LED array with a pulse width-modulated (PWM) current featuring a variable duty-cycle, so as to adjust the light level (i.e., vary the average current value while keeping a constant peak current value). This technique, often called PWM dimming, allows for chromatic stability of the emitted light, causing less color shift than amplitude dimming [6]-[8], and is thus employed in most dimming applications [9]-[17]. It also provides means to dim LEDs down to very low levels with the devices still emitting light, enhancing dimming dynamic range compared to amplitude modulation (AM) dimming.

Dimmable off-line LED drivers with power factor correction (PFC) are often implemented with multi-staged approaches: the PFC converter comprises the first switching stage, with the second switching stage being a current or power-controlling converter. These two stages could also be combined in an integrated (or single-stage) topology. The two-stage approach is shown in Fig. 1 (a), whereas an integrated approach is given in a generalized manner in Fig. 1 (b). The integration of stages allows for reduction in the number of static power switches (MOSFETs, IGBTs) as well as a reduction in control loops and switch-driving circuitry, being a very common alternative for implementing the so-called single-stage off-line LED drivers [13]-[16]. In cases where PWM dimming is desired, though, the use of a dedicated additional switch in series (or parallel, depending on converter output characteristics) with the LEDs is needed to perform the dimming action, as done in [14]-[16]. Thus, current approaches for PWM dimmable off-line LED drivers require the use of, at least, two power switches – one for power control (PC) and PFC (as in single-stage converters) and the other dedicated for the dimming function itself.

Proposing a dimmable single-switch LED driver with PFC is not trivial, since the only power switch available on the topology must perform the active role in current regulation, power factor correction and also PWM dimming. The main issue is to accomplish all those features by using only the few degrees of freedom imposed by a single-switch topology, while still being able to keep a constant peak current on the LED for the whole dimming range and not losing the PFC characteristics at diminishing light levels.

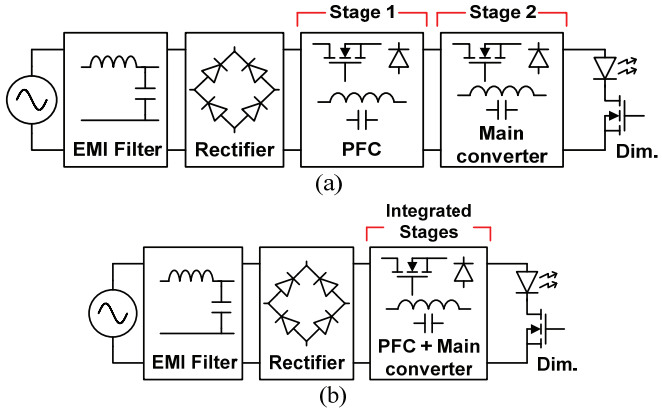

Fig. 1. Two common approaches for off-line LED drivers with PFC and dimming: (a) two-stage with series PWM dimming and (b) single-stage (integrated) with series PWM dimming. Both proposals employ a dedicated power switch solely for the PWM dimming operation.

Manuscript received on 25/10/2012. Revised on 08/01/2013. Accepted for publication in 08/01/2013 to Special Session by recommendation of the Associate Editors Pedro Francisco Donoso-García and Ricardo Nederson do Prado.

In some approaches for PWM dimming employing a dimming frequency much lower than the converter switching frequency (such as in enable dimming [11], [13] or burst-mode dimming [18]), the converter may lose the PFC characteristics because the dimming operation creates instantaneous power oscillations on the input which increase the total harmonic distortion (THD) of input current and lower the power factor (PF). An example of an integrated converter which loses PFC characteristics when dimming is enabled is given in [13]. One natural solution to overcome this issue is to adopt high-frequency series PWM dimming [16] rather than a low-frequency scheme, because of the slow dynamics of the PFC converter. At frequencies closer to the switching frequency, the switching of current (i.e., dimming) is effectively filtered out by the converter and does not create instantaneous power fluctuations at the input, which would otherwise lower the PF during normal dimming operation.

The challenge of proposing a novel single-switch topology with PWM dimming is addressed in this paper, by employing a modified flyback converter with a special variable frequency control law that is able to compensate for load changes during dimming operation, while keeping the peak current value constant. The high-frequency dimming approach is thus employed, in order to conserve the PFC characteristics of the converter for the whole dimming range. The restriction of employing only one active switch also obliges the use of high-frequency PWM for dimming.

II. DIMMING OF LEDS CONSIDERING LUMINOUS FLUX LINEARITY AND COLOR STABILITY

A brief discussion regarding the two mainstream techniques of LED dimming is done in this section, analyzing their implications on photometrical performance. These techniques are namely the PWM dimming and the AM dimming. A conceptual representation of both of these methods is given in Fig. 2. The first one uses a constant peak value and varies the duty-cycle of current, applying controlled pulses on the load, whereas the second one varies the peak value itself (which is equal the average in this case), without any pulse modulation strategy. Both of them are able to vary the average value, which is the keystone of dimming, but by different means.

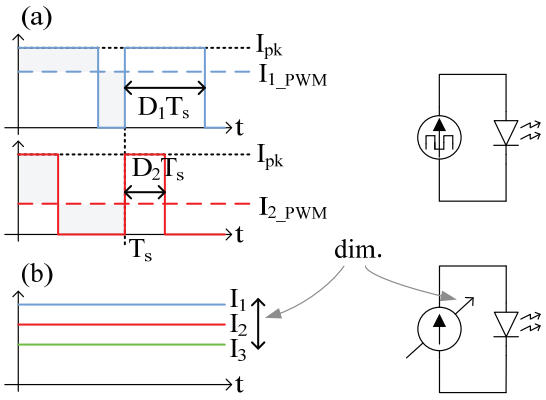

Fig. 2. Dimming of LEDs by means of (a) PWM and (b) AM. D_1 and D_2 are two different duty-cycles implying in current levels $I_{1\_PWM} = D_1.I_{pk}$ and $I_{2\_PWM} = D_2.I_{pk}$ for PWM dimming, whereas I_1, I_2 and I_3 are 3 different amplitude setpoint values for AM dimming.

To decide which of both techniques should be employed in an application requiring outstanding LED photometrical performance (e.g., where color stability or dimming linearity is of paramount importance, such as indoor lighting or display backlight), one can use photometrical measurements (flux and spectral data) of the LEDs under PWM and AM dimming for comparison. Such approach is shown in figures 3 and 4. These curves were obtained using an integrating sphere (1 m diameter) plus spectrophotometer, measuring a properly heatsinked LED (Osram LUW W5PM). In all curves the 100% level equals 1 A (average).

In Fig. 3, it is possible to see from the trend lines that PWM dimming implies in much less color shift for the whole dimming range, having a less steep slope in correlated color temperature (CCT) change than AM does.

Fig. 4 compares how the luminous flux per LED varies along the dimming range in each case. It is easy to see that PWM implies in a linear dimming action, whereas AM dimming has a non-linear behavior, though PWM implies in slightly reduced luminous efficacy for most of the dimming range (this is signaled by lower flux values in PWM for corresponding average current levels in AM).

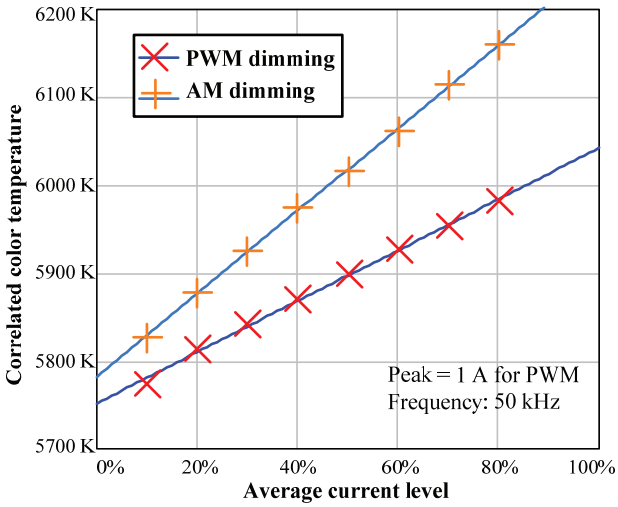

Fig. 3. Comparison of chromatic shifts under PWM and AM dimming based on correlated color temperature (CCT).

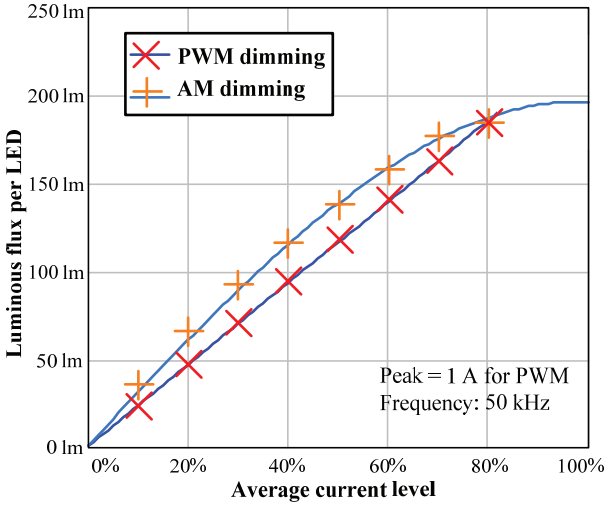

Fig. 4. Comparison between the linearity of PWM and AM dimming based on the luminous flux per LED.

The spectra of the LED under each current level (given in Fig. 5) also show the linearity of this approach (PWM dimming), since almost equal spacing between spectral distributions can be noticed between dimming steps.

From these data altogether, it can be concluded that, given its better linearity and chromaticity stability, PWM dimming is preferred, justifying the choice for proposing the novel PWM-dimmable off-line driver presented in this work.

III. PROPOSED TOPOLOGY AND ANALYSIS

The novel topology proposed for the off-line single-switch dimmable LED driver is based on a slight modification of the flyback converter (though it does not provide galvanic isolation). It is known that the flyback converter whenever operated in discontinuous conduction mode (DCM) provides inherent power factor regulation, because the input current follows the input voltage waveform, thus emulating a resistance for the power grid and providing close to unitary power factor [19], [20]. The derivation of the dimmable LED driver topology is done by taking a flyback single-stage PFC and sharing its power switch also for the dimming action, resulting in the topology presented in Fig. 6, where the switch M is not only employed to provide a current path for the primary of the flyback transformer in each switching cycle, but is also able to break the current applied to the LED array, with the same high frequency.

In Fig. 6, L_m is the magnetizing inductance of the flyback transformer seen from the primary. The transformer has a primary-secondary turns ratio of 1:n. capacitor C_o is large enough to yield negligible 120 Hz ripple which arises from off-line operation (given that line frequency is f_L = 60 Hz).

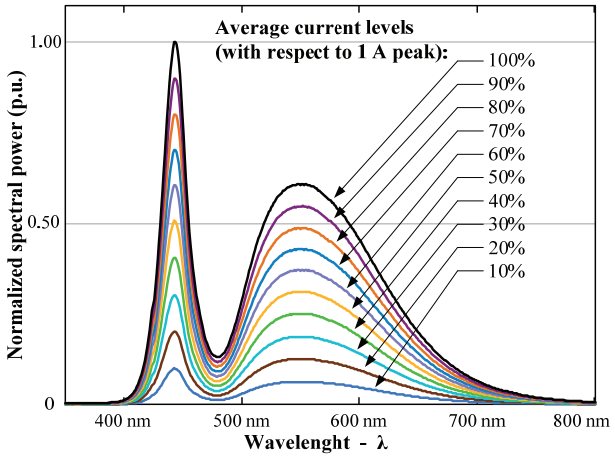

Fig. 5. Normalized spectra of an LED under PWM dimming.

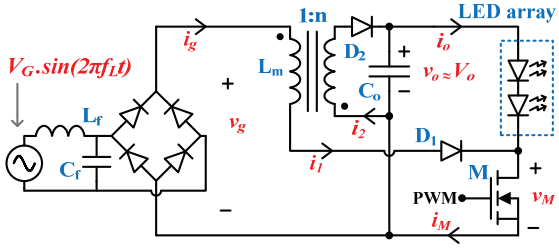

Fig. 6. Topology of the proposed single-switch PWM-dimmable off-line LED driver with power factor correction.

The input electromagnetic interference (EMI) filter (L_f and C_f) is only used to suppress switching current harmonics.

The use of one sole power switch to perform all functions of the converter implies in some design constraints (e.g., duty-cycle must be used to set the light level only, not regulating the output voltage or peak current) and also imprints an overcurrent stress on the switch (M), since it will handle both the flyback primary and output currents at the same time. Being operated in DCM for PFC realization (i.e., the magnetizing current in the flyback coupled inductors reaches zero at the end of every switching cycle, thus L_m discharges completely), the peak voltage stress on the switch will be the output voltage reflected at the primary plus the input voltage (peak of line voltage, V_G). The idealized steady-state waveforms seen in the converter at this peak voltage are given in Fig. 7.

For the analysis and design of the converter, the LED array static electrical model is used, which comprises a voltage source (threshold voltage, V_{th}) in series with a resistance (dynamic diode resistance, r_d) and an ideal diode. This model is also used in [10], [11], [13], [15] and [16], being enough for design purposes also in dimming applications. Given that the peak of current through the LEDs (I_{pk}) is a design constraint for a given LED array, the output voltage can be written as (1).

$$V_o = r_d I_{pk} + V_{th} \tag{1}$$

The constraint for the flyback to be operated in DCM is given by (2), where D_{crit} is the maximum (critical) allowed duty-cycle for given V_o (dependent on LED array) and V_G.

$$D_{crit} = \frac{V_o}{V_o + nV_G} \tag{2}$$

Equation (2) depends on the turns ratio n. Thus, n can be chosen in order to achieve a wide dimming range: when n is

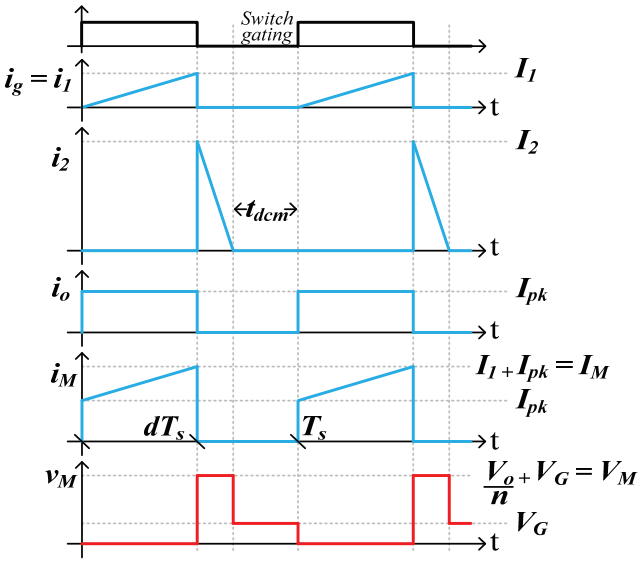

Fig. 7. Idealized waveforms for the converter operating in DCM at the peak of line voltage V_G. T_s is one switching period ($T_s = 1/f_s$).

small enough, D_{crit} is large enough so that dimming can extend from low duty-cycles up until high duty-cycles without losing DCM operation, hence the PFC characteristics of the converter. Care must be taken, though, since the voltage stress on the power switch increases with decreasing n (see Figure 7), thus there is a trade-off between voltage stress and dimming range.

One can then chose a maximum duty-cycle D_{max} below the limit imposed by (2), which will be considered the rated output current of the driver, i.e., the 100% light level, even though it is still a square current wave – this is because duty-cycle will not be allowed to rise above this level.

The equivalent resistance emulated by the DCM flyback on its input is given by (3), thus the input power drained by the converter is given by (4), where $f_s = 1/T_s$ is the switching frequency and d is the duty-cycle, both at a given operating point (d, f_s).

$$R_G(d, f_s) = \frac{2L_m f_s}{d^2} \tag{3}$$

$$P_{in}(d, f_s) = \frac{V_G^{\,2}}{4L_m f_s} d^2 \tag{4}$$

Equation (4) shows that when varying the operating duty-cycle of the converter to achieve different light levels, the power transferred from the input to the output by the converter varies along, proportional to the square of that variation. Were the converter operated at fixed frequency, the peak of output current would increase or decrease with duty-cycle changes; this is highly undesirable for the PWM dimming function, since it needs (and assumes) a constant peak current on the LEDs, varying the average value of i_o only by modulation of the current pulse width. One solution to keep a constant peak current on the output is to employ a frequency compensation control law, which changes the switching frequency whenever a duty-cycle dimming step is applied, in order to compensate the power drained and keep I_{pk} constant. Thus, in this converter, duty-cycle is used only to control the light level, while frequency is used to compensate for achieving a constant peak at output current. The average power delivered at the output is given by (5).

$$P_{out}(d) = V_o I_{pk} d \tag{5}$$

Considering some efficiency η and equaling (4) and (5), the frequency compensation control law (6) can be obtained.

$$f_s(d) = \frac{\eta V_G^{\,2}}{4L_m I_{pk}(V_{th} + I_{pk} r_d)} d \tag{6}$$

Equation (6) shows that the higher the duty-cycle (i.e., the light level), the higher the frequency needed to compensate for the input power change, keeping I_{pk} constant. The output power will then increase linearly with duty-cycle.

The design of the magnetizing inductance is done for the worst case scenario, i.e., the heaviest load current (highest duty-cycle, D_{max}), so that the converter will still operate in DCM even at D_{max}. Also at D_{max}, the frequency will be at its maximum, f_{s_max}, according to the compensation law (6). The parameter f_{s_max} can then be chosen *a priori* as an upper limit for switching frequency; L_m will be smaller for higher f_{s_max}. By isolating L_m from (6) applied to $d = D_{max}$ and $f_s = f_{s\_max}$, the upper limit for L_m is found to be given by (7). Any value equal or below will ensure DCM operation (since D_{max} was chosen below D_{crit}).

$$L_m \le \frac{\eta V_G^{\,2} D_{\max}}{4 f_{s\_\max} I_{pk}(V_{th} + r_d I_{pk})} \tag{7}$$

The output capacitor can be sized to yield negligible output voltage ripple, which is given by (8) for the heaviest load (at D_{max} and f_{s_max}). This voltage ripple results from the instantaneous input power oscillating at twice line frequency (120 Hz for a line frequency f_L = 60 Hz), thus it is a low-frequency ripple which implies in a low-frequency envelope on the output current, whose peak-to-peak amplitude will be given by (9).

$$\Delta V_o = \frac{D_{\max}^{\,2} V_G^{\,2}}{8\pi V_o L_m C_o f_L f_{s\_\max}} \tag{8}$$

$$\Delta I_{pk} = \frac{\Delta V_o}{r_d} \tag{9}$$

The peak current stresses on the diodes and power switch can be found to be given by (10), (11) and (12), with respect to the waveforms in Fig. 7. The peak voltage stress on the switch is given by (13), and is an important design parameter to be considered, as it will be shown in the next section.

$$I_1 = \frac{V_G}{L_m} \frac{D_{\max}}{f_{s\_\max}} \tag{10}$$

$$I_2 = \frac{I_1}{n} = \frac{V_G}{nL_m} \frac{D_{\max}}{f_{s\_\max}} \tag{11}$$

$$I_M = I_{pk} + I_1 = I_{pk} + \frac{V_G}{L_m} \frac{D_{\max}}{f_{s\_\max}} \tag{12}$$

$$V_M = V_G + \frac{V_o}{n} \tag{13}$$

IV. DESIGN EXAMPLE

The design procedure for the proposed high power factor single-switch dimmable LED driver is done for a given LED array to be driven (parameters r_d, V_{th}, I_{pk} are assumedly known) and for a given input line voltage (V_G). Transformer turns ratio (n) is chosen as low as possible to increase the dynamic range of dimming, according to (2), but also paying

attention to the increase in diode D_2 current stress (11) and, more importantly, the peak voltage stress on the power switch, (13). Then values for L_m and C_o can be found for given D_{max} and f_{s_max}.

For this design example, an LED array comprising 32 series-associated Lumileds Luxeon K2 Emitter (LXK2-PWC4-0200) high-power white LEDs fitted in a properly sized heatsink was chosen as the load. The parameters for the static electrical model were found to be r_d = 22 Ω and V_{th} = 88 V for this particular 32-LED array. The intended peak current for this design was chosen I_{pk} = 1 A. From (1), it is found that the output voltage will then be V_o = 110 V.

Line voltage was chosen 127 V (RMS), thus with peak voltage V_G = 180 V. Converter efficiency was estimated η = 80% for design purposes.

In order to choose the most adequate value for the transformer turns ratio n, one can plot both the critical duty-cycle (2) and peak switch voltage stress (13) against n and graphically select one optimal value in the voltage stress versus dimming dynamic range trade-off. This is done in Fig. 8, where the turns ratio was selected n = 0.177, yielding a voltage stress on the switch close to 801 V and a critical duty-cycle of 77.6%. This value ensures good dynamic range, since duty-cycle used for dimming can go even beyond 70% without the converter losing its inherent PFC characteristics (i.e., entering continuous conduction mode). Also, the voltage peak of 801 V is not so high that cannot be handled by a high-voltage power MOSFET or IGBT.

Since D_{crit} was found to be 0.776 for parameters n = 0.177, V_G = 180 V and V_o = 110 V, the designer can now choose D_{max} and f_{s_max}. A value of D_{max} = 0.7 was therefore chosen (thus d = 70% is for the maximum light level, yielding 700 mA of maximum average current with the constant 1 A peak). Maximum frequency, f_{s_max}, was chosen to be 49 kHz, in order to avoid using too high switching frequencies which could increase losses in the power switch.

From these values altogether, the design of the converter can be concluded by employing (7) to find that the value for the magnetizing inductance should be lower than 838 µH.

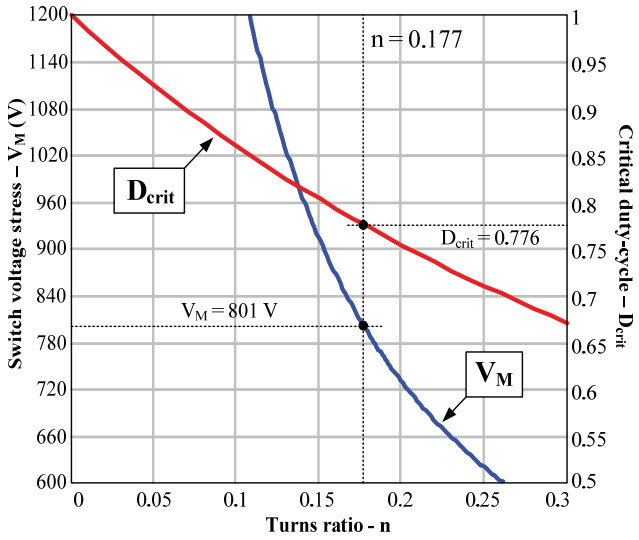

Fig. 8. Design curves for analyzing the peak switch voltage stress and the critical duty-cycle for the converter as functions of the flyback transformer turns ratio, for selecting the parameter n.

Thus an inductance L_m = 833 µH meets this constraint. Using (8) to size the output capacitor returns that a capacitance C_o = 470 µF will yield a small 4 V peak-to-peak voltage ripple on the output. A summary of this design example is given in Table I.

The switching frequency control law (6) for this particular design is plotted in Fig. 9, along with the output average current for every light level of the designed dimming range (from 20% to 70% duty-cycle).

V. EXPERIMENTAL RESULTS

A prototype of the high power factor single-switch dimmable LED driver designed in the previous section was built and tested. For this prototype, an input EMI filter was added to suppress switching harmonics, comprising L_f = 4 mH and C_f = 220 nF. The power switch M was chosen to be an IRG4PH20KD IGBT, only due to lab momentarily unavailability on MOSFETs rated at 800 V / 4.1 A, though a low resistance MOSFET could yield less conduction losses than an IGBT. D_1 diode is a MUR460 and D_2 is a MUR860.

TABLE I
Summary of the Parameters for the LED Driver

Part	Parameter value
LED array	r_d = 22 Ω V_{th} = 88 V I_{pk} = 1 A
Converter operation	f_{s_max} = 49 kHz (desired) D_{max} = 0.7 (desired) η = 80% (estimated)
Line voltage	V_G = 180 V (from 127 VRMS) f_L = 60 Hz
Flyback transformer	n = 0.177 (5.65 : 1 ratio) L_m = 833 µH
Dimming range	D_{max} = 0.7 @ fs = 49 kHz –700 mA, 100% dim. level D_{min} = 0.2 @ fs = 14 kHz – 200 mA, 28.5% dim. level
Output filter	C_o = 470 µF ΔV_o = 4 V (3.6%) ΔI_{pk} = 180 mA (18%)
Current and voltage stresses on switch/diodes	I_1 = 3.1 A I_2 = 17.4 A I_M = 4.1 A V_M = 801 V

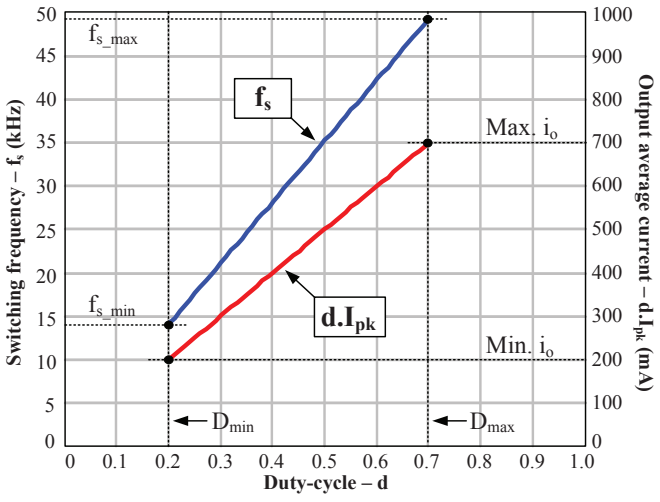

Fig. 9. Switching frequency and average LED current as functions of duty-cycle for the whole dimming range.

A blocking diode could also be added in series with the LED module, to eventually protect it from the primary flyback voltage appearing across the switch when it opens – this was done in this particular prototype for safety purposes.

A photo of the prototype plus the LED array employed in the dimmable LED system proposed is given in Fig. 10.

The prototype was triggered by using a gate driver integrated circuit, whose signal was fed from the PWM channel of a low-cost microcontroller. A selectable duty-cycle and frequency control program was implemented in an ATMEGA8 8-bit / 16 MHz microcontroller that receives a duty-cycle value and compensates the switching frequency to keep the peak of LED current stabilized around 1 A. The experimental waveforms are given in figures 11 to 13.

The output waveforms (Fig. 11 and Fig. 12) show the square current wave applied to the LED array.

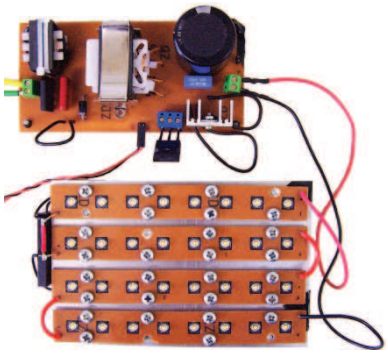

Fig. 10. Prototype of the high power factor single-switch LED driver with series PWM dimming, along with the 32-LED array.

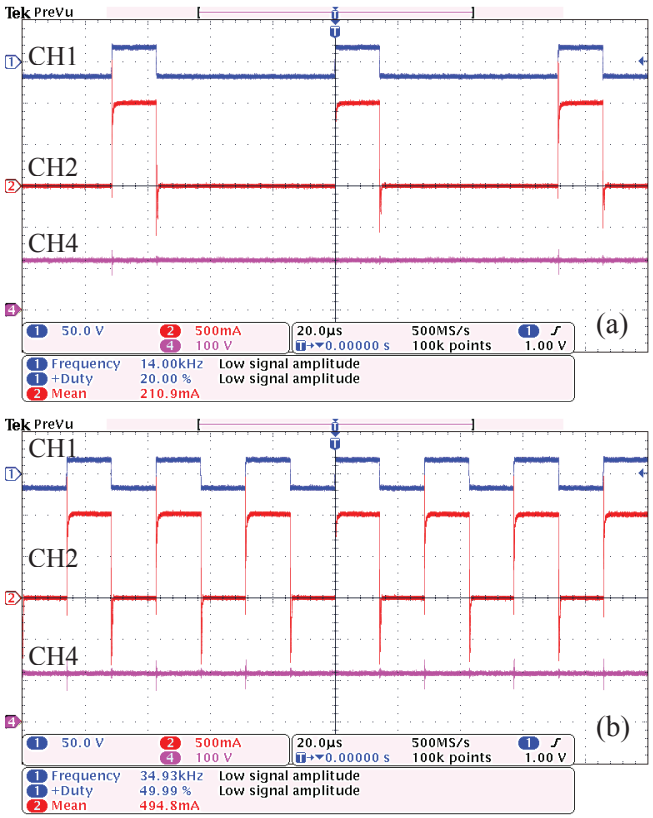

Fig. 11. Gating signal (CH1 – 50 V/div), LED current (CH2 – 500 mA/div) and output voltage (CH4 – 100 V/div) for two different light/average current levels: (a) 20% and (b) 50% duty-cycle. Time scale: 20 µs/div.

Several duty-cycles, varying from the lowest to the highest light levels, were tested, three of which are given in the aforementioned waveforms. The waveforms on the input of the converter are given in Fig. 13. They show high PF and low total harmonic distortion (THD) of input current, both for the lowest and highest light levels.

Figures 14 to 16 show all the experimental data, obtained from the prototype, organized by mean of graphs. The curves shown in Fig. 14 can easily be compared to the same theoretical curves from Fig. 9, showing good precision in the theoretical description given for the novel converter.

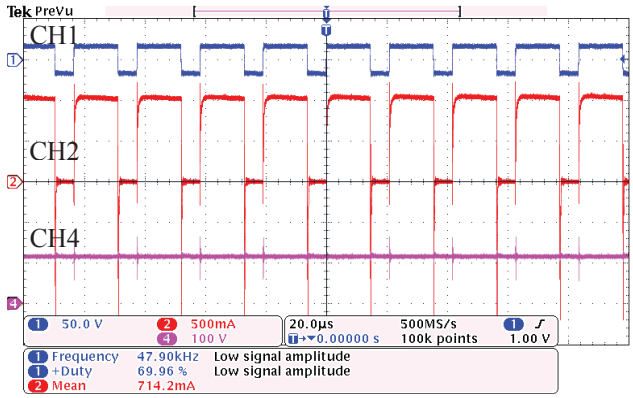

Fig. 12. Gating signal (CH1 – 50 V/div), LED array current (CH2 – 500 mA/div) and output voltage (CH4 – 100 V/div) at the maximum light level: 70% duty-cycle (considered here the 100% level of light emitted). Time scale: 20 µs/div.

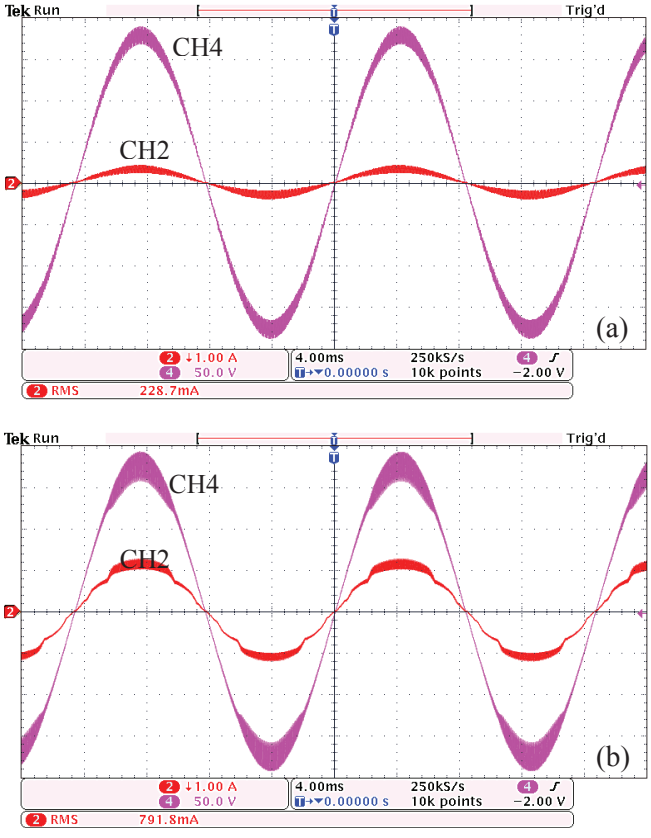

Fig. 13. Input voltage (CH4 – 50 V/div) and input current (CH2 – 1 A/div) at the converter for the two extreme levels possible for dimming: (a) at 20% duty-cycle (lightest load) and (b) at 70% duty-cycle (heaviest load). Time scale: 4 ms/div.

In Fig. 15, the power factor can be seen to be almost unitary for the whole dimming range, with very low input current THD, as expected and desired.

Fig. 16 shows that efficiency stands around 80% for the whole dimming range. This efficiency is not so high, but this is expected given the current and voltage stresses on the semiconductors, especially on the main power switch.

A dimming step on the control variables was also applied, changing both duty-cycle and frequency according to the control law (Fig. 14), in order to verify the dynamic response of the converter on its input and output. This step was applied from full load condition (70% duty-cycle, 700 mA) to the lowest light level considered (20% duty-cycle, 200 mA). The waveforms during the dimming step at the output and input of the converter are given in Fig. 17 and Fig. 18, respectively (the step is marked by an arrow in both waveforms).

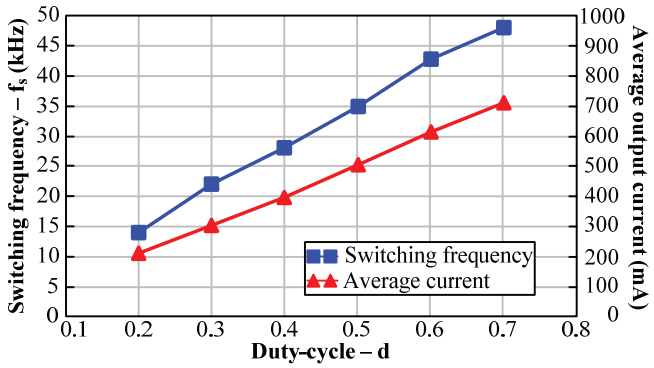

Fig. 14. Switching frequency and average output current as functions of duty-cycle for every light level measured.

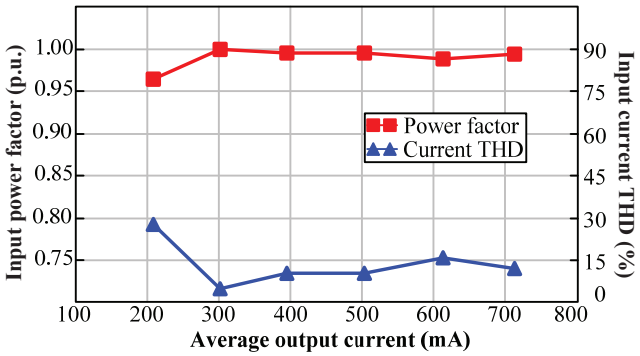

Fig. 15. Input power factor and input current THD as functions of the light level (represented by the absolute value of average output current on the horizontal axis).

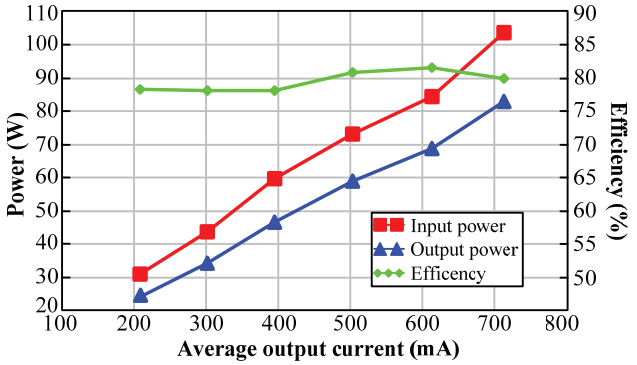

Fig. 16. Evolution of efficiency, input and output powers against average output current.

This was an open loop test, only to verify the change in input and output powers and the behavior of the peak of the output current (which was kept constant before and after the step, as desired for proper dimming operation).

Fig. 19 shows the current and voltage on the main power switch, at the peak of line voltage and at full load condition (maximum light level, at d = 70%). The current and voltages stresses also accord to the theoretical predictions.

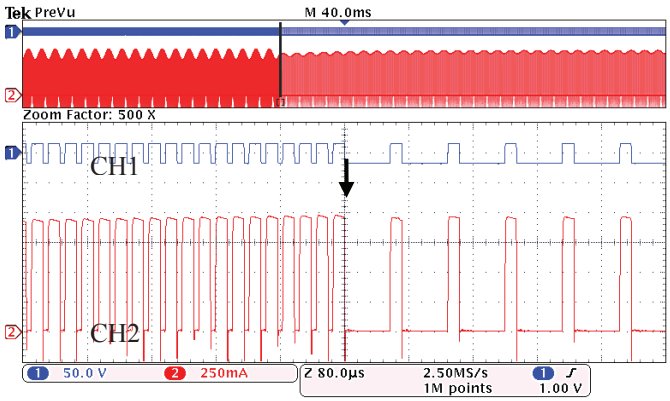

Fig. 17. Gating signal (CH1 – 50 V/div) and output current (CH2 – 250 mA/div) when a dimming step from full load to 20% duty-cycle is applied. Time scale: 80 µs/div.

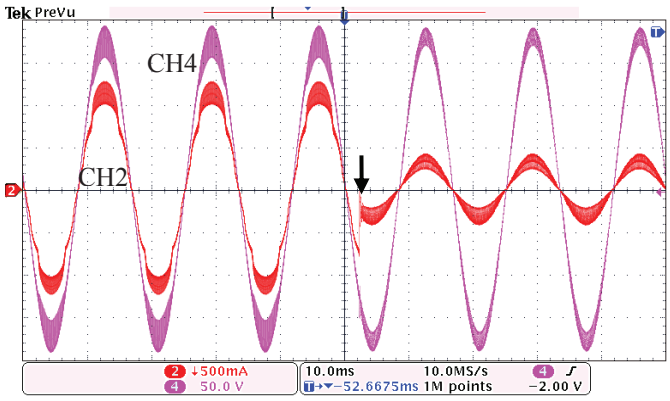

Fig. 18. Input (line) voltage (CH4 – 50 V/div) and input current (CH2 – 500 mA/div) when a dimming step from full load to 20% duty-cycle is applied. Time scale: 10 ms/div.

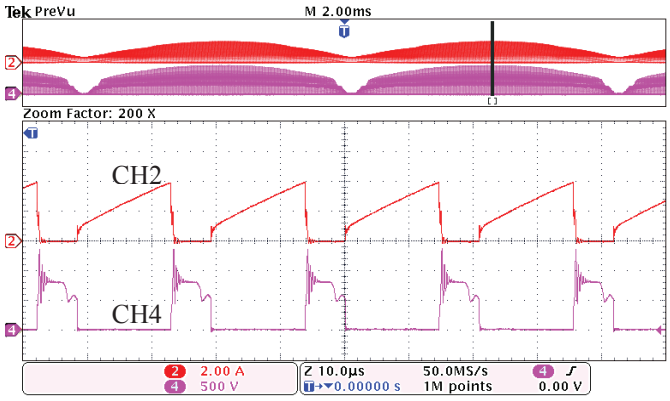

Fig. 19. Switch current (CH2 – 2 A/div) and voltage (CH4 – 500 V/div) at the peak of line voltage (V_G), for the maximum duty-cycle (d = 70%), showing peak current and voltage stresses on the shared power switch. Time scale: 10 µs/div.

VI. CONCLUSION

This work presented a novel single-switch converter topology for LED driving, which is capable of power factor correction and PWM dimming. The converter presented relies on a sole switch to perform all the functions of the driver, such as PFC on the input and dimming at the output; it also regulates the output peak current, keeping it constant in order to conserve chromaticity of the LEDs while dimming with a square current waveform. The operation strategy was to regulate peak output current by modulating the switching frequency, whereas the high-frequency PWM dimming function is performed by duty-cycle variations. It has been shown that PWM dimming provides better linearity and color stability than AM dimming, thus being the dimming technique of choice for developing the new LED driver topology.

A 100 W (peak) prototype of the converter was built for experimental validation of the novel topology. The experimental results presented accord with the theoretical description of the converter and operation was indeed very satisfactory for all the light levels intended for the driver. Power factor was kept high at all cases and efficiency reached a maximum of 82%, which is fair enough given the simplicity of the converter proposed and the lack of degrees of freedom to be explored for all the functions of the driver, also taking into account the current and voltage stresses in the shared switch.

Though not addressed in this paper, future works should bring the dynamic modeling of the converter to obtain a proper small-signal model for frequency and duty-cycle variations, thus enabling the design of a controller for closed-loop operation. Its function would be to dynamically regulate the output peak current at given light levels (controlled by d) by means of frequency modulation.

It is proposed that control action is taken only on the switching frequency to keep output peak current constant, whereas duty-cycle is directly altered by the user for achieving the desired light level, such as shown schematically in Fig. 20. A voltage-controlled oscillator (VCO) generating a triangular waveform (PWM carrier) is used to set the switching frequency of the converter, given the compensated frequency signal (f_s) fed from the controller.

In this case, it should be stressed that the crossover frequency of the peak current controller (e.g., a PI controller) should be low enough so as to not compensate the low-frequency ripple that appears as an envelope on the output current waveform (this compensation would lower the power factor, because it would also create instantaneous power fluctuations on the input).

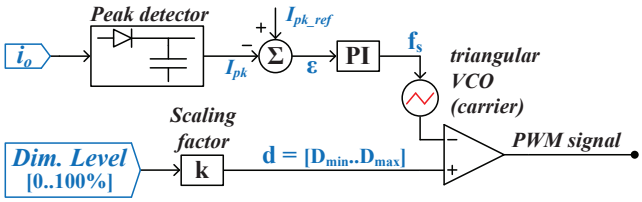

Fig. 20. Possible control scheme for the proposed converter.

A seminal work regarding this novel topology has recently been published by the authors [21], though presenting a more simplified analysis of the proposed LED driver and dimming technique.

ACKNOWLEDGMENT

Authors thank financial support from Eletrobras, CAPES, FAPEMIG, CNPq and the Electrical Engineering Post-Graduate Program of the Federal University of Juiz de Fora.

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