

A THREE-PHASE RECTIFIER FOR WECS WITH INDIRECT CURRENT CONTROL

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Abstract – This paper presents a novel Wind Energy Conversion System (WECS) capable of processing the energy from a Permanent Magnetic Synchronous Generator (PMSG) coupled to a three-blade wind turbine and injecting it into the utility power grid. This WECS is composed by two stages: a three-phase rectifier and a single-phase inverter. The ac-dc stage consists of three single-phase bridgeless rectifiers processing the power of each phase of the PMSG separately. The dc-ac stage is composed of a full-bridge inverter with controlled output current. Besides, indirect current control for High Power Factor (HPF) operation is employed, allowing the unification of two important techniques currently available, that are one cycle control (OCC) and self-control (SC). Additionally, a third technique, that comprises the optimum characteristics of both OCC and SC, is proposed and applied to the rectifier stage of the proposed WECS. The proposed WECS and control technique are both validated by experimental results from a 5kW prototype.

Keywords - Indirect current control, grid-connected system, one cycle control, power factor correction, self-control, three-phase bridgeless rectifier and wind energy systems.

I. INTRODUCTION

Since they do not require external excitation (absence of brushes) and allow a high number of poles (absence of gearboxes), permanent magnet synchronous generators (PMSGs) have been widely employed in variable speed WECS, allowing the reduction of maintenance costs and increasing the lifetime of the wind generator [1]-[3].

Its high efficiency and high reliability enable the reduction of the cost per kilowatt-hour generated from the wind, making the investment more attractive and reducing the payback time. Thus, injecting the energy generated by WECS into the conventional power grid becomes interesting, once that the use of battery banks is eliminated.

On the other hand, the use of synchronous generators in WECS connected to the grid requires the complete conditioning of generated power, since it occurs with variable frequency and amplitude. The usual way to accomplish this task is through electronic processing systems, where the generated voltage is rectified to establish a dc link. Then a voltage-source inverter injects the extracted

power in the form of electrical current [4]-[5] by using interface inductors, as shown in Figure 1.

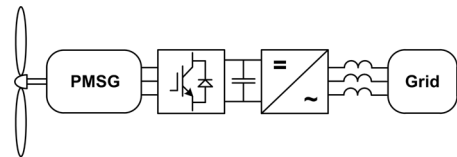


Fig. 1. Variable-speed WECS connected to the grid based on PMSG.

Low-order voltage and current harmonics cause heating in synchronous and asynchronous machines, reducing their efficiency, and may also cause damage to the torque development [6]. If the additional heating is not taken into account in the design of the machine, the harmonic components of voltage and current can still cause a reduction in the useful life of the generator. Therefore, the rectifier stage in systems similar to that represented in Figure 1 are supposed operate with high power factor.

This paper presents a WECS whose structure is similar to that in Figure 1. Its rectifier stage and the respective control technique allow the PMSG to see a resistive load, assuring high power factor operation. The proposed rectifier allows the modulation of both half cycles of the current extracted from the PMSG without using series-connected switches. Furthermore, the implementation of the proposed control technique for the rectifier does not demand a current compensator as well as a reference signal.

II. POWER PROCESSING TOPOLOGIES APPLIED TO WECS BASED ON PMSG

There are several power electronic structures that can be applied to WECS. The simplest arrangement that provides the operation of the rectifier stage with high power factor is shown in Figure 2 [7]-[11]. Its main advantages are control simplicity and the reduced number of components. However, in the rectifier stage, there are always three power semiconductors in the current path, reducing the efficiency of this topology. Also, PFC is achieved only in discontinuous conduction mode (DCM).

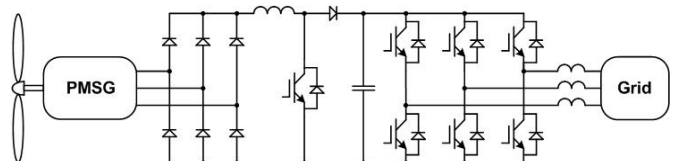


Fig. 2. WECS with intermediate boost converter.

Another option to achieve high power factor in the generator side is to use a pulse width modulation (PWM) rectifier in the WECS. The traditional topology applied in high power WECSs is shown in Figure 3 [12] and uses a back-to-back converter [13]-[14]. In the rectifier stage of this structure, there are only two semiconductors in the current path through each phase and the current can be modulated in both half cycles. However, there are switches connected in series, increasing the complexity of the drive circuit.

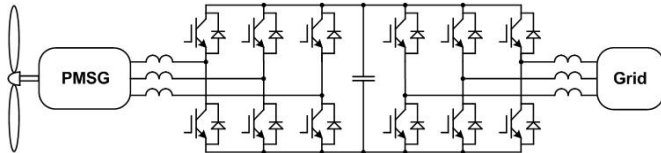


Fig. 3. WECS with back-to-back converter.

Figure 4 shows a WECS that uses a variation of the back-to-back converter [15], as proposed in [16]. Only four semiconductors are used in the rectifier stage of this topology. Moreover, maintaining voltage balance across the capacitors of the dc link is not a trivial task, what is compromised by the low degrees of freedom in modulation technique of this converter. Furthermore, there are still switches connected in series in the rectifier stage.

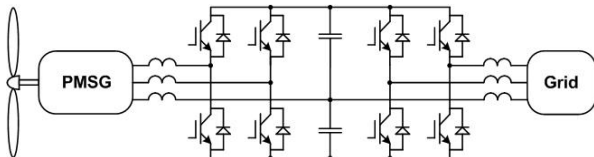


Fig. 4. WECS with a variation of the back-to-back converter.

An alternative to the back-to-back converter is shown in Figure 5 [17]. The rectifier stage of this WECS consists of a three-phase semi-controlled rectifier, and therefore all switches are connected to the same reference node, with no switches in series. However, this topology only allows the current extracted from the PMSG to be modulated in positive half cycles, reducing its power factor and increasing the total harmonic distortion (THD) of the input current.

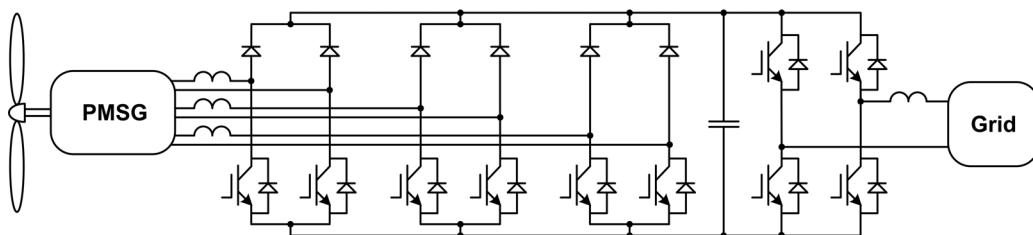


Fig. 6. Circuit of the proposed WECS.

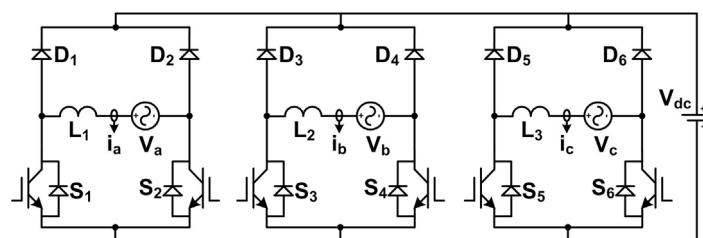


Fig. 7. Rectifier stage of the proposed WECS in detail.

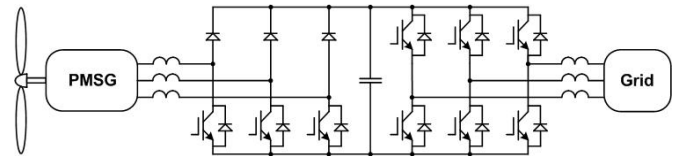


Fig. 5. WECS with three-phase semi-controlled rectifier.

III. PROPOSED POWER PROCESSING TOPOLOGY

Figure 6 presents the schematic diagram of the proposed WECS. The main advantage of this system lies in the ac-dc stage, which uses a single-phase bridgeless rectifier [18]-[23]. Then, considering the same power and dc link voltage ratings, there is an increase of the phase voltages of PMSG by $\sqrt{3}$ times, with corresponding reduction in its current, if compared to the rectifier stages of the WECSs in Figure 3 and Figure 5. Also there is an improvement in the loss distribution mechanism, since more semiconductors are used.

In addition, there are only two power semiconductors in the current path of each phase; all switches of the rectifier stage are connected to the same reference node, what avoids short circuit through a leg and simplifies the driver circuit; and both half cycles of the input currents can be modulated.

A full-bridge single-phase inverter was chosen as the dc-ac stage, with experimental validation from a prototype rated at input power of 5 kW and input voltage per phase of 220 V. For higher power levels, a three-phase inverter stage with higher input voltage level is more appropriate in order to reduce the current stresses in the semiconductors.

A. Rectifier stage

The rectifier stage of the proposed WECS is shown in detail in Figure 7, as the dc link and inverter are represented by a dc voltage source. Voltages $V_{a,b,c}$ are the output voltages of PMSG and inductors $L_{1,2,3}$ are the boost inductors of the rectifier. Each one of the bridgeless rectifiers operates independently and is phase-shifted in time by 120 electrical degrees.

In continuous conduction mode (CCM), each rectifier has four stages of operation: two stages during the positive half cycle and two stages during the negative half cycle, as shown in Figure 8, considering the bridgeless rectifier associated with phase 'a' of the PMSG.

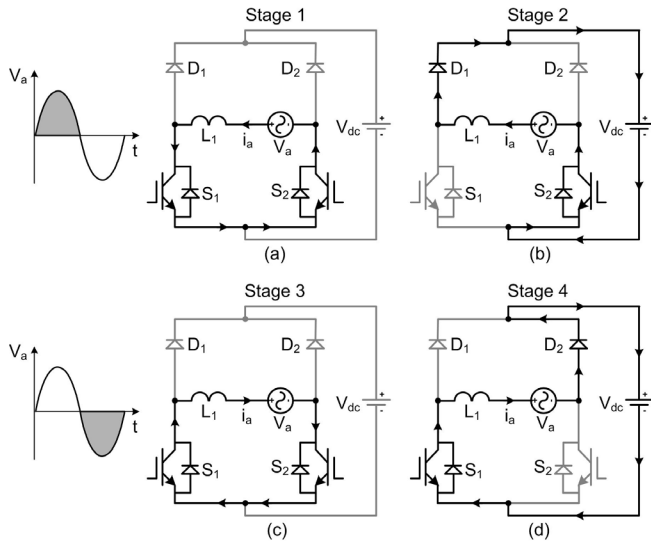


Fig. 8. Operation stages of the bridgeless rectifier.

During the positive half cycle of the input voltage V_a , the topological state of the bridgeless rectifier depends only on the state of switch S_1 . When S_1 is turned on (Figure 8.a), the PMSG transfers energy to L_1 and current i_a increases. When S_1 is turned off (Figure 8.b), both the PMSG and L_1 transfer energy to the dc link. The stages related with the negative half cycle of V_a (Figure 8.c and Figure 8.d) are similar, except that the topological state of the rectifier is determined by the state of switch S_2 .

Since only one switch determines the topological state of the bridgeless rectifier in each half cycle of input voltage, these switches can be commanded symmetrically or asymmetrically. In the asymmetrical command, aiming to reduce losses by reverse conduction, each switch remains turned on during the half cycle in which it does not influence the operation of the topology.

However, this strategy involves a more complex control circuit and is only effective when using MOSFETs. In symmetrical command, both switches are driven with the same gating signal, simplifying the drive circuit, as this strategy was adopted in this work.

B. Voltage and current stresses in the semiconductors of the rectifier stage

The modulation index M_r of the rectifier stage is given by Eq. (1), where V_{epk} is the PMSG output phase voltage peak value and V_{dc} is the dc link voltage average value.

$$M_r = \frac{V_{epk}}{V_{dc}} \quad (1)$$

The maximum voltage across the semiconductors of the rectifier stage is equal to the dc link voltage. The average (I_{SRavg}) and rms (I_{SRrms}) values of the reverse current through each switch ($S_{1, \dots, 6}$) are given, respectively, by Eqs. (2) e (3), where I_{epk} is the peak value of the phase current.

$$I_{SRavg} = \frac{I_{epk}}{\pi} \quad (2)$$

$$I_{SRrms} = \frac{I_{epk}}{2} \quad (3)$$

The average (I_{Davg}) and rms (I_{Drms}) values of the current that flows through each boost diode ($D_{1, \dots, 6}$) are given, respectively, by Eqs. (4) and (5).

$$I_{Davg} = \frac{I_{epk}}{4} \cdot M_r \quad (4)$$

$$I_{Drms} = I_{epk} \cdot \sqrt{\frac{2}{3 \cdot \pi}} \cdot M_r \quad (5)$$

The average (I_{Savg}) and rms (I_{Srms}) values of the forward current through each switch ($S_{1, \dots, 6}$) are given, respectively, by Eqs. (6) and (7).

$$I_{Savg} = I_{SRavg} - I_{Davg} \quad (6)$$

$$I_{Srms} = \sqrt{I_{SRrms}^2 - I_{Drms}^2} \quad (7)$$

C. Inverter stage

Figure 9 shows the inverter stage, where the dc link and the rectifier stage are represented by a voltage source (V_{dc}), L_s is the interface inductor between the inverter and the power grid and V_r is the grid voltage.

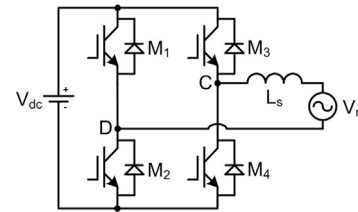


Fig. 9. Inverter stage of the proposed WECS.

In order to reduce the volume and weight of L_s , as well as the inverter switching losses, unipolar modulation was adopted to generate the control signals of switches $M_{1, \dots, 4}$.

D. Voltage and currents stresses in the semiconductors of the inverter stage

The modulation index M_i of the inverter stage is given by Eq. (8), where V_{rpk} is grid voltage peak value and V_{dc} is the average dc link voltage.

$$M_i = \frac{V_{rpk}}{V_{dc}} \quad (8)$$

The maximum voltage across the semiconductors of the inverter stage is equal to the dc link voltage. The average (I_{MRavg}) and rms (I_{MRrms}) values of the current through each respective anti-parallel diode of a given switch ($M_{1, \dots, 4}$) are given by (9) and (10), respectively, where I_{Lspk} is the peak value of the output inverter current.

$$I_{MRavg} = 0.19 \cdot \frac{I_{Lspk}}{\pi} \quad (9)$$

$$I_{MRrms} = 0.41 \cdot \frac{I_{Lspk}}{2} \quad (10)$$

The average (I_{Mavg}) and rms (I_{Mrms}) values of the forward current through each inverter switch ($M_{1, \dots, 4}$) are given, respectively, by Eqs. (11) and (12).

$$I_{Mavg} = \frac{I_{Lspk}}{4} \cdot M_i + I_{MRavg} \quad (11)$$

$$I_{Mrms} = \sqrt{2 \cdot I_{Lspk}^2 \cdot \frac{M_i}{3 \cdot \pi} + I_{MRrms}^2} \quad (12)$$

IV. RECTIFIER STAGE CONTROL

A. High power factor operation

Figure 10 shows a flowchart that presents the classification of the main techniques for power factor correction, based on the following characteristics:

- Type: active or passive;
- Conduction mode: discontinuous (DCM), boundary (BCM), or continuous (CCM);
- Switching frequency: variable or fixed;
- Current control: direct or indirect.

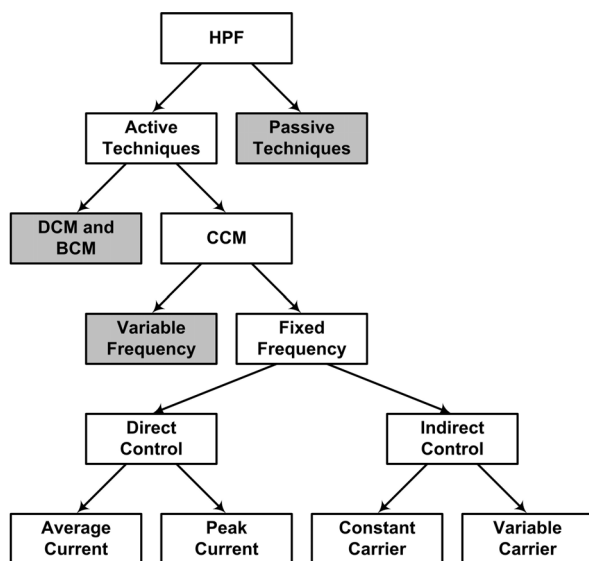


Fig. 10. Classification of PFC techniques.

The passive techniques are beyond the scope of this work. In active techniques, the operation in DCM and BCM involves high current stresses across the semiconductors and higher levels of electromagnetic interference (EMI), as the power level for applications where such control techniques can be used becomes restrict [24].

The techniques applied to CCM converters with variable switching frequency makes the design of reactive elements quite complex while the maximum switching frequency may become too high, reducing the rectifier efficiency. Thus, active techniques for power factor correction in CCM with fixed switching frequency are the most widely used industrially. These techniques can also be classified based on the direct or indirect current control [25].

B. Direct current control

In direct current control techniques, the input current is imposed through a specific control loop. This control loop compares the feedback signal of the input current with a reference signal which has the shape, phase and proportional amplitude as desired. The main direct current control

techniques are: peak current control (Figure 11.a) [26] and average current control [27] (Figure 11.b).

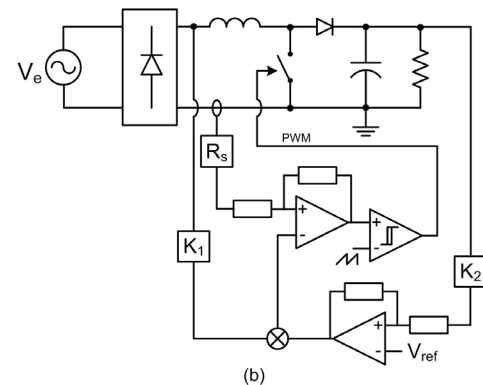
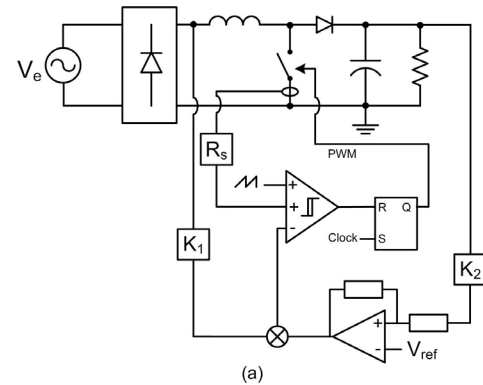


Fig. 11. PFC rectifiers operating with a) peak current control and b) average current control.

The low noise immunity and unstable behavior for duty cycle values higher than 0.5 for the peak current control [26], and the complex implementation for average current control led to research of simpler control techniques. The results of such studies have been reported from the second half of the 1990s in several papers [24][25][28], and resulted in the indirect current control theory.

C. Indirect current control

In indirect current control, the feedback current signal is directly used in the PWM control of the rectifier switches. Then low current THD results, without the need for a current reference signal and even a compensator for the current loop. Analogously to the conventional power factor correction boost rectifier, the static gain of the single-phase bridgeless rectifier, shown in Figure 12, is given by Eq. (13).

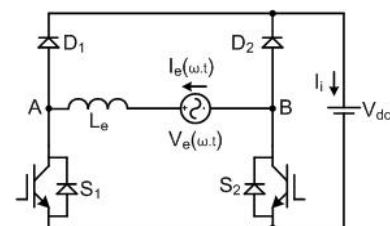


Fig. 12. Schematic diagram of the single-phase bridgeless rectifier.

$$V_{dc} = |V_e(\omega \cdot t)| \cdot \frac{1}{1-D} \quad (13)$$

When operating with high power factor, in terms of nodes A and B, the bridgeless rectifier is seen as a resistance R_e , as shown in Figure 13.

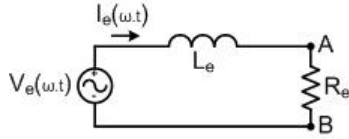


Fig. 13. Electrical model of the high power factor bridgeless rectifier.

When $R_e \gg L_e$, by Ohm's law, it gives:

$$|V_e(\omega \cdot t)| = R_e \cdot |I_e(\omega \cdot t)| \quad (14)$$

Substituting Eq. (14) in Eq. (13) and algebraically manipulating the terms, it comes to Eq. (15).

$$1 - D = \frac{R_e}{V_{dc}} \cdot |I_e(\omega \cdot t)| \quad (15)$$

Eq. (15) establishes that the complementary duty cycle of the bridgeless rectifier's switches, operating with high power factor, is directly proportional to the absolute value of the input current, whose proportionality factor K_∞ is given by Eq. (16).

$$K_\infty = \frac{R_e}{V_{dc}} \quad (16)$$

Figure 14 shows the representation of Eq. (15) in terms of a schematic diagram, where R_{sh} is the current sensor gain, F_m is the modulator gain and ABS is the absolute value function.

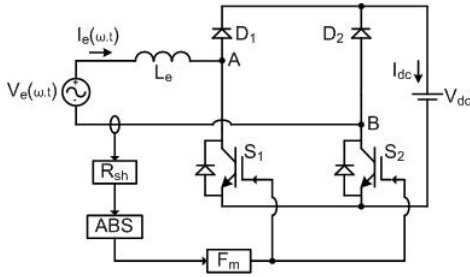


Fig. 14. Schematic representation of Eq. (15).

The open loop gain (K_{ol}) in Figure 14 is given by Eq. (17).

$$K_{ol} = R_{sh} \cdot F_m \quad (17)$$

By equating Eq. (16) to Eq. (17), R_e can be expressed as a function of current sensor gain R_{sh} , modulator gain F_m and rectifier output voltage V_{dc} , as given by Eq. (18).

$$R_e = R_{sh} \cdot F_m \cdot V_{dc} \quad (18)$$

According to Eq. (18), one can vary the emulated resistance (R_e) by changing either the current sensor gain (R_{sh}) or the modulation gain (F_m), resulting in two types of indirect current control: indirect current control with fixed carrier and indirect current control with variable carrier.

1) Indirect current control with fixed carrier

In indirect current control with fixed carrier [28], the PWM modulation is performed by comparing the current feedback signal with a fixed slope carrier. The variation of the emulated resistance R_e occurs by multiplying the current sensor signal by a control signal v_m obtained from maximum

power point tracker, which increases or decreases the current sensor gain, as shown in Figure 15.

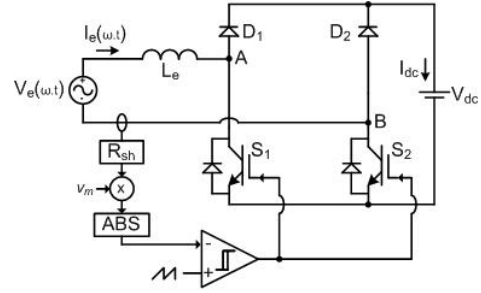


Fig. 15. Indirect current control with fixed carrier.

With the technique shown in Figure 15, the emulated resistance R_e can be given by Eq. (19).

$$R_e = v_m \cdot R_{sh} \cdot F_m \cdot V_{dc} \quad (19)$$

2) Indirect current control with variable carrier

In indirect current control with variable carrier, PWM modulation is performed by comparing the current feedback signal with an adjustable slope carrier. The adjustable slope carrier results in a modulator with variable gain, allowing the control of the emulated resistance R_e . The work proposed in [24] uses a resettable integrator excited by a control signal v_m to implement the carrier with adjustable slope, as shown in Figure 16.

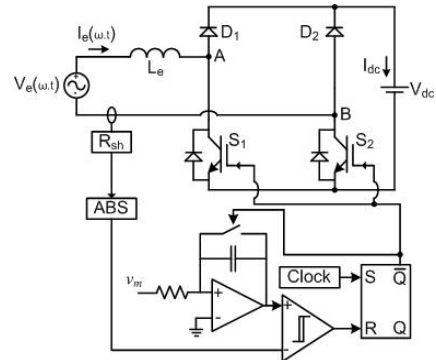


Fig. 16. Indirect current control with variable carrier.

However, this technique results in a rather complex and difficult to implement modulator, in either analog or digital ways. An adjustable slope carrier can be obtained more easily using only one fixed slope carrier and a multiplier circuit. Figure 17 illustrates this new technique.

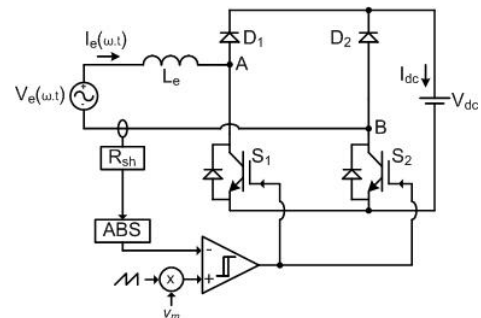


Fig. 17. New indirect current control technique with variable carrier.

This is the technique used to control the rectifier stage of the WECS proposed in this paper. In both indirect current control with variable carrier techniques, the emulated resistance R_e is given by Eq. (20).

$$R_e = \frac{R_{sh} \cdot V_{dc}}{V_m} \quad (20)$$

V. INVERTER STAGE CONTROL

The traditional average current control technique was used in the inverter stage, in order to inject a current in phase with the grid voltage and with low THD, as shown in Figure 18.

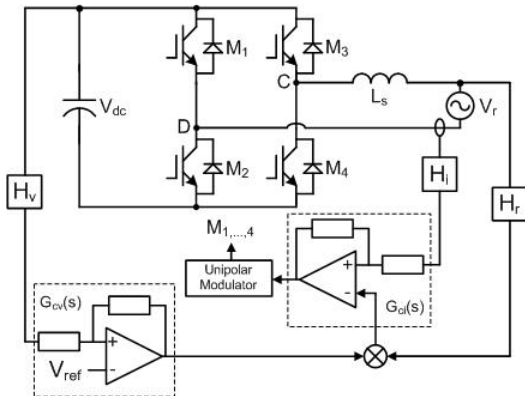


Fig. 18. Closed-loop operation of the inverter stage.

From the grid voltage, and by adjusting gain H_r , both the shape and synchronism signal of the injected grid current are obtained. The voltage controller ($G_{cv}(s)$) adjusts the amplitude of the current shape through a multiplier, thus changing the rms value of grid-injected current in order to maintain the value of dc link feedback signal equal to the reference value V_{ref} .

The current controller ($G_{ci}(s)$) provides the modulating signal to the unipolar modulator in order to make the feedback signal of the grid interface inductor (L_s) follow the control signal provided by voltage controller.

VI. EXPERIMENTAL RESULTS

The proposed WECS prototype was built and tested, whose picture is shown in Figure 19.

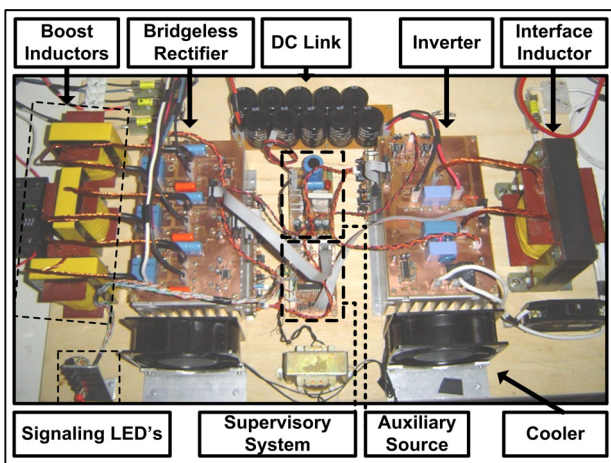


Fig. 19. Prototype picture.

The specifications and parameters used to implement the prototype are shown in Tables I and II.

TABLE I
Rectifier Specifications and Parameters.

Parameter	Specification
Rms input voltage range	50 V – 210 V
Input voltage frequency	60 Hz
Output voltage	400 V
Switching frequency	30 kHz
Input inductors	1 mH
Input power	5 kW

TABLE II
Inverter Specifications and Parameters.

Parameter	Specification
Dc link voltage	400 V
Grid voltage	220 V
Grid frequency	60 Hz
Output inductor	1.5 mH
Switching frequency	30 kHz
Output power	4.6 kW

Figure 20 shows phase ‘a’ current and as well as its respective voltage for rated power. The obtained power factor is equal to 0.995, and the total harmonic distortion of the current is about 1.66%.

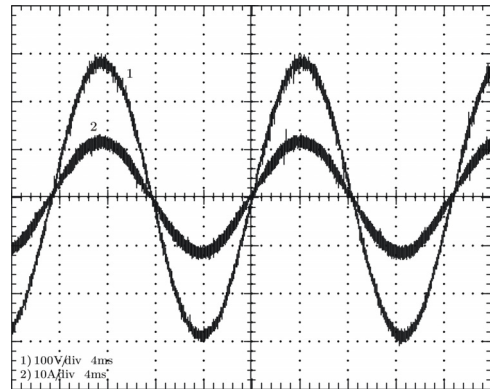


Fig. 20. Rectifier boost inductor current (2 - 10 A/div - 4 ms) and input voltage (1 - 100 V/div - 4 ms) waveforms of phase ‘a’.

Figure 21 presents the three-phase line currents of the rectifier for the rms phase voltage equal to 210 V and rated power.

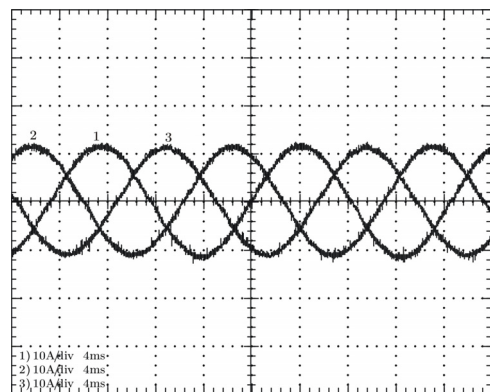


Fig. 21. Line currents of the rectifier stage for input line voltage of 210 Vrms (10 A/div - 4 ms)

Figure 22 represents the harmonic spectrum of the input current at rated power. Such results demonstrate that the proposed technique is able to extract quasi-sinusoidal currents from the generator, with good equilibrium among the line currents, what minimizes the losses and mitigates oscillating torque.

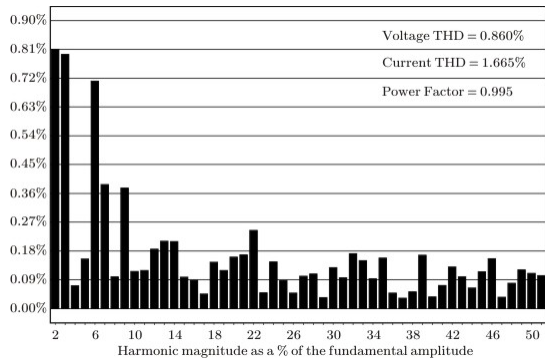


Fig. 22. Harmonic spectrum of the input current of the rectifier stage ($V_{in}=210$ Vrms and $P_{in}=5$ kW).

Figure 23 shows the current injected in the grid by the inverter and the utility voltage, as the achieved power factor is 0.998.

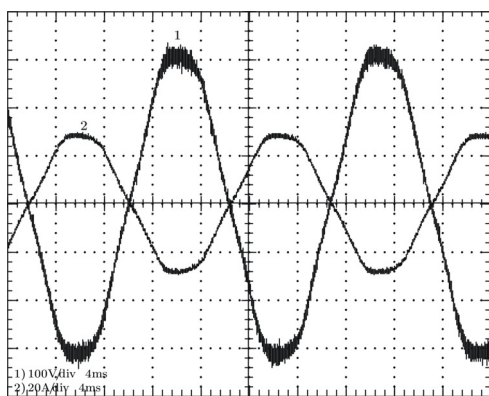


Fig. 23. Grid voltage (1 - 100 V/div - 4ms) and inverter-grid current (2 - 20 A/div - 4ms) waveforms.

The total harmonic distortion of the grid-injected current is about 4.25%, as the third and the fifth harmonics are the most relevant components, as shown in Figure 24.

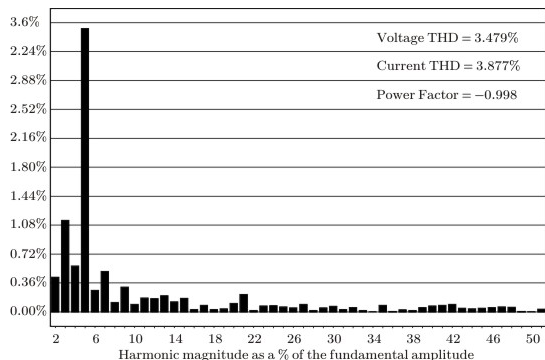


Fig. 24. Harmonic spectrum of the grid-injected current.

Such waveforms show that the technique used to control the inverter stage is able to inject currents into the grid with low THD and near zero reactive power.

Figure 25 shows the dynamic response for a positive step in the rectifier input voltage from 61.6 Vrms (1 kW) to 98.3 Vrms (4 kW).

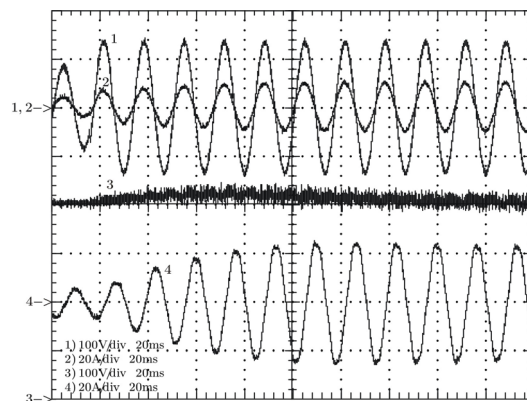


Fig. 25. Rectifier input voltage (1 - 100V/div - 20ms), rectifier input current (2 - 20A/div - 20ms), dc link voltage (1 - 100 V/div - 20ms) and grid-injected current waveform (4 - 20A/div - 20ms).

Figure 26 shows the dynamic response for a negative step in the input rectifier voltage from 98.3Vrms (4 kW) to 61.6Vrms (1 kW).

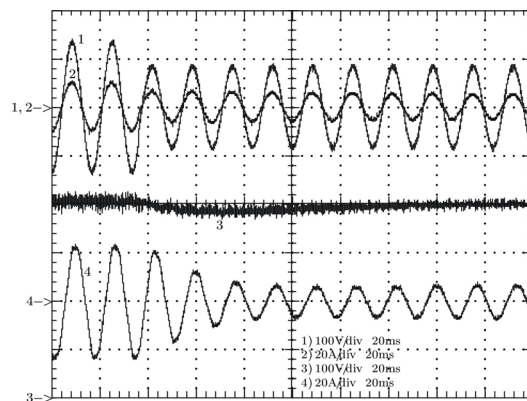


Fig. 26. Rectifier input voltage (1 - 100V/div - 20ms), rectifier input current (2 - 20A/div - 20ms), dc link voltage (1 - 100 V/div - 20ms) and grid-injected current waveforms (4 - 20A/div - 20ms).

One can see in Figure 25 and Figure 26 that the response of the control loop is slow in order to keep low THD of the grid injected current but satisfactory voltage regulation is achieved even in high load step situations. Figure 27 shows the measured efficiencies compared with similar works [17].

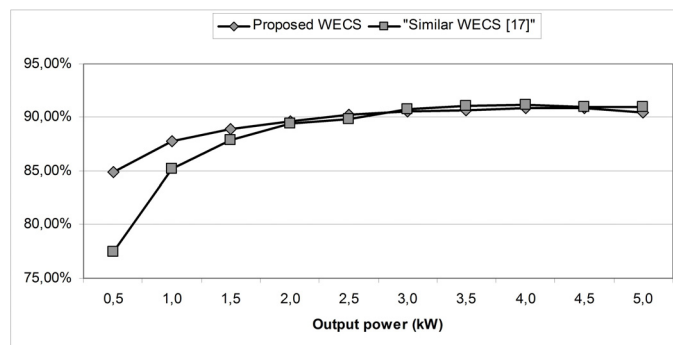


Fig. 27. Efficiency versus output power of the proposed WECS and WECS proposed in [17].

It must be mentioned that, since the current THD and the rms currents are lower than those obtained in [17], additional gain in the efficiency is expected in the electrical generator, what improves the overall efficiency of the WECS.

VII. CONCLUSION

A wind energy conversion system has been presented and developed. The main advantages, when compared to other topologies mentioned, are the use of switches connected to the same reference node, robustness due to the absence of controlled switches in the same leg and the ability to process times more power, considering the same voltage and current switches ratings.

Furthermore, it summarizes the indirect current control for high power factor rectifiers and a new indirect current control with variable carrier implementation technique has been proposed and validated with experimental results.

The experimental results from an experimental prototype rated at 5kW have shown the system effectiveness, which presents an average global efficiency of 90%, power factor higher than 0.99 in both input and output quantities of the WECS and very low harmonic distortion of rectifier input currents and grid-injected current.

Also, there is an additional gain in the generator design, because lower phase currents and higher phase voltages can be used considering the same power and dc link voltage ratings.

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