COMPARATIVE ANALYSIS AMONG INTEGRATED AND SIMPLIFIED ZVT TOPOLOGIES APPLIED TO THREE-PHASE INVERTERS

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***Abstract* – This paper presents a peer comparison between the integration and simplification concepts of zero-voltage-transition (ZVT) circuits applied to voltage fed three-phase inverters used in industrial adjustable-speed drives. Initially, both concepts are defined and their main advantages and limitations are identified. Thereafter, a comparison is made between two selected topologies, considering modulation strategies, main and auxiliary circuit losses and the harmonic content of the inverter output voltage. It is demonstrated that when the load demands a voltage with low harmonic content, the simplified ZVT topologies are recommended and when the number of components is the main concern, the integrated ZVT topologies may be the best choice. Finally, experimental results for the selected topologies operating at 1.5 kW and 20 kHz are presented in order to confirm the comparative analysis carried out. The simplified ZVT topology presented an efficiency of 98.1% at nominal operation while the integrated ZVT topology presented an efficiency of 97.2% at the same condition.**

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***Keywords* – Harmonic Content, Semiconductor Losses, Soft-Switching, Zero-Voltage-Switching.**

I. INTRODUCTION

Modern power electronics applications, such as uninterrupted power supplies [1], distributed generation [2], and converter and motor-drive systems [3], usually comprise a set of static converters (multistage) or multipole converters. One remarkable application of multiphase converters is in industrial adjustable-speed drives (ASDs), composed by a three-phase voltage-source inverter. In the last decades, successive advances of the IGBT technology have made it possible to considerably reduce the size and cost per kilowatt of industrial ASDs. However, problems related to high frequency pulse-width modulation (PWM) inverters, such as voltage transients of harmful effects on motor winding insulation [3] and EMI degradation [4], still a primary concern.

Many of these problems can be overwhelmed by employing soft-switching techniques [5], which also allow an increase in the PWM frequency without penalizing the converter efficiency. Additional benefits of high-frequency operation are superior dynamic response [6] and increased power density, with reduced audible noise [7].

The zero-voltage-transition (ZVT) technique has received special attention by researchers [8]-[14] due to its simplicity, soft-switching conditions for a wide load range, closest operation to the PWM converter counterpart and low losses in the auxiliary commutation circuit (ACC) [9].

Aiming to make the ZVT multipole converters even more attractive to the competitive industrial ASD market, many topologies have been proposed [10]-[12] with reduced switch count and lower cost. The reduced number of auxiliary switches is achieved by means of an integrated auxiliary commutation circuit (iACC), represented in the schematic of Fig. 1 (a). The iACC provides conditions to commutate every main semiconductor switch under zero-voltage-switching (ZVS). Regrettably, these structures introduce some restrictions on converter operation, such as the requirement of synchronized switching events in the PWM poles. To avoid these restrictions, simplified auxiliary commutation circuits (sACC) have been proposed [13]-[14], where each ACC operates independently per PWM pole, as represented in the schematic of Fig. 1 (b). Therefore, this approach enables to modulate the PWM poles independently in multipole applications, allowing the application of any modulation strategy, such those that aim to obtain a minimum total harmonic distortion (THD) or a reduction in the switching losses [15]-[16].

This way, in order to address the benefits and constraints of integrated and simplified ZVT topologies, a comparison between the concepts of integration and simplification of ZVT auxiliary circuits applied to three-phase inverters used in the industrial ASDs is made in this paper, where detailed analyses are presented as well as new conceptual insights.

This paper is organized as follows: Section II presents the concepts of integration and simplification of multipole ZVT topologies. Section III describes the design procedure, the modulation strategies of the compared topologies and the comparison methodology itself. The comparative results obtained by simulation are presented in Section IV meanwhile experimental results are provided in Section V. Finally, Section VI presents the conclusions.

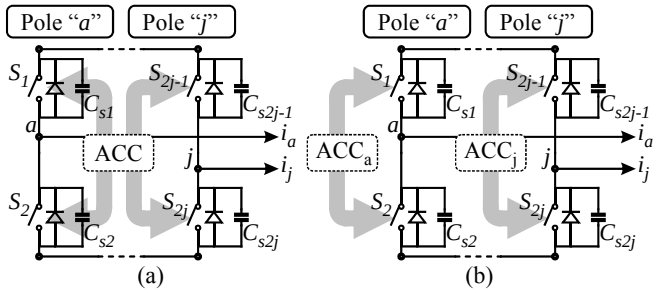

Fig. 1. Conceptual ZVT circuits. (a) Integrated ACC. (b) Simplified ACC.

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II. DEFINITIONS FOR THE INTEGRATION AND SIMPLIFICATION CONCEPTS

To achieve the zero-voltage conditions for the PWM pole switches (S_1, S_2,…S_{1j}, S_{2j}), a parallel path to divert the current flowing out (in) to the pole must be provided. This way, a controlled current source must be connected to each PWM node ("*a*" to "*j*", Fig. 1). Usually, an inductor (L_{xj}) is employed in order to provide a current path in the ACC with a controlled *di/dt* slope [17], reducing the reverse recovery phenomenon in PWM pole antiparallel diodes. In order to charge or discharge L_{xj}, it is mandatory to apply an appropriate voltage level across its terminals, which can be accomplished by using an auxiliary voltage source (AVS) – composed of a set of devices (auxiliary switches and voltage sources) [9].

As demonstrated in the following sections, both integration and simplification methodologies are based on the different possibilities of AVS implementation.

A. The ZVT Auxiliary Circuit Integration Concept (iACC)

The ZVT iACC concept is defined as the reduction of the ACC by sharing one or more of the AVS components among two or more PWM poles or stages. A reduction in the number of components needed to obtain the ZVS is achieved only by using the energy of one commutation to assist another, Fig. 1 (a). The synthesis methodology of ZVT iACC is proposed in [9], which is based on the interconnection in series or in parallel the AVSs of different ACCs. In the series integration, the current is transferred from one pole to another with the objective of reducing the circulating energy and the number of devices. On the other hand, in the parallel integration the current from the poles is transferred to a terminal with constant voltage level. It objectives only to reduce the number of ACC devices, i.e., no energy is saved.

The main drawback of the iACC concept is the need for synchronous-switching of the PWM poles, which makes its design methodology more restraining and complex [17]. Therefore, for three-phase inverters, complex modulation techniques are required, with a particular switching state vector (SSV) sequence, which usually includes an additional "extra" vector (non-adjacent to the reference voltage vector in the Space Vector Modulation), making it impossible to employ SSVs with a reduced output voltage THD or reduced switching losses, as in [15].

B. The ZVT Auxiliary Circuit Simplification Concept (sACC)

The ZVT sACC concept is defined as the reduction of the ACC by sharing one or more of the AVS devices between the semiconductor switches of the one PWM pole, as depicted in Fig. 1 (b). A synthesis methodology of ZVT sACC is presented in [18], which is based on the reduction of the number of high-frequency controlled switches necessary to implement the AVS. This way, [18] proposes a set of "simplified switches" that employ only one high-frequency controlled switch. It is important to notice that the set of simplified switches can be placed at different locations into the sACC, i.e. connected to other auxiliary devices, connected to the dc rails or connected to the middle point of the dc bus, according to the rules established [18].

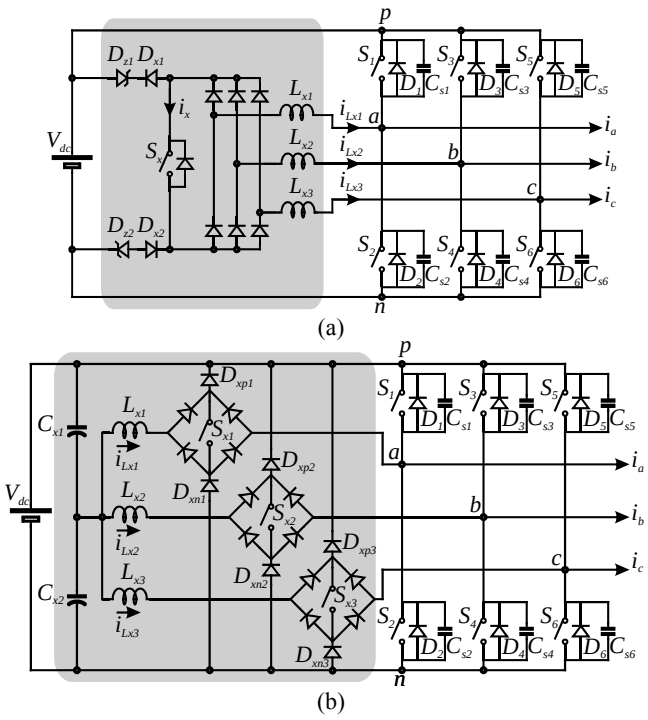


Fig. 2. Analyzed topologies. (a) Integrated topology from [11]. (b) Simplified topology from [14].

III. COMPARISON METHODOLOGY

In order to compare the main advantages and drawbacks of both integration and simplification concepts applied to ZVT circuits, two topologies have been selected for the following analyses. Figure 2 (a) shows the iACC ZVT topology chosen [11] and Fig. 2 (b) shows the sACC ZVT topology chosen [14] to represent each concept in the following analysis.

The comparison methodology between iACC and sACC ZVT topologies of Fig. 2 is based on the semiconductor device loss analysis and on the harmonic content of the line voltage supplied to the load. In order to carry out a fair comparison, the design methodology and modulation strategies of both topologies are based on the same criteria.

A. Auxiliary Circuit Design

For simplicity, it is considered that $L_x = L_{x1} = L_{x2} = L_{x3}$ as well as $C_s = C_{s1} = ... = C_{s6}$.

1) Integrated ZVT Topology

Aiming to limit the *di/dt* slope in the turn-off of the antiparallel diodes D_1, D_2, … [19], the minimum value of $L_{x(min)}$ can be calculated according to (1), where V_{dc} is the dc bus voltage. To guarantee the ZVS turn-on of the main switches, they must not be turned-on during the resonant period [20]. Thus, the resonant interval must be smaller than their dead-time (t_{d_on}). Otherwise, the selected dead-time must be higher than the minimum dead-time ($t_{d(min)}$) necessary to block completely the main switches. Then, the minimum snubber capacitor ($C_{s(min)}$) that ensures this condition can be calculated by (2).

$$L_{x(min)} = \frac{2V_{dc}}{3\,di/dt_{(max)}} \tag{1}$$

$$C_{s(min)} = \frac{t_{d(min)}^{\ 2}}{2L_x\pi^2} \quad (2)$$

Other important parameters to be considered in the iACC design are the maximum inverter modulation index ($m_{(max)}$) and the current peak through the iACC devices. The maximum modulation index can be calculated by (3), where $D_{(max)}$ is the maximum duty-cycle and $D_{(min)}$ is the minimum duty-cycle, both dependent of the iACC operation times. The definition of $D_{(max)}$ and $D_{(min)}$ is explained in detail in Appendix A. Additionally, the normalized current peak through the iACC devices ($\bar{i}_{ACC(pk)}$), normalized to the load current peak ($i_{j(pk)}$), can be calculated by (4), where I_{lin} is the current at the end of the linear charging stage, and $i_{res(pk)}$ is the resonant current peak (vide Appendix A).

$$m_{(max)} = D_{(max)} - D_{(min)} \quad (3)$$

$$\bar{i}_{ACC(pk)} = \frac{I_{lin} + i_{res(pk)}}{i_{j(pk)}} \quad (4)$$

2) Simplified ZVT Topology

The minimum value for the auxiliary inductors for a given maximum *di/dt* slope in the turn-off of the antiparallel diodes can be calculated by (5). The $C_{s(min)}$ can be calculated by (2). In the same way, $D_{(max)}$ and $\bar{i}_{ACC(pk)}$ for sACC can be calculated by (3) and (4).

$$L_{x(min)} = \frac{V_{dc}}{2\,di/dt_{(max)}} \quad (5)$$

This topology allows defining a minimum load current ($I_{(min)}$) for a snubber commutation that ensures the discharge of C_s to a desired voltage level before turning on the complementary main switch. Thus, for values below $I_{(min)}$, the ACC can assist the commutation from switch to antiparallel diode of the PWM pole. Therefore, $I_{(min)}$ can be calculated by (6), where t_{d_off} is the dead-time selected for the turn-off of the main switches, with $t_{d\_off} \geq t_{d(min)}$, and V_{th} is the desired voltage level. Furthermore, as the analyzed topology makes use of the dc bus mid-point, it demands a boosting current (I_{bst}) previous to the resonant stage in order to compensate for the conduction losses in the sACC, thus ensuring the ZVS condition.

$$I_{(min)} = 2\,C_s\left(V_{dc} - V_{th}\right)\big/ t_{d\_off} \quad (6)$$

B. Space Vector Modulation Scheme

For simplicity, in the following analysis is assumed that the reference voltage vector ($\mathbf{V_{ref}}$) is in the sectors I or II of the SVM Hexagon (αβ coordinates) presented in Fig. 3 (a), and the load current vector ($\mathbf{I_{load}}$) is in sector I, representing a maximum displacement of 30° between them. Considering the load current directions defined in Figure 2, through the relation between the spaces in αβ coordinates and *abc* coordinates, it can be demonstrated that $i_a(t) > 0$, $i_b(t) < 0$ and $i_c(t) < 0$. In addition, $i_a(t)$ is the highest current in sector I.

1) Integrated ZVT Topology

In the aforementioned conditions, the iACC must assist the commutation from D_2, D_3 and D_5 [$\mathbf{V_{4(npp)}}$] to S_1, S_4 and S_6 [$\mathbf{V_{1(pnn)}}$], respectively, as shown in Figure 2(a). The subscript letters represent the state of the PWM poles, i.e. "*npp*" corresponds to the state that the node "*a*" is connected to the negative dc bus "*n*," and the nodes "*b*" and "*c*" are connected to the positive dc bus "*p*" (see Figure 2).

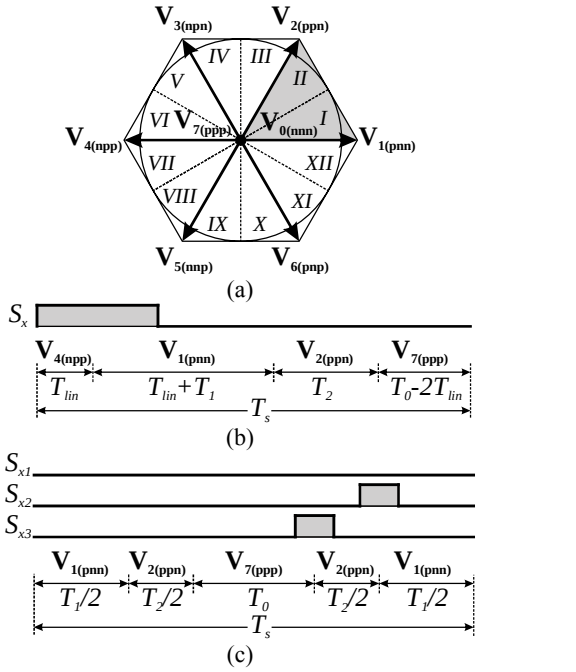


Fig. 3. Space Vector Modulation. (a) SVM Hexagon. (b) SSVs of the integrated topology. (c) SSVs of the simplified topology.

In order to activate the iACC only once per switching period (T_s), the turn-on of S_1, S_4 and S_6 must be synchronized. It can be seen that $\mathbf{V_{1(pnn)}}$ and $\mathbf{V_{4(npp)}}$ are complementary vectors and, also, $\mathbf{V_{4(npp)}}$ is an extra SSV non-adjacent to $\mathbf{V_{ref}}$. According to [21], it is reasonable to use the nearest possible SSV of $\mathbf{V_{ref}}$, since this result in smaller ripples over variables of interest (load currents or voltages). Expanding the analysis to other sectors, it can be concluded that at least one extra non-adjacent SSV is necessary in each case. This characteristic yields in an important limitation of iACC ZVT topologies.

The modulation strategy proposed by [11] for this topology can be seen in Figure 3(b), where T_{lin}, T_1, T_2 and T_0 represent the times that each vector must be applied during the switching period. The determination of T_{lin} is presented in Appendix A. It can be noted that the auxiliary switch, S_x, must be turned on simultaneously with the application of $\mathbf{V_{4(npp)}}$ and must be turned off after the demagnetization of the auxiliary inductors, which finish before the change from $\mathbf{V_{1(pnn)}}$ to $\mathbf{V_{2(ppn)}}$. The remaining SSVs are defined by opening the switches S_4 and S_6 one after another.

2) Simplified ZVT Topology

As the auxiliary circuit operates individually for each PWM pole, the sACC ZVT topology has one additional degree of freedom for the selection of the SSVs sequence. Therefore, the selected sequence may employ only adjacent SSVs to $\mathbf{V_{ref}}$, it also may be symmetric (to reduce the output voltage harmonics [15]), and does not commutate the PWM pole with the highest current, as can be seen in Figure 3(c). The selected sequence does not commutate the pole "*a*," and only a main switch changes its state (on/off)

from one SSV to the following one, as indicated by the subscript letters of the SSVs. In addition, the SSVs are allocated symmetrically in the switching period to reduce the output voltage harmonic content.

As shown in Figure 3(c), the auxiliary switches S_{x2} and S_{x3} are turned on only during the commutation process from D_3 to S_4 [$\mathbf{V_{2(ppn)}}$ to $\mathbf{V_{1(pnn)}}$] and from D_5 to S_6 [$\mathbf{V_{7(ppp)}}$ to $\mathbf{V_{2(ppn)}}$], respectively. It can be noted in Figure 3(c) that the pole "*a*" does not commutate because it conducts the highest current in this sector, reducing the switching losses. Thus, the auxiliary switch correspondent to the pole "*a*," S_{x1}, is not turned-on during this switching period.

C. Loss Analysis of ZVT Topologies

As presented in [19], the loss analysis is carried out according to the information provided by the semiconductor manufacturers in the datasheets of the selected devices or by experimental measurement of conduction and switching losses. The main circuit has been implemented with three SKM50GB123D dual-pack SEMIKRON® modules (1200V/50A). The semiconductor devices employed in the integrated and simplified ACCs are summarized in Table I.

The semiconductor losses in the main circuit can be estimate using the parameters defined in (7)-(9). For both iACC and sACC, the major losses are mainly due to conduction losses, since the auxiliary switches commutate under zero-current-switching (ZCS). In this way, the conduction losses can be estimated using the parameters are defined by (10)-(11). The constants of (7)-(8) and (10)-(11), summarized in Table I, were obtained using a curve fitting adjust. Due to the use of different snubber capacitors, the coefficients of (9) were obtained by experimental measurement of the losses with a LeCroy® 6030A oscilloscope, similar to the procedure carried out in [22].

$$v_{ce}(i_s) = A\, i_s^{\,B} + C \tag{7}$$

$$v_f(i_s) = A\, i_s^{\,B} + C \tag{8}$$

$$E_{off}(i_s) = A\, i_s^{\,B} + C \tag{9}$$

$$v_{ce\_ACC}(i_s) = A\, i_s^{\,B} + C \tag{10}$$

$$v_{f\_ACC}(i_s) = A\, i_s^{\,B} + C \tag{11}$$

Where:

- v_{ce} - Forward voltage drop of main IGBTs (V).
- v_f - Forward voltage drop of antiparallel diodes (V).
- E_{off} - Turn-off energy loss in one commutation of main IGBTs (mJ).
- v_{ce_ACC} - Forward voltage drop of auxiliary IGBTs (V).
- v_{f_ACC} - Forward voltage drop of auxiliary diodes (V).
- i_s - Current through the semiconductor device (A).

In addition, if a snubber capacitor is not completely discharged before the turn-on process of the switch, the remaining energy will be dissipated on the correspondent switch, and the turn-on capacitive loss (E_{on}) can be estimated by (12), where $v_{cs}(t)$ is the remaining voltage at the turn-on instant.

$$E_{on}(v_{cs}) = C_s\, v_{cs}^{\,2}(t) \tag{12}$$

The losses in the simulation period (T) at the main circuit can be calculated by (13)-(15). It is important to highlight that T/T_s must be an integer value.

TABLE I
Mathematical Model Coefficients

Parameter	Curve Fitting Constants			Circuit	Device	Test Conditions
	A	***B***	***C***			
$v_{ce}(i_s)$	0.609	0.460	0.042	Main	IGBT Module SKM50GB123D	–
$v_f(i_s)$	0.274	0.415	0.634			–
$E_{off}(i_s)$	0.105	0.599	0			C_s = 2.2 nF R_g = 9.2 Ω
	0.182	0.351	0			C_s = 3.6 nF R_g = 9.2 Ω
$v_{ce\_ACC}(i_s)$	0.120	0.716	0.726	iACC	IRG4PC40UD*	–
	0.182	0.832	0.880	sACC	IRG4BC20UD*	–
$v_{f\_ACC}(i_s)$	0.313	0.284	0.094	iACC	MUR1560*	–
	0.370	0.475	0.315	sACC	8ETH06*	–

*Discrete device.

$$P_{cnd} = \frac{1}{T}\int_0^T \left[v_{ce}(i_s)\, r(t) + v_f(i_s)\left(1 - r(t)\right)\right] \left| i_s(t) \right| dt \tag{13}$$

$$P_{on} = \frac{1}{T}\sum_{k=1}^{T/Ts} E_{on}\left(v_{cs}(k\,T_s)\right) \tag{14}$$

$$P_{off} = \frac{1}{T}\sum_{k=1}^{T/Ts} E_{off}\left(i_s(k\,T_s)\right) \tag{15}$$

Where:

- P_{cnd} - Conduction losses in one main device (W).
- $r(t)$ - (1) if the IGBT is on or (0) if the diode is on.
- P_{on} - Turn-on losses in one main device (W).
- P_{off} - Turn-off losses in one main device (W).

Furthermore, the conduction losses in the iACC and sACC can be calculated by (16) and (17), respectively, defined in Appendix B. It must be highlighted that E_{iACC} and E_{sACC} are the total energy related to the conduction losses.

$$P_{iACC} = E_{iACC}/T \tag{16}$$

$$P_{sACC} = E_{sACC}/T \tag{17}$$

Finally, the total losses (P_{tot}) are given by (18).

$$P_{tot} = 3\left(P_{cnd} + P_{on} + P_{off}\right) + P_{ACC} \tag{18}$$

Where:

- P_{ACC} - (P_{iACC}), (16), if the iACC is in analysis or (P_{sACC}), (17), if the sACC is in analysis.

D. Harmonic Content Analysis of ZVT Topologies

The indices of performance used to compare the power quality of the voltage delivered to load by iACC and sACC ZVT topologies are the total harmonic distortion (THD), the first order distortion factor (DF1) and the second order distortion factor (DF2).

The THD is obtained by the ratio of the sum of all voltage harmonics in frequencies above the fundamental to the voltage in the fundamental frequency. The DF1 represents the attenuation provided mainly by the leakage inductance in inductor motor applications. Furthermore, the DF2 represents the attenuation caused, for example, by a *LC* filter installed between inverter output and load in uninterruptible power supply applications. These performance indices are defined in [23].

IV. COMPARATIVE RESULTS

Before comparing the performance of the selected topologies with respect to the indices defined in Section III, it is important to define equivalent design parameters for both converters of Figure 2.

A. Auxiliary Circuit Design Methodology

In order to ensure the topologies of Figure 2 to operate closest to their hard-switched counterpart and present low losses in ACC, the selected resonant devices (L_x and C_s) must provide operation with a high modulation index and low current peak through the auxiliary devices. This way, the equations (1) to (5) are numerically solved and plotted in Figure 4 for both iACC and sACC ZVT topologies, using the restrictions and specifications summarized in Table II. The shaded area in the abacus of Figure 4 represents the region where all the restrictions given by (1) to (5) are complied.

Aiming to reduce the volume related to the ACCs, it is important to select small values for L_x. Furthermore, it can be seen in Figure 4 that the larger C_s is, the smaller the maximum modulation index is [Figure 4 (a) and (c)] and the larger the current peak through the ACCs is [Figure 4 (b) and (d)]. Hence, small values for C_s are preferable.

Taking into account the aforementioned constraints, the selected resonant devices and the resulting limitations of iACC and sACC ZVT topologies of Figure 2 are presented in Table III. The selected values of L_x and C_s imply similar efforts and limitations in both topologies. It is important to notice that after selecting L_x and C_s, the dead-time to be implemented, t_{d_on}, in both converters can be calculated using (2).

Additionally, a long dead-time was selected for the turn-off of main switches, t_{d_off}, in order to guarantee the almost complete discharge of the snubber capacitors for low load current levels without ACC assistance, as summarized in Table III. It must be highlighted that if t_{d_off} were not enough (when load current is near zero), there is the possibility of assisting the snubber commutation in the sACC ZVT topology. This way, from (6) a minimum value was selected for load current, which defines the activation of the sACC of Figure 2 (b) in order to discharge C_s.

B. Simulation Results

In order to compare both iACC and sACC ZVT topologies with respect to the performance indices defined in Section III, a numerical simulation of the converters for a 60 Hz output voltage is performed using Matlab® software. The simulation parameters are presented in Table II and Table III. The results are evaluated for a wide range of loads, represented by the modulation index.

TABLE II
Restrictions and Specifications for the ZVT Topologies

Parameter	Value
Output power	P_{out} = 1.5 kW
Dc bus voltage	V_{dc} = 350 V
Switching frequency	f_s = 20.04 kHz
Output line voltage (RMS)	V_{ab} = 220 V (60 Hz)
Load current peak	$i_{j(pk)}$ = 5.57 A
Minimum dead-time of the switches	$t_{d(min)}$ = 480 ns
Maximum *di/dt* of the diodes	$di/dt_{(max)}$ = 50 A/µs

TABLE III
Converter Parameters for the ZVT Topologies

Parameter	Integrated ZVT [Fig. 2 (a)]	Simplified ZVT [Fig. 2 (b)]
Auxiliary inductors	L_x = 5.65 µH	L_x = 4.40 µH
Snubber capacitors	C_s = 2.2 nF	C_s = 3.6 nF
Resultant *di/dt* of the diodes	*di/dt* = 40 A/µs	*di/dt* = 40 A/µs
Dead-time for the turn-on	t_{d_on} = 490 ns	t_{d_on} = 500 ns
Dead-time for the turn-off	t_{d_off} = 1.4 µs	t_{d_off} = 1.4 µs
Minimum load current	–	$I_{(min)}$ = 0.5 A
Boosting current	–	I_{bst} = 2.30 A

In Figure 5, the results for the losses in both topologies can be individually evaluated and compared. As can be seen in Figure 5 (a), the turn-on losses of the iACC ZVT topology are not completely eliminated due to the residual voltage on the snubber capacitors at the end of t_{d_off} for low load current levels. Additionally, the turn-off losses are substantial, basically due to the additional turn-off commutation caused by the extra SSVs. Regrettably, these extra SSVs commutate the PWM pole with the highest current, as can be inferred observing Figure 3 (b) for the conditions defined in Section III. The conduction losses observed are approximately proportional to the modulation index (or to the load current).

As can be seen in Figure 5 (b), the turn-on losses of the sACC ZVT topology are almost completely eliminated due to the assistance by the ACC in the commutation from switches to antiparallel diodes for low load current levels. It can be highlighted that this assistance and also the boosting current (constant value) contribute to increase the turn-off

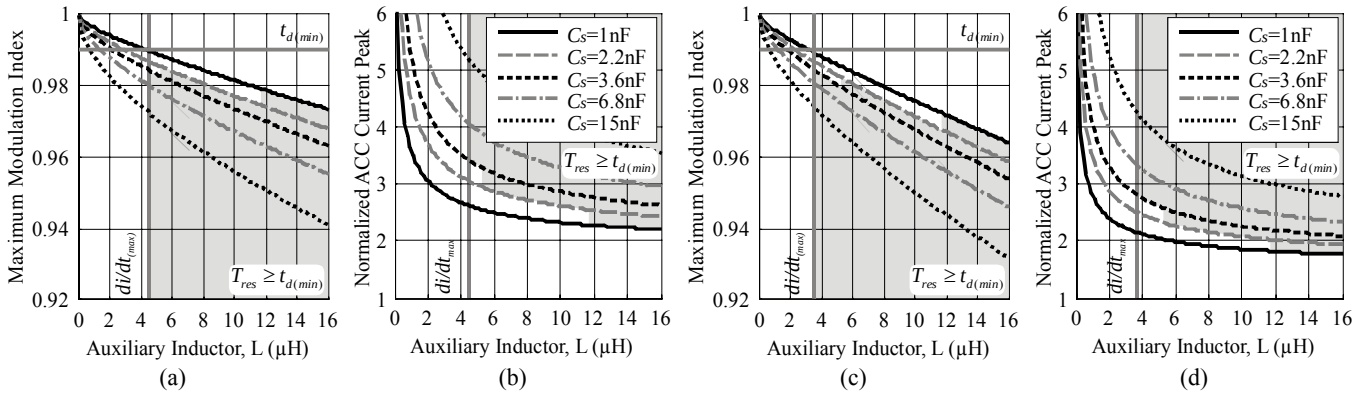


Fig. 4. Project abacus. Integrated ZVT Topology: (a) Maximum modulation index and (b) normalized resonant current peak. Simplified ZVT Topology: (c) Maximum modulation index and (d) normalized resonant current peak.

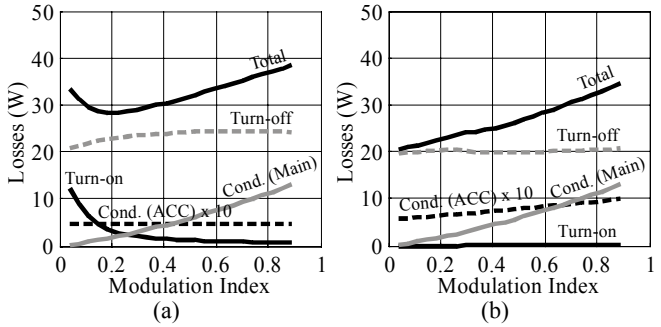


Fig. 5. Converter losses. (a) Integrated topology. (b) Simplified topology.

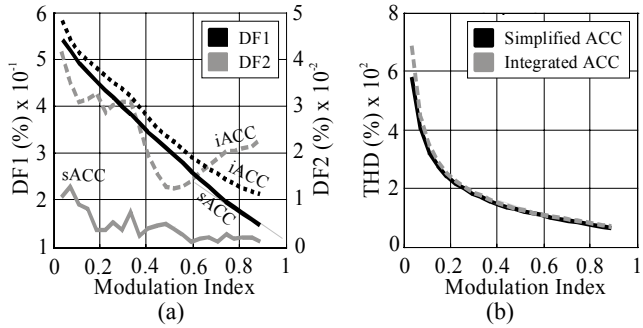


Fig. 6. Harmonic content of the voltage synthesized by the converters. (a) First and second order distortion factors. (b) Total harmonic distortion.

losses in the main switches. This can be inferred from the practically constant behavior of the turn-off losses for all modulation indices. As in the iACC ZVT topology, the conduction losses are approximately proportional to the modulation index in the simplified one. The influence of the extra SSVs in total losses of the converter is evident in Figure 5, where the total losses observed in the integrated ZVT topology are greater than in the simplified one due to the additional turn-off in the PWM pole with the highest current.

It is important to note that conduction losses in the ACCs of the sACC ZVT topology are higher than in the integrated one, as can be seen in Figure 5. This occurs because there are three independent ACCs in the sACC ZVT topology, while in the integrated topology there is only one ACC, and both ACCs process similar load current levels, as can be concluded observing the abacus of Figure 4 (b) and (d). Furthermore, the losses in the ACCs of the sACC ZVT topology increase with the load current.

The harmonic content of the output voltage synthesized by both iACC and sACC ZVT topologies can be compared in Figure 6. With respect to DF1, Figure 6 (a), it can be seen that the output voltage synthesized by the simplified topology results in a better performance when compared to the integrated one. This implies that in applications where the load provides a first order attenuation, the simplified topology results in a reduced harmonic content. Moreover, in Figure 6 (a), it is also possible to compare the DF2 performance index of both topologies. Again, the modulation scheme employed in the simplified topology results in a reduced harmonic content after the second order filter when compared to the integrated one. It means that the simplified topology has less impact on the volume of the output filter than does the integrated topology. The THD, Figure 6 (b), indicates that the simplified topology has slightly less harmonic content in the output line voltage than does the integrated topology, especially at low modulation index where the impact of the extra SSVs is more substantial. Therefore, as was expected, the modulation employing a symmetric sequence and without extra SSVs results in improved power quality of the output voltage delivered to load.

V. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, an experimental comparative analysis of the inverter efficiency and output voltage total harmonic distortion is carried out between the inverters shown in Figure 2. The prototype parameters are described in Table II. The resonant components for both integrated and simplified ACCs prototypes are designed according to Section III and summarized in Table II. The resonant inductors have been implemented with ferrite EE-20/10/5 cores. The SVM and the command strategy of main and auxiliary switches of both ZVT topologies have been implemented with a Xilinx® Spartan-3E FPGA.

A. Integrated ACC Operation

In order to verify the integrated ACC operation, the simultaneous commutations of poles "*a*", "*b*" and "*c*" are presented in Figure 7 (a)-(c). These commutations occur during the transition from $\mathbf{V_{2(ppn)}}$ to $\mathbf{V_{5(nnp)}}$, i.e., from antiparallel diodes D_1, D_3 and D_6 to switches S_2, S_4 and S_5, respectively. As shown in Figure 7 (a)-(c), the current of pole "*c*" is the highest.

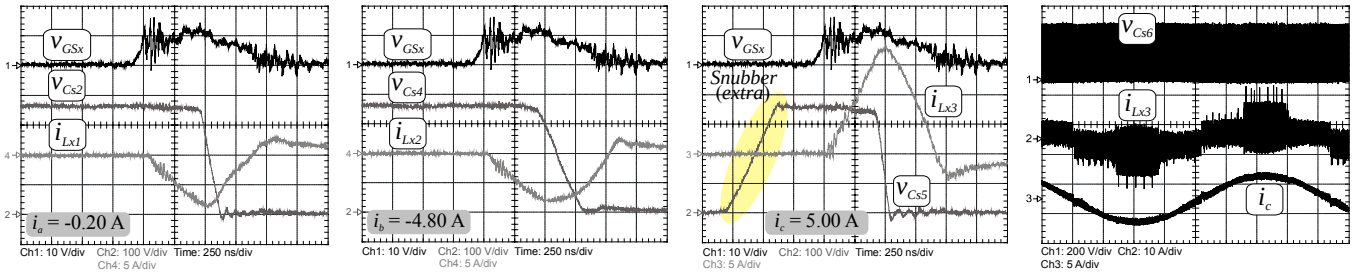
As can be seen in Figure 7 (a), the main switch S_2 is turned on after the voltage on its snubber capacitor (v_{Cs2}) reaches zero volts, ensuring the ZVS condition. The same can be observed in Figure 7 (b)-(c) with respect to S_4 and S_5. This way, the integrated ACC can provide conditions to commutate all the main switches under ZVS condition. Figure 7 (c) also demonstrates the previous turn-off of S_5 (snubber commutation) necessary to implement the extra SSV in this sector. It is important to highlight that this extra commutation occurs in the pole with the highest current.

The PWM patterns for pole "*c*" (v_{Cs6}), the current in the ACC (i_{Lx3}), and the pole current (i_c) are shown in Figure 7 (d) for the integrated ZVT topology. It can be seen that pole "*c*" presents commutations in the entire load current period due to the modulation strategy employed in the simplified ZVT topology.

B. Simplified ACC Operation

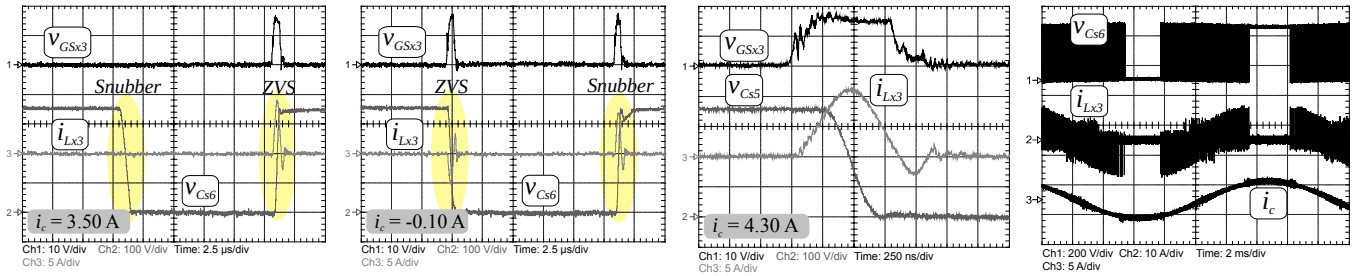
As the simplified ACCs of each PWM pole are the same, only the waveforms of pole "*c*" are presented.

Figure 8 (a) presents the experimental results for the simplified ACC when the absolute value of $i_c(t)$ is higher than I_{min}. As indicated by the gate signal of the auxiliary switch S_{x3} (v_{GSx3}), the ACC assists only the ZVS commutation (D_6 to S_5). When the absolute value of $i_c(t)$ is smaller than I_{min}, the ACC also assists the snubber commutation, as shown in Figure 8 (b). A detailed ZVS commutation from D_6 to S_5 is presented in Figure 8 (c). As can be seen, the main switch S_5 is turned on after the voltage on its snubber capacitor (v_{Cs5}) reaches zero volts, characterizing a ZVS commutation. In addition, the



(a) (b) (c) (d)

Fig. 7. Experimental waveforms for the integrated ZVT topology. Commutation from (a) D_1 to S_2; (b) D_3 to S_4; and (c) D_6 to S_5. (d) Steady-state operation.



(a) (b) (c) (d)

Fig. 8. Experimental results for the simplified ZVT topology. Commutations of pole "*c*" for (a) $|i_c(t)| > I_{(min)}$; and (b) $|i_c(t)| \le I_{(min)}$. (c) Commutation from D_6 to S_5. (d) Steady-state operation.

auxiliary switch S_{x3} is turned off after $i_{Lx3}(t)$ reaches zero, characterizing a ZCS commutation.

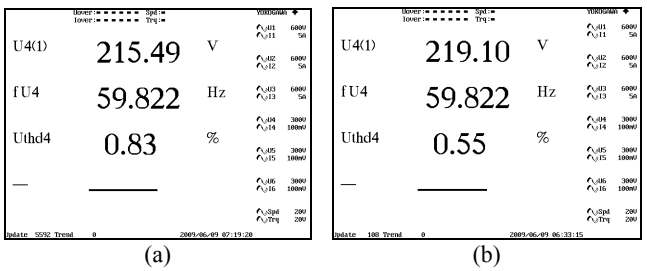
The PWM patterns for pole "*c*" (v_{Cs6}), the current in the ACC (i_{Lx3}), and the pole current (i_c) are shown in Figure 8 (d) for the simplified ZVT topology. It can be noted that the pole "*c*" does not commutate when $i_c(t)$ is 60° around its peak value.

C. Harmonic Content and Converter Efficiency

Both THD and efficiency measures were acquired with the digital power meter WT1600 (Yokogawa®).

The harmonic content of the voltage delivered to the load was evaluated by measuring the THD of the line voltage after a second order output filter with L = 3.7 mH and C = 4.0 µF per phase. The THD was 0.83% for the integrated ZVT topology [see Figure 9 (a)] and 0.55% for the simplified one [see Figure 9 (b)].

Finally, the efficiency measurements for the nominal conditions established in Table II were 97.16% for the integrated topology and 98.05% for the simplified one, as can be seen in Figure 10. Additionally, in Figure 10 are presented the estimated and measured efficiencies of both topologies. The efficiency was calculated taking into account the total losses shown in Figure 5. As can be seen, the estimated and measured results are very close for the entire load range.



(a) (b)

Fig. 9. Harmonic content of the line voltage. (a) Integrated ZVT topology. (b) Simplified ZVT topology.

VI. CONCLUSION

The comparative analysis carried out between the two selected topologies demonstrated that the technique selected to derive the ACC has significant impact on the performance of the converter. It was demonstrated that total losses observed in the iACC ZVT topology are greater than in the simplified one due to the additional turn-off in the PWM pole with the highest current caused by the necessity of extra SSVs. Additionally, it became clear that modulation strategies employing a symmetric sequence and without extra SSVs, as in sACC ZVT topologies, results in an improved power quality of the output voltage delivery to the load. On the other hand, iACC ZVT topologies can guarantee the ZVS condition for main switches of the converter with a more compact

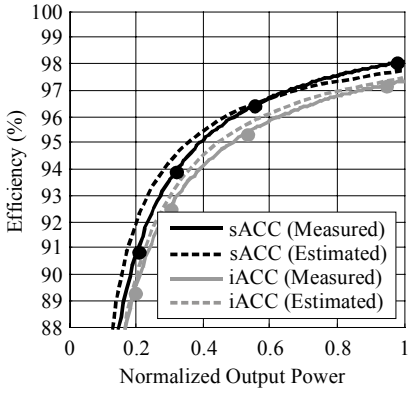


Fig. 10. Estimated and measured efficiency comparison between integrated and simplified ZVT topologies.

ACC than sACC ZVT topologies due to the utilization of the energy of one commutation to assist another one.

Therefore, when the load demands a voltage with low harmonic content, the sACC ZVT topologies are indicated. When the number of components in the auxiliary circuit is the main concern, the iACC ZVT topologies can be better.

Additionally, the comparative methodology introduced in the paper, which takes into account the global performance of the converter, can be used for other topologies of converters, enabling the engineer to select among different soft-switching solutions or to optimize the project of a given topology.

APPENDIX A
EQUATIONS EMPLOYED IN THE DESIGN ABACI

Generally speaking, it can be assumed that command signals of pole "*j*" and the current through the ACC of both analyzed topologies has the shape shown in Figure 11, where PWM_j is the modulation applied to the pole, G_{Sxj} is the auxiliary switch command signal, G_{S2j-1} is the positive main switch command signal, G_{S2j} is the negative switch command signal, $i_{Lxj}(t)$ is the current through the auxiliary inductor, I_{lin} is the current at the end of the linear charging stage, whose duration is T_{lin}, and $i_{res(pk)}$ is the resonant current peak that occurs at the middle of the resonant interval (T_{res}). It is assumed that the charging and discharging stages have approximately the same duration, defined as T_{lin}.

As can be seen in Figure 11Fig. 11, before PWM_j reaches a high level, determining the turn-off of S_{2j} (negative main switch), the auxiliary switch S_{xj} is turned on (as inferred by its command signal, G_{Sxj}) in order to diverge the load current, $i_j(t)$, from the main antiparallel diode. This way, this stage, named charging stage, whose duration is T_{lin}, limits the maximum duration of the PWM_j pulse, i.e., it limits the maximum duty-cycle ($D_{(max)}$). Hence, $D_{(max)}$ can be calculated by (19).

$$D_{(max)} = T_{lin} / T_s \tag{19}$$

After PWM_j determines the turn-off of S_{2j}, its complementary switch (S_{2j-1}) is not turned on before the end of the resonant stage, whose duration is T_{res}. Additionally, PWM_j must be at a high level during the discharging stage, whose duration is T_{lin}. Thus, the resonant and discharging stages limit the minimum duration of the PWM_j pulse, i.e., they limit the minimum duty-cycle (D_{min}). Therefore, D_{min} can be calculated by (20).

$$D_{(min)} = 1 - \left(T_{lin} + T_{res}\right) / T_s \tag{20}$$

As the line voltage is the difference between the voltages synthesized by each PWM pole, the maximum implementable modulation index can be calculated by (21), with $D_{(max)} \geq D_{(min)}$ and $0 \leq m_{(max)} \leq 1$.

$$m_{(max)} = D_{(max)} - D_{(min)} \tag{21}$$

The parameters T_{lin} and T_{res} of both iACC and sACC can be calculated according to Table IV. It is important to highlight that T_{lin} is timing variable in the sACC because it is proportional to $i_j(t)$ (see Table IV). This way, in order to determine $m_{(max)}$ for the sACC ZVT topology, the maximum value for $i_j(t)$ ($i_{j(pk)}$) must be chosen.

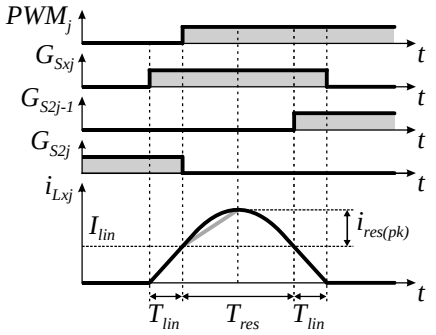


Fig. 11. General current through the ACC devices.

APPENDIX B
LOSS ANALYSIS IN THE ACCS

The auxiliary switches of the ACCs in the topologies analyzed operate under ZCS (the switches turn off only after the complete discharge of the auxiliary inductors) and hence, their switching losses may be disregarded. Therefore, the conduction losses in the ACCs of both topologies can be calculated using the current information and the forward voltage drop of the semiconductor devices [24].

With semiconductors forward voltage drop, defined in (10)-(11), and their current, approximated by (22), the conduction energy loss of the auxiliary devices is calculated.

$$i_{Lxj}(t) = \begin{cases} \dfrac{I_{lin}}{T_{lin}} t, & 0 \leq t < T_{lin} \\ \dfrac{2\, i_{res(pk)}}{T_{res}} \left(t - T_{lin}\right) + I_{lin}, & T_{lin} \leq t < T_{lin} + \dfrac{T_{res}}{2} \end{cases} \tag{22}$$

The energy loss during the conduction of an auxiliary semiconductor device (E_{dev}) in an ACC activation can be calculated by (23), where $v_{dev}(i_{Lxj})$ is the forward voltage drop of the analyzed semiconductor device, defined in (10)-(11). As the integration limits of the integral of (23) are defined taking into account the symmetry of the current waveform of Figure 11, a factor "2" is employed multiplying the entire equation (23).

$$E_{dev} = 2 \int_0^{Tlin+Tres/2} v_{dev}\left(i_{Lxj}\right) i_{Lxj}(t)\, dt \tag{23}$$

With (22) and (23), and assuming that the forward voltage drop on the device under analysis has the format defined in (10) or (11), the conduction energy loss on the considered semiconductor device during an ACC activation can be calculated by (22). It must be noted that the coefficients *A*, *B* and *C*, and the parameters T_{lin}, T_{res}, I_{lin} and i_{res_pk} of (22) are defined in Table I and Table IV, respectively. This way, upon employing (22) there is no requirement to simulate the waveform of Figure 11, minimizing the computational efforts.

A. Integrated ZVT Topology

The total conduction energy loss of iACC (E_{iACC}) of Figure 2 (a) can be calculated by (24), where E_{dev1} [defined in (25)] is the conduction energy loss of the auxiliary switch, and E_{dev2} and E_{dev3} [defined in (26) and (27), respectively] are

TABLE IV
Parameters for the Integrated and Simplified ACCs

Parameter	Integrated ACC (Extracted from [10])	Simplified ACC (Extracted from [13])
I_{lin}	$\sqrt{3}i_{j(pk)}$	$i_j(t)+I_{bst}$
T_{lin}	$3L_xI_{lin}/(2V_{dc})$	$2L_xI_{lin}/V_{dc}$
T_{res}	π/ω_n	π/ω_n
$i_{res(pk)}$	$2V_{dc}/(3Z)$	$V_{dc}/(2Z)$

the conduction energy losses in the auxiliary diodes. It can be highlighted that there are three auxiliary diodes conducting during iACC operation, where one is conducting the entire $i_{Lxj}(t)$ and the other ones are conducting $i_{Lxj}(t)/2$. Thus, the conduction energy losses of the auxiliary diodes are calculated separately, and E_{dev3} is multiplied by a factor "2" in (24). The constants and parameters employed in (25)-(27) are summarized in Table I and Table IV.

$$E_{iACC}=\sum_{k=1}^{T/Ts}\left[E_{dev1}+E_{dev2}+2E_{dev3}\right] \quad (24)$$

Where:

$$E_{dev1}=E_{dev}\left(T_{lin},T_{res},I_{lin},i_{res(pk)}\right)\Big|_{\text{IRG4PC40UD}}, \quad (25)$$

$$E_{dev2}=E_{dev}\left(T_{lin},T_{res},I_{lin},i_{res(pk)}\right)\Big|_{\text{MUR1560}}, \quad (26)$$

$$E_{dev3}=E_{dev}\left(T_{lin},T_{res},I_{lin}/2,i_{res(pk)}/2\right)\Big|_{\text{MUR1560}}. \quad (27)$$

The losses observed in the iACC are constant due to its current levels and activation times being fixed (fixing timing control), as summarized in Table IV. Finally, the total conduction loss in the iACC (P_{iACC}) averaged in the simulation period, T, can be calculated by (28).

$$P_{iACC}=E_{iACC}/T \quad (28)$$

B. Simplified ZVT Topology

The total conduction energy loss of sACC (E_{sACC}) of Figure 2 (b) can be calculated by (29), where E_{dev1} [defined in (30)] is the conduction energy loss of the auxiliary switch, and E_{dev2} [defined in (31)] is the conduction energy loss in the auxiliary diodes. It is important to note that there are two auxiliary diodes conducting the entire $i_{Lxj}(t)$ during the sACC operation. This way, E_{dev2} is multiplied by a factor "2" in (29). Furthermore, the constants and parameters employed in (30)-(31) are summarized in Table I and Table IV.

$$E_{sACC}=\sum_{j=a}^{c}\sum_{k=1}^{T/Ts}\left[E_{dev1}\left(kT_s\right)+2E_{dev2}\left(kT_s\right)\right] \quad (29)$$

Where:

$$E_{dev1}\left(kT_s\right)=E_{dev}\left(T_{lin}\left(kT_s\right),T_{res},I_{lin}\left(kT_s\right),i_{res(pk)}\right)\Big|_{\text{IRG4BC20UD}}, \quad (30)$$

$$E_{dev2}\left(kT_s\right)=E_{dev}\left(T_{lin}\left(kT_s\right),T_{res},I_{lin}\left(kT_s\right),i_{res(pk)}\right)\Big|_{\text{8ETH06}}. \quad (31)$$

It is also important to note that the losses in the sACC are timing variable, i.e., its linear charging stage duration, T_{in}, is proportional to $i_j(t)$ (variable timing control), as presented in Table IV. Therefore, E_{dev1} and E_{dev2} must be evaluated for the k-th sACC activation, as presented in (29). Finally, the total conduction loss in the sACC (P_{sACC}) averaged in the simulation period, T, can be calculated by (32).

$$P_{sACC}=E_{sACC}/T \quad (32)$$

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