ADAPTED MODULATION FOR THD PERFORMANCE IMPROVEMENT AND LOSSES REDUCTION ON MULTILEVEL INVERTERS

G.A.L. Henn[1], P.P. Praça[2], R.N.A.L. Silva[2], D.S. Oliveira Jr[2], L.H.S.C. Barreto[2], E.R.C. da Silva[3]
[1]Universidade Federal Rural do Semi-Árido / [2]Universidade Federal do Ceará / [3]Universidade Federal de Campina Grande
[2]Departamento de Engenharia Elétrica
[2] Fortaleza – CE, Brasil, 60455-760
e-mails: gustavo.henn@ufersa.edu.br, lbarreto@dee.ufc.br

***Abstract* – This paper presents an adapted carrier-based PWM modulation technique to be applied on both Neutral Point-Clamped (NPC) and Flying Capacitor (FC) structures of multilevel inverters. The proposed modulation leads to an improved performance on the output voltage THD. It also reduces the total loss dissipation across the semiconductors devices compared to other conventional carrier-based PWM modulation techniques, such as Phase-Shifted PWM (PSPWM) and Level-Shifted PWM (LSPWM). In order to demonstrate the effectiveness of the proposed technique, it was developed a three-phase, three-level, 6kW prototype for both NPC and FC topologies.**

***Keywords* - Losses Reduction, Multilevel Inverters, PWM Modulation, THD Performance.**

I. INTRODUCTION

During the last years, several topologies of multilevel inverters have attracted attention and have been largely used on industry applications, due to their capability of reducing harmonics on the output voltage, and lowering voltage stresses across the semiconductors, especially under medium and high power applications, as reactive power compensators and AC motor electric drives [1], [2].

Among the different proposed structures, three are mainly used: Neutral Point-Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB), though this last one requires isolated DC sources, which limits its application.

The NPC topology (Figure 1) was proposed in [3] and presents the following features: reduced block voltage across the switches, no isolated DC sources are required, reduced losses and EMI, and possibility of reactive power control [4]. The main drawbacks are: high number of semiconductors, voltage misbalancing between DC-link capacitors, and it is hard to be expanded to high-level systems [2].

As an alternative for the NPC, it was proposed in [5] the FC structure (Figure 2), which advantages are: fewer power semiconductors, redundant commutation stages, possibility of active and reactive power control, and easy expansion to operate with more levels [6], [7]. As drawback, it can be stated: volume and weight of the structure, due to the use of more capacitors, and the concernment with the capacitors charge and discharge dynamic process.

Artigo submetido em 29/04/2010. Primeira revisão em 05/11/2010; segunda revisão em 30/04/2011. Aceito para publicação em 04/05/2011 por recomendação do editor João Onofre P. Pinto.

However, due to the growing tendency of using more switches, and the constant concernment with the processed energy quality and losses reduction, several modulation techniques have been proposed during the last two decades.

The simplest modulation is the Phase-Shifted PWM (PSPWM), where two triangular carriers are shifted by 180º, as presented in Figure 3a, balancing naturally the voltage across the flying capacitors. However, it is only applicable on FC structures and the output voltage harmonic performance is poor, especially for low modulation index [1], [8], [9]. As an alternative, though the THD performance is also poor, the Level-Shifted PWM with Phase Opposition Disposition (LSPWM-POD) technique, presented in Figure 3b, can be applied on both NPC and FC topologies, where two carriers are mirrored from each other [8], [10].

Recently, it was proposed in [11] a carrier-based PWM method, especially designed for flying capacitor multilevel inverters, as can be observed in Figure 4a. It improves the output voltage harmonic content by applying the same amount of time on the flying capacitors charge and discharge operation over one period. Despite the good performance achieved in terms of THD, this technique can only be applied on FC structures, as it is based on the PSPWM.

Thus, in order to overcome this drawback, this paper proposes an adaptation of the technique proposed in [11], mirroring the carriers, based on the LSPWM-POD technique, as shown in Figure 4b. The main features of the proposed modulation are: can be applied on both NPC and FC topologies, improved output voltage THD performance, and losses reduction. As a drawback, it can be stated the complexity to digitally generate the carriers and the poor THD performance for very low modulation index region.

Next section presents a detailed study on the losses of each modulation applied on both topologies, while the THD measurements are presented on last section in order to proper confirm the analysis developed through the whole paper.

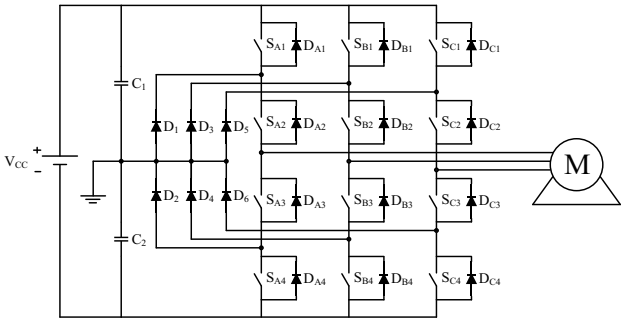

Fig. 1. Three-phase, three-level, NPC topology.

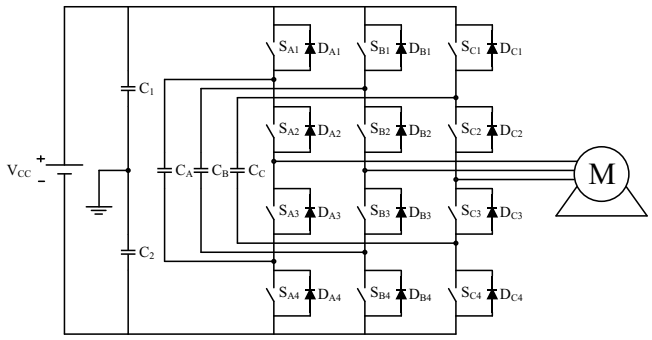

Fig. 2. Three-phase, three-level, FC topology.

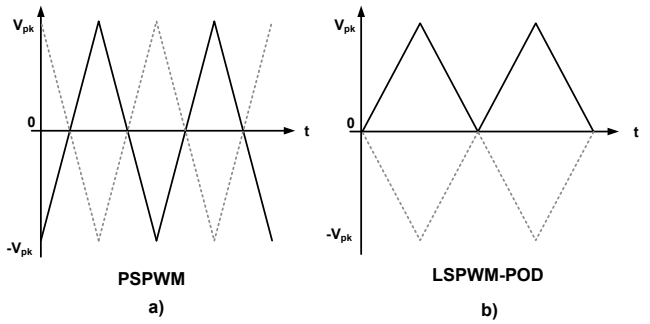

Fig. 3. Modulation techniques: a) PSPWM; b) LSPWM-POD.

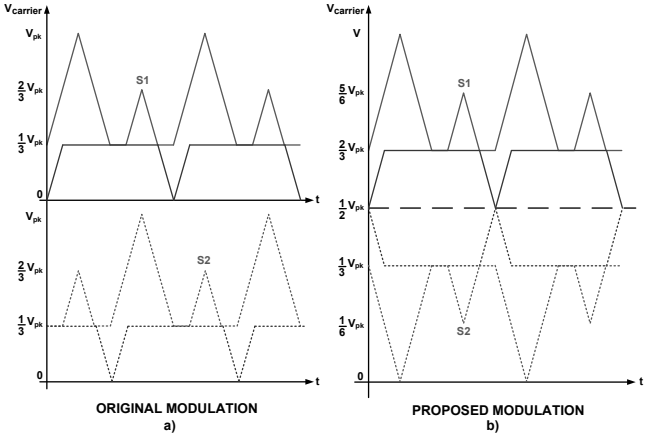

Fig. 4. a) Modulation proposed in [11]; b) Proposed Modulation.

II. LOSSES ANALISYS

A. Modulations Switching Characteristics

As can be observed in Figure 5, due to the characteristics of PSPWM, the switches are indefinitely commutating over one switching period, as the modulator is always crossing one carrier, raising the losses associated to the switches.

The same occurs with the technique proposed in [11], as it is based on PSPWM, with two modified carriers shifted by 180º. On Figure 4a, the two carriers are separated in two axis just for a better comprehension. The sine wave modulator is offseted from $0.5V_{pk}$ and varies between 0 and V_{pk}, proportionally to the modulation index. When the modulator varies between 0 and $V_{pk}/3$, the PWM pulses are generated comparing it to the low part of the carriers. If the sine wave is within the range $V_{pk}/3$ and V_{pk}, the pulses are obtained by comparing the modulator to the high part. This technique results in PWM pulses generated all over the switching period, as the modulator is always crossing one carrier.

On the other hand, Figure 6 presents the switching pulses for the LSPWM-POD. It is important to notice that, as the modulator signal crosses with only one carrier at any time, just two switches commutate over a half period, while the others remain turned-off or turned-on, depending on situation, which are both illustrated on Figure 6. On the first case, S_{x1} is commutating, while S_{x2} is always turned-on. On the other possibility, S_{x2} is switching, while S_{x1} is always turned-off. It must be noticed that, depending on the topology, S_{x3} is complementary to S_{x1}, and S_{x4} to S_{x2}, or the opposite, where x=a,b,c.

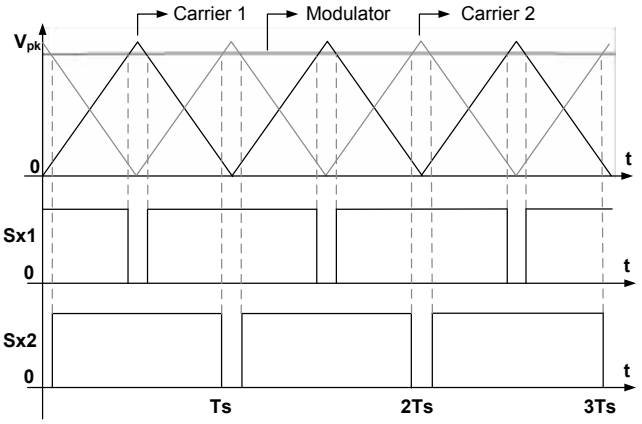

Fig. 5. Details of pulses generation on PSPWM modulation.

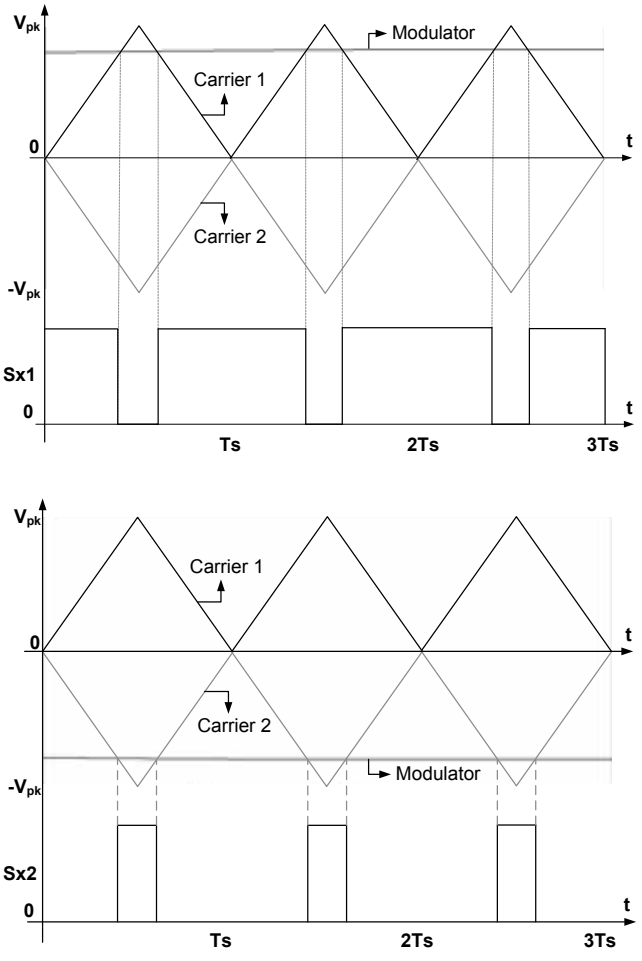

Fig. 6. Details of pulses generation on LSPWM-POD modulation.

Analyzing the two figures above, it can be stated that the losses associated to the semiconductors on the LSPWM-POD modulation are reduced if compared to the PSPWM. Thus, adapting the modulation technique proposed in [11] to the one presented on Figure 4b will also reduce the losses, as detailed on next section.

Thus, Figure 4b presents the proposed modulation, where two carriers are mirrored from each other, with one of them varying between 0 and $0.5V_{pk}$, while the other one from $0.5V_{pk}$ to V_{pk}. As on the modulation proposed in [11], the modulator signal is still offseted from $0.5V_{pk}$, and the PWM pulses generation process is analog to the original one (Figure 4a), though only two switches commutate during a half switching period, resulting in reduced switching stress across the semiconductors, as in LSPWM-POD technique. Figure 7 presents the switching pattern of the proposed technique for one inverter leg. Also, it must be noticed that those pulses are referent to the Neutral Point-Clamped topology. For the Flying Capacitor structure, the pulses from S_{x3} and S_{x4} should be shifted.

B. PSPWM Applied to FC

In order to determine the current stress on each semiconductor, it must be calculated the modulation functions for the various combinations of topology versus modulation, which can be obtained by observing the current waveforms behavior through the switches on each state changing, when comparing the modulator and the carriers.

Equations (1) and (2) present the functions for switches S_{x1} and S_{x2}, while (3) and (4), for semiconductors S_{x3} and S_{x4}, where θ_o is the load angle, M_{max} is the maximum modulation index, and $I_{o.pk}$ is the phase output peak current.

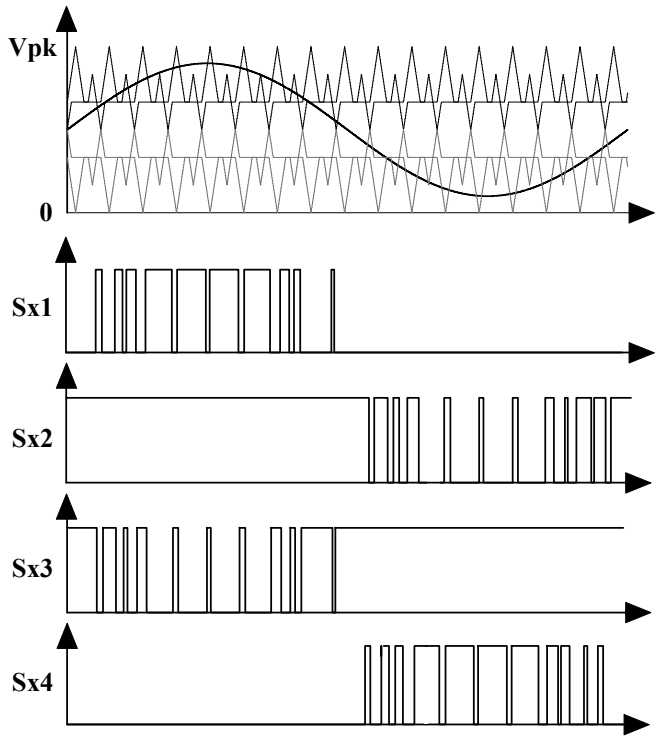

Fig. 7. Switching pattern of the proposed technique for the Neutral Point-Clamped topology.

$$\delta_{Sa1}(\omega t)=\begin{cases}0 & 0\le\omega t\le\theta_o\\ 1-\frac{1}{2}\cdot M_{\max}\cdot sin(\omega t) & \theta_o\le\omega t\le\pi\\ 1-\frac{1}{2}\cdot M_{\max}\cdot|sin(\omega t)| & \pi\le\omega t\le\pi+\theta_o\\ 0 & \pi+\theta_o\le\omega t\le 2\pi\end{cases} \quad (1)$$

$$i_o(\omega t)=I_{o.pk}\cdot sin(\omega t-\theta_o) \qquad \theta_o\le\omega t\le\pi+\theta_o \quad (2)$$

$$\delta_{Sa3}(\omega t)=\begin{cases}1-\frac{1}{2}\cdot M_{\max}\cdot sin(\omega t) & 0\le\omega t\le\theta_o\\ 0 & \theta_o\le\omega t\le\pi+\theta_o\\ 1-\frac{1}{2}\cdot M_{\max}\cdot|sin(\omega t)| & \pi+\theta_o\le\omega t\le 2\pi\end{cases} \quad (3)$$

$$i_o(\omega t)=\begin{cases}-I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o\le\omega t\le\pi\\ -I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi\le\omega t\le\pi+\theta_o\end{cases} \quad (4)$$

For the diodes, the equations below follow the same model as the switches: (5) and (6) presents the functions for diodes D_{x1} and D_{x2}, while (7) and (8), for D_{x3} and D_{x4}.

$$\delta_{Da1}(\omega t)=\begin{cases}\frac{1}{2}\cdot M_{\max}\cdot sin(\omega t) & 0\le\omega t\le\theta_o\\ 0 & \theta_o\le\omega t\le\pi+\theta_o\\ \frac{1}{2}\cdot M_{\max}\cdot|sin(\omega t)| & \pi+\theta_o\le\omega t\le 2\pi\end{cases} \quad (5)$$

$$i_o(\omega t)=\begin{cases}-I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o\le\omega t\le\pi\\ -I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi\le\omega t\le\pi+\theta_o\end{cases} \quad (6)$$

$$\delta_{Da3}(\omega t)=\begin{cases}0 & 0\le\omega t\le\theta_o \quad or \quad \pi+\theta_o\le\omega t\le 2\pi\\ \frac{1}{2}\cdot M_{\max}\cdot sin(\omega t) & \theta_o\le\omega t\le\pi\\ \frac{1}{2}\cdot M_{\max}\cdot|sin(\omega t)| & \pi\le\omega t\le\pi+\theta_o\end{cases} \quad (7)$$

$$i_o(\omega t)=\begin{cases}I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o\le\omega t\le\pi\\ I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi\le\omega t\le\pi+\theta_o\end{cases} \quad (8)$$

C. LSPWM-POD Applied to FC

Equations (9) and (10) present the functions for switch S_{x1}, while (11) and (12), for S_{x2}, for the LSPWM-POD modulation applied to FC topology.

$$\delta_{Sa1}(\omega t)=\begin{cases}0 & 0\le\omega t\le\theta_o\\ M_{\max}\cdot sin(\omega t) & \theta_o\le\omega t\le\pi\\ 0 & \pi\le\omega t\le 2\pi\end{cases} \quad (9)$$

$$i_o(\omega t)=I_{o.pk}\cdot sin(\omega t-\theta_o) \qquad \theta_o\le\omega t\le\pi \quad (10)$$

$$\delta_{Sa2}(\omega t)=\begin{cases}0 & 0\le\omega t\le\theta_o\\ 1 & \theta_o\le\omega t\le\pi\\ M_{\max}\cdot|sin(\omega t)| & \pi\le\omega t\le\pi+\theta_o\\ 0 & \pi+\theta_o\le\omega t\le 2\pi\end{cases} \quad (11)$$

$$i_o(\omega t)=\begin{cases} I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o \le \omega t \le \pi \\ I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi \le \omega t \le \pi+\theta_o \end{cases} \quad (12)$$

Though the modulation functions for switches S_{x3} and S_{x4} are different from those presented above, the resulting current stress through S_{x3} is equal to S_{x1}, while S_{x4} is equal to S_{x2}. For the diodes, the equations below follow the same model as the switches: (13) and (14) presents the functions for D_{x1}, while (15) and (16), for D_{x2}. Also, the current stress on D_{x3} is equal to D_{x1}, and D_{x4} is equal to D_{x2}.

$$\delta_{Da1}(\omega t)=\begin{cases} M_{\max}\cdot sin(\omega t) & 0 \le \omega t \le \theta_o \\ 0 & \theta_o \le \omega t \le 2\pi \end{cases} \quad (13)$$

$$i_o(\omega t)=-I_{o.pk}\cdot sin(\omega t-\theta_o) \quad 0 \le \omega t \le \theta_o \quad (14)$$

$$\delta_{Da2}(\omega t)=\begin{cases} 1 & 0 \le \omega t \le \theta_o \\ 0 & \theta_o \le \omega t \le \pi+\theta_o \\ 1-M_{\max}\cdot\left|sin(\omega t)\right| & \pi+\theta_o \le \omega t \le 2\pi \end{cases} \quad (15)$$

$$i_o(\omega t)=\begin{cases} -I_{o.pk}\cdot sin(\omega t-\theta_o) & 0 \le \omega t \le \theta_o \\ -I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi+\theta_o \le \omega t \le 2\pi \end{cases} \quad (16)$$

D. LSPWM-POD Applied to NPC

Equations (17) and (18) present the functions for switch S_{x1}, while (19) and (20), for S_{x2}, for the LSPWM-POD modulation applied to NPC topology. As observed on last case, the modulation functions for switches S_{x3} and S_{x4} are different from S_{x1} and S_{x2}, but the current stress on S_{x4} is equal to S_{x1}, and S_{x3} is equal to S_{x2}, and the same occurs with the diodes. Equations (21) and (22) present the modulation functions for D_{x1}, while (23) and (24) for D_{x2}.

$$\delta_{Sa1}(\omega t)=\begin{cases} 0 & 0 \le \omega t \le \theta_o \\ M_{\max}\cdot sin(\omega t) & \theta_o \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \quad (17)$$

$$i_o(\omega t)=I_{o.pk}\cdot sin(\omega t-\theta_o) \quad \theta_o \le \omega t \le \pi \quad (18)$$

$$\delta_{Sa2}(\omega t)=\begin{cases} 0 & 0 \le \omega t \le \theta_o \\ 1 & \theta_o \le \omega t \le \pi \\ M_{\max}\cdot\left|sin(\omega t)\right| & \pi \le \omega t \le \pi+\theta_o \\ 0 & \pi+\theta_o \le \omega t \le 2\pi \end{cases} \quad (19)$$

$$i_o(\omega t)=\begin{cases} I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o \le \omega t \le \pi \\ I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi \le \omega t \le \pi+\theta_o \end{cases} \quad (20)$$

$$\delta_{Da1}(\omega t)=\begin{cases} M_{\max}\cdot sin(\omega t) & 0 \le \omega t \le \theta_o \\ 0 & \theta_o \le \omega t \le 2\pi \end{cases} \quad (21)$$

$$i_o(\omega t)=-I_{o.pk}\cdot sin(\omega t-\theta_o) \quad 0 \le \omega t \le \theta_o \quad (22)$$

$$\delta_{Da2}(\omega t)=\begin{cases} M_{\max}\cdot sin(\omega t) & 0 \le \omega t \le \theta_o \\ 0 & \theta_o \le \omega t \le 2\pi \end{cases} \quad (23)$$

$$i_o(\omega t)=-I_{o.pk}\cdot sin(\omega t-\theta_o) \quad 0 \le \omega t \le \theta_o \quad (24)$$

The neutral clamped diodes (D1 and D2) also must have its modulation functions determined, as calculated below. Equations (25) and (26) are relative to D1. The functions of D2 are suppressed, as the current stresses through both diodes are equal to each other.

$$\delta_{D1}(\omega t)=\begin{cases} 0 & 0 \le \omega t \le \theta_o \\ M_{\max}\cdot sin(\omega t) & \theta_o \le \omega t \le \pi \\ M_{\max}\cdot\left|sin(\omega t)\right| & \pi \le \omega t \le \pi+\theta_o \\ 0 & \pi+\theta_o \le \omega t \le 2\pi \end{cases} \quad (25)$$

$$i_o(\omega t)=\begin{cases} I_{o.pk}\cdot sin(\omega t-\theta_o) & \theta_o \le \omega t \le \pi \\ I_{o.pk}\cdot sin(\omega t-\theta_o) & \pi \le \omega t \le \pi+\theta_o \end{cases} \quad (26)$$

E. Comparative Analysis

The next step is to determine the average and RMS current values using the previously calculated modulation functions, using equations below:

$$I_{Sxy_{MED}}=\frac{1}{2\pi}\cdot\int_0^{2\pi}\delta_{Sxy}(\omega t)\cdot i_o(\omega t)\cdot d(\omega t) \quad (27)$$

$$I_{Sxy_{RMS}}=\sqrt{\frac{1}{2\pi}\cdot\int_0^{2\pi}\delta_{Sxy}(\omega t)\cdot i_o(\omega t)^2\cdot d(\omega t)} \quad (28)$$

It must be noticed that, as the modulation functions of the technique proposed in [11] and the one proposed in this paper are very complex to be determined, and the simulated values for the other techniques are very close to the calculated ones, the average and RMS current values used for both modulation techniques are simulated and not calculated.

According to [12] - [14], the conduction losses across the switches and diodes can be determined using (29) and (30), where x=a,b,c, and y=1,2,3,4.

$$P_{Sxy_{COND}}=V_{TO}\cdot I_{Sxy_{MED}}+R_S\cdot I^2_{Sxy_{MED}} \quad (29)$$

$$P_{Dxy_{COND}}=V_D\cdot I_{Dxy_{MED}}+R_D\cdot I^2_{Dxy_{RMS}} \quad (30)$$

The parameters from equations above are defined as:

- V_{TO} is the variable that represents the constant parcel of the opposition to the current flow through the switch;
- R_S is the variable that characterizes the linear growth of the opposition to the current flow through the switch;
- V_D and R_D are defined similarly to V_{TO} and R_S, respectively, though with respect to the diodes.

The commutation losses across the switches are calculated from (31) to (34), while the reverse recovery losses associated to the diodes are determined using (35) and (36). The methodology to calculate all the used parameters is presented on these references.

$$W_{Sxy_{ON}}(\omega t)=k_{0_{ON}}+k_{1_{ON}}\cdot i_{Sxy}(\omega t)+k_{2_{ON}}\cdot i_{Sxy}(\omega t)^2 \quad (31)$$

$$W_{Sxy_{OFF}}(\omega t)=k_{0_{OFF}}+k_{1_{OFF}}\cdot i_{Sxy}(\omega t)+k_{2_{OFF}}\cdot i_{Sxy}(\omega t)^2 \quad (32)$$

$$P_{Sxy_{ON}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} W_{Sxy_{ON}}(\omega t) \cdot d(\omega t) \quad (33)$$

$$P_{Sxy_{OFF}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} W_{Sxy_{OFF}}(\omega t) \cdot d(\omega t) \quad (34)$$

$$W_{rr}(i_D) = V_{CC} \cdot t_{rr} \left(0.35 \cdot I_{rrN} + 0.15 \cdot \frac{i_C}{I_{CN}} \cdot I_{rrN} + i_C \right) \quad (35)$$

$$P_{rr} = \frac{1}{2\pi} \cdot \int_0^{2\pi} W_{rr}(\omega t) \cdot d(\omega t) \quad (36)$$

Table I presents the employed components to develop the NPC and FC structures, while Table II presents the calculated overall losses for one leg of the multilevel inverter with a 6kW, 70% power factor load, where it can be observed that the proposed modulation is capable to reduce losses, up to approximately 8.5% on each inverter leg.

TABLE I
Employed components specifications

Switches Sx1, …, Sx4	IGBT GP50B60PD1
Clamped Diodes D1, …, D6	MUR 860
Flying Capacitors	3 parallel 470µF/450V
DC Bus Capacitors	470µF/450V

TABLE II
Overall losses for each combination

	FC	NPC
PSPWM	146.403 W	-
LSPWM-POD	140.218 W	123.331 W
Proposed in [11]	149.435 W	-
Proposed in this paper	136.792 W	120.842 W

III. EXPERIMENTAL RESULTS

This section presents the experimental results referent to the proposed modulation. Figure 8 presents the output voltage THD of each modulation applied to FC and NPC topologies. From the THD results, it can be stated that, for a high modulation index, above 0.5, the use of the proposed modulation technique is recommended. However, for a low modulation index application, the technique proposed in [11] is the best among the ones observed.

The degradation on the THD performance noticed for low modulation indexes of the proposed modulation is due to the fact that the modulator does not cross with the high carrier region. It results in a sparse output voltage, with short-duration pulses, which affects the THD. On the contrary, the modulation proposed in [11] is capable of maintaining the duration of each pulse, even for a low modulation index.

Figures 9 and 10 present the phase and the line-to-line output voltage, respectively, where it can be observed that the proposed modulation technique produces the expected behavior of a three-phase, three-level Neutral Point Clamped multilevel inverter. The results illustrating the operation of the FC topology are omitted due to the fact that one of the main advantages of the proposed modulation is to adapt the modulation technique proposed in [11] to be applicable on the NPC topology, maintaining the improved THD performance.

Finally, Figure 11 presents the comparison between the efficiency curves from the presented techniques varying with different modulation indexes for both NPC and FC topologies. The presented efficiency curves confirm the theory developed through the whole paper, which states that the proposed modulation reduces the losses associated to the semiconductors devices.

It must be noticed that, on Figure 11a, there are just two modulation techniques curves being compared, while in Figure 11b there are four. This is due to the behavior from the NPC and FC topologies, as the NPC does not accept modulation techniques based on phase-shifted carriers.

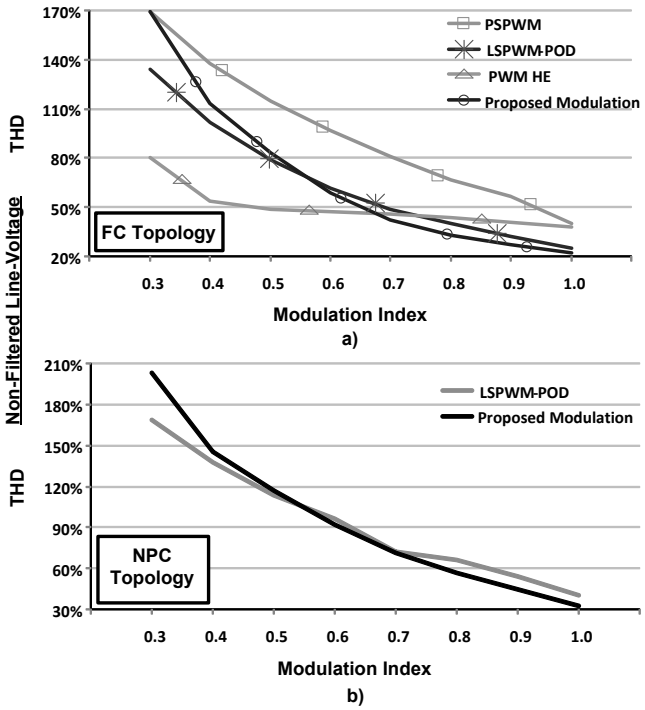

Fig. 8. Non-filtered line-voltage THD performance curves: a) FC Topology; and b) NPC Topology.

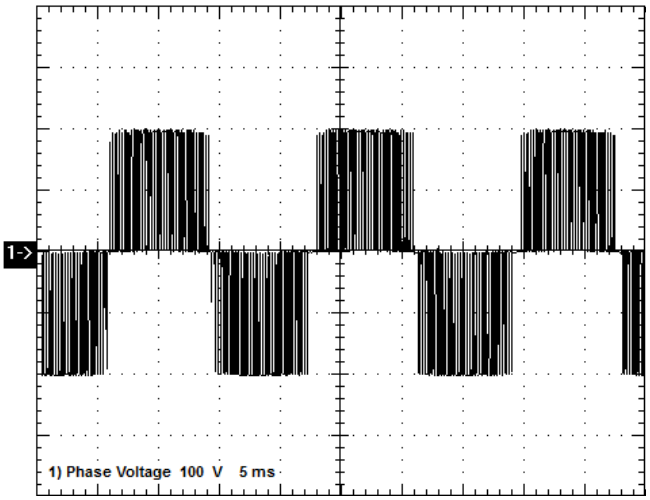

Fig. 9. Output phase voltage on the NPC converter operating with the proposed modulation.

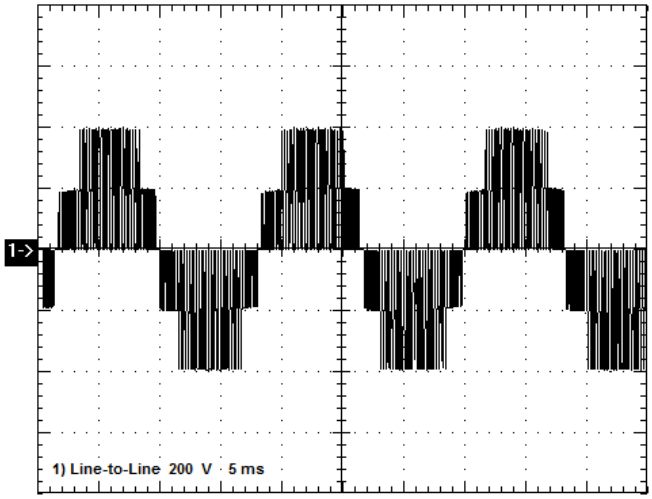

Fig. 10. Output line-to-line voltage on the NPC converter operating with the proposed modulation.

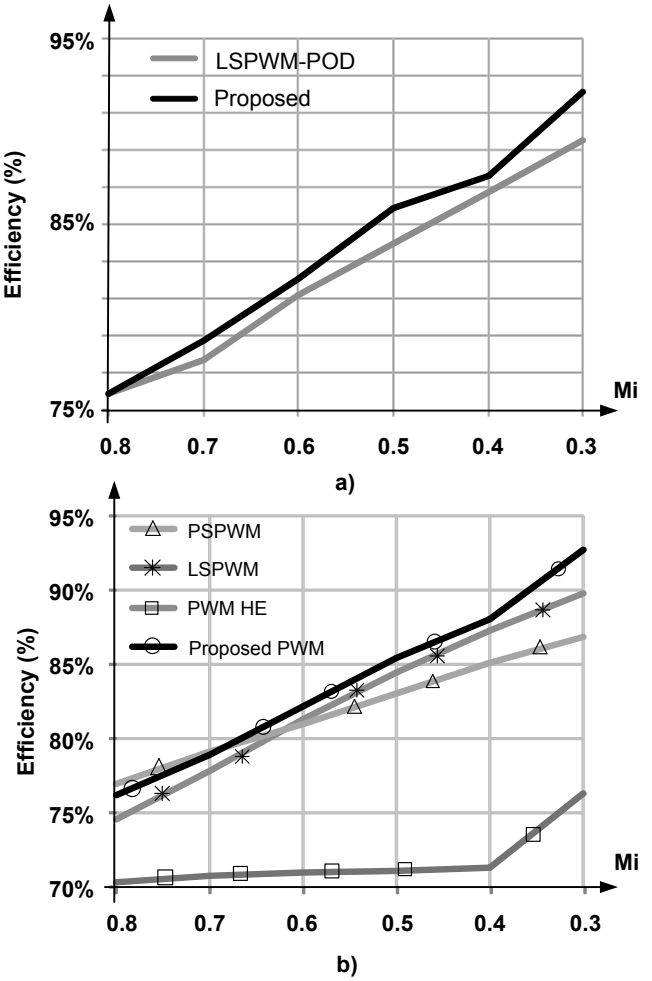

Fig. 11. Efficiency curves comparison for different modulation techniques: a) NPC topology; and b) FC topology.

IV. CONCLUSION

This paper presented a FC and a NPC three-phase, three-level inverter operating with an adapted modulation. Along with the theoretical analysis showing the characteristics, advantages, and disadvantages of each modulation (PSPWM, LSPWM-POD, modulation proposed in [11], and the one proposed in this paper), it was detailed the full losses analyses for each combination of the various modulations techniques applied on both inverter structures.

Compared to the conventional modulation techniques and the one proposed in [11], the proposed modulation improved the output voltage THD performance for high modulation index region, while the original is most suitable for low modulation indexes, which is the main drawback of the proposed topology.

In terms of losses across the semiconductors devices, the proposed modulation offers the best solution among the analyzed possibilities, raising the efficiency up to approximately 4% on low modulation index region, and 2% for high modulation indexes.

At last, the experimental waveforms of the output phase voltage and line-to-line voltage validate the whole analysis, as the characteristics of these waveforms are coherent to the expected ones on a three-phase, three-level NPC multilevel inverter. Thus, it can be stated that the proposed modulation is suitable for both NPC and FC topologies.

As future work, the authors propose the application of the proposed modulation technique on structures with more than three levels, as this possibility has been already discussed for the technique proposed in [11].

ACKNOWLEDGMENTS

The authors would like to thank to CAPES and CNPq (processes 620057/2006-8 and 620165/2008-1) for the financial support.

REFERENCES

[1] L.G. Franquelo, J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, "The Age of Multilevel Converters Arrives", *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, Jun. 2008.

[2] W.K. Lee, S.Y. Kim, J.S. Yoon, D.H. Baek, "A comparison of the carrier-based PWM techniques for voltage balance of flying capacitor in the flying capacitor multilevel inverter", *Applied Power Electronics Conference and Exposition, 2006,* vol. 1, Mar 2006.

[3] A. Nabae, I. Takahashi, H. Akagi, "A neutral-point clamped PWM inverter", *IEEE Transactions on Industry Applications*, vol. 1A-17, no. 5, pp. 518-523, Set. 1981.

[4] J.-S. Lai, F.Z. Peng, "Multilevel converters - a new breed of power converters", *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509-517.

[5] T. A. Meynard, H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters", *23rd IEEE Power Electronics Specialists Conference, PESC'92*, vol. 1, pp. 397-403, Jul. 1992.

[6] M.F. Escalante, J.-C. Vannier, A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 809-815, Ago. 2002.

[7] S. G. Lee, D. W. Kang, Y. H. Lee, D. S. Hyun, "The carrier-based PWM method for voltage balancing of flying capacitor multilevel inverter", *32nd IEEE Power Electronics Specialists Conference,* vol. 1, pp. 126-131.

[8] B.P. McGrath, D.G. Holmes, "Multicarrier PWM strategies for multilevel inverters", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858-867, Ago. 2002.
[9] Y. Liang, C.O. Nwankpa, "A power-line conditioner based on flying capacitor multilevel voltage-source converter with phase-shift SPWM", *IEEE Transactions on Industry Applications*, vol. 36, no. 4, pp. 965-971, Jul/Ago. 2000.
[10] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A new multilevel PWM method: A theoretical analysis", *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp. 497-505, Jul. 1992.
[11] H. Wang, Y. Deng, X. He, "Novel carrier-based PWM method with voltage balance for flying capacitor multilevel converters", *35th IEEE Power Electronics Specialists Conference, PESC'04*, vol. 6, pp. 4423-4427, Jun. 2004.
[12] A.L. Batschauer, A.J. Perin, S.A. Mussa, M.L. Heldwein, "Evaluation of the hybrid four-level converter employing half-bridge modules for two different modulation schemes", *25th IEEE Applied Power Electronics Conference, APEC'10*, pp. 909-914, Fev. 2010.
[13] U. Drofenik, J.W. Kolar, "A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations of power electronics systems", *International Power Electronics Conference, IPEC'05*, CD-ROM, Abr. 2005.
[14] F. Casanellas, "Losses in PWM inverters using IGBTs", *IEE Proceedings in Electric Power Applications*, vol. 141, no. 5, pp. 235-239, Set. 2004.
[15] Jing Ning; Yuyao He; "Phase-Shifted Suboptimal Pulse-Width Modulation Strategy for Multilevel Inverter," *Industrial Electronics and Applications, 2006 1ST IEEE Conference on* , vol., no., pp.1-5, 24-26 May 2006.
[16] Yu Liu; Hoon Hong; Huang, A.Q.; , "Real-Time Algorithm for Minimizing THD in Multilevel Inverters With Unequal or Varying Voltage Steps Under Staircase Modulation," *Industrial Electronics, IEEE Transactions on* , vol.56, no.6, pp.2249-2258, Jun 2009.
[17] Yu Liu; Hoon Hong; Huang, A.Q.;, "Real-Time Calculation of Switching Angles Minimizing THD for Multilevel Inverters With Step Modulation," *Industrial Electronics, IEEE Transactions on* , vol.56, no.2, pp.285-293, Feb. 2009.
[18] R.N. Ray, D. Chatterjee, S.K. Goswami, "Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique," *Power Electronics, IET*, vol.2, no.6, pp.646-652, Nov. 2009.

BIOGRAPHIES

G.A.L. Henn, was born in Fortaleza-CE, Brazil, in 1983. He received the BSc and MSc degrees in electrical engineering from Federal University of Ceará, Brazil, in 2006 and 2008, respectively. Currently is PhD candidate on power electronics in Federal University of Ceará, researcher in the Group of Power Processing and Control, and professor on the Rural Federal University of the Semi-Arid, Mossoró/RN. His interest areas include static power converters, renewable energy applications, and multilevel inverters.

P.P. Praça, was born in Fortaleza, Ceará, Brazil, in 1979. He received the BSc degree in electronic engineering from University of Fortaleza, Brazil, in 2003, and MSc degree in power electronics from Federal University of Ceará, Brazil, in 2006. Currently is PhD candidate on power electronics in Federal University of Ceará, researcher in the Group of Power Processing and Control, and assistant professor since 2008 on the same institution. His interest areas include static power converters, soft commutation, UPS applications, industrial automations, and renewable energy applications.

R.N.A.L. Silva, was born in Fortaleza, Ceará, Brazil, in 1982. She received the BSc degree in electronic engineering from University of Fortaleza, Brazil, in 2006 and MSc degree in power electronics from Federal University of Ceará, Brazil, in 2009. Currently, she is PhD candidate on electrical engineering in Federal University of Ceará and researcher in the Group of Power Processing and Control. Her interest areas include static power converters, renewable energy applications, and multilevel inverters.

D.S. Oliveira Jr., was born in Santos, São Paulo, Brazil, in 1974. He received the BSc and MSc degrees in electrical engineering from the Federal University of Uberlândia, Brazil, in 1999 and 2001, respectively, and the PhD degree from the Federal University of Santa Catarina, Brazil, in 2004. Currently, he is a researcher in the Group of Power Processing and Control and professor since 2004 on Federal University of Ceará. His interest areas include static power converters, soft commutation and renewable energy applications.

L.H.S.C. Barreto, was born in Navirai-MS, Brazil, in 1974. He received the BSc degree from the Federal University of Mato Grosso, Cuiabá-MT, Brazil, in 1997, the MSc (1999) and the PhD degree (2003) from the Federal University of Uberlândia, Uberlândia-MG. Since 2003 he is a professor of electrical engineering in the Federal University of Ceará, Fortaleza - CE, Brazil. His current research work is in the area of power electronics and renewable energy.

E.R.C. da Silva, was born in Pelotas, Brazil, in, 1942. He received the B.C.E.E. degree from the Polytechnic School of Pernambuco, Brazil, in 1965, the M.S.E.E. degree from the University of Rio de Janeiro, Brazil, in 1968, and the D.Eng. degree from the University Paul Sabatier, France, in 1972. From 1967 to 2002, he joined the staff of the Electrical Engineering Department, Federal University of Paraiba, Brazil. Since 2002 he is a professor of electrical engineering in the Federal University of Campina Grande, Brazil. In 1990, he was with COPPE, Federal University of Rio de Janeiro, and from 1990 to 1991, as Visiting Professor in the University of Wisconsin, USA. His current research work is in the area of power electronics and motor drives.