ONLINE MONITORING OF CAPACITORS IN POWER CONVERTERS

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***Abstract* – In power converters, the filtering or DC link capacitors are usually the component with shortest lifetime. With the aging, both electrolytic and film capacitors do often burst out, causing serious damages or even the destruction of the whole power stage. In this paper, a technique for diagnostic purposes is presented to estimate online, and even in real time, the aging of capacitors in different converters. The technique is based on the estimation of the capacitors equivalent series resistance (ESR) and capacitance (C). In this way, predictive maintenance can be carried out and it is possible to alarm for the capacitor replacement before failure.**

In order to demonstrate and validate the effectiveness and accuracy of the proposed technique, several power topologies are discussed, showing experimental results. An embedded prototype with the real-time estimation through a Digital Signal Processor (DSP) is constructed and presented.

***Keywords* - Power Converters, Diagnosis, Electrolytic Capacitors, Equivalent Series Resistance, Capacitance, Predictive Maintenance.**

I. INTRODUCTION

Reliability and the consequent availability of power systems is closely related to the performance of the power converters and/or the electrical machines involved in them. Early stage diagnostic tools are very useful to avoid serious drawbacks in the whole system by means of predictive maintenance. These tools lead to lower expenses caused by breakdowns, downtimes, redundant equipments and so on.

Besides the great interest on diagnostic techniques for electrical machines, in the last years an increasing interest on diagnosis of power converters has been noticed as well. The greater interest has been focused on systems involving inverters, where it is usual to deal with semiconductors failures, also calling for the need of fault-tolerant structures [1]. Regarding DC/DC converters, electrolytic capacitors are the usual choice for smoothing their output voltage. This is due to their cost, size and performance [2]. However, these components appear as the most life-limiting component, being responsible for more than 50% of their failures [3]. Therefore, suitable diagnostic techniques are needed to prevent the failure of electrolytic capacitors, especially in critical high performance applications.

The deterioration of electrolytic capacitors is mainly caused by the electrolyte evaporation as a result of temperature effects during their service life. This evaporation is reflected in some electrical parameters [4, 5]. The most affected one is the ESR, which increases largely with respect to its initial value. It has been stated by manufacturers that the life of a capacitor finishes when its ESR becomes at least two times higher than its initial value at the same temperature conditions [6]. This large variation makes that most of the techniques proposed in the literature are based only in the ESR estimation [7-20] However, also the value of the capacitance is affected when the electrolytic capacitor is degraded. Its capacitance decreases with the volume of the remaining electrolyte. As result of this process, the typical evolutions of capacitance and ESR versus time, are shown in Figure 1. According to this, it is possible to take into account the capacitance estimation, which may have a decrease of 20% with respect to its initial value [17]. This can be done with the goal of reinforcing and improving the diagnostic conclusions in electrolytic capacitors.

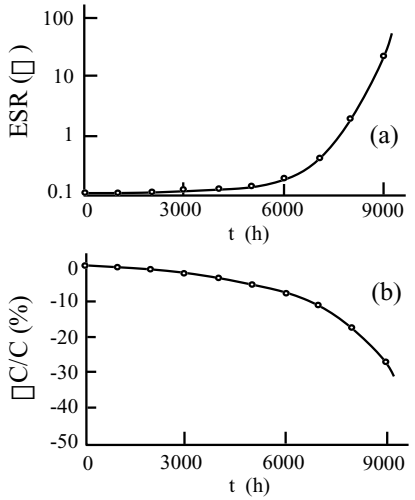

Fig. 1. ΔC/C and ESR characteristics under high-temperature load test: (a) ESR versus working hours characteristics; (b) ΔC/C versus working hours characteristics [7].

Thus, in this paper a novel technique applied for Buck and Boost based topologies of DC/DC converters is presented. The greatest advantages concerning previously published works are the estimation of both C and ESR parameters, improving the diagnostic conclusions, and also the low computation and sampling efforts linked to the adopted approach in real time, not calling for the need of powerful microprocessors and consequently resulting in a lower cost system.

II. THE ELECTROLYTIC CAPACITOR MODEL IN A BUCK CONVERTER

In the context of DC/DC conversion, the Buck converter, Figure 2, is very important and widely used. Thus, the

Manuscript received 14/10/2010; revised 15/03/2011. Accepted for publication 11/04// 2011 recommended for the special section by the editor in charge Antonio J. Marques Cardoso.

development of diagnostic tools may enhance its high performance.

It is well known that every switching DC/DC converter presents several discrete states. For the Buck converter, in the case of Continuous Conduction Mode (CCM), only the discrete states of Figures 3a and 3b occur. However, in Discontinuous Conduction Mode (DCM) also the discrete state of Figure 3c is present.

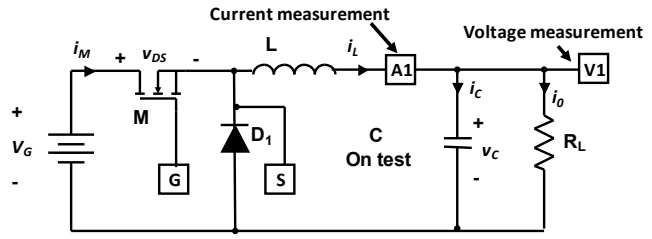

Fig. 2. DC/DC Buck converter connected to a resistive load and using an ideal capacitor.

On the other hand, in Figure 4a an equivalent circuit for the electrolytic capacitor is shown. Due to its physical design and construction, a capacitor does not only has capacitance, C, but it also has a series resistance (R_S), an inductance (ESL) and a parallel resistance ($R_{LEAKAGE}$).

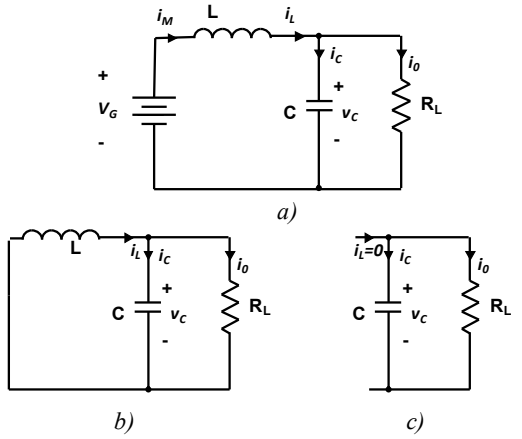

Fig. 3. DC/DC Buck Converter: (a) MOSFET conduction state, (b) non conduction state and (c) discontinuous state.

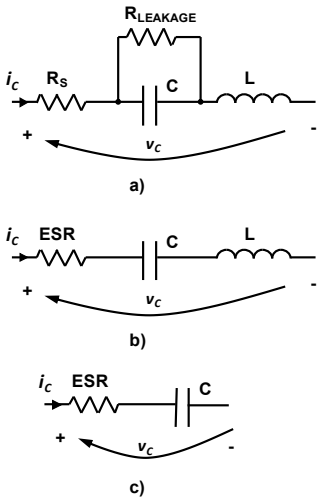

Fig. 4. Electrolytic capacitor equivalent circuit: (a) Series-Parallel configuration (b) Series configuration; (c) Simplified Series configuration where ESL is neglected.

However, this model can be simplified by joining both resistances as in Figure 4b. This is the so called Equivalent Series Resistance (ESR). This model is widely used, and it is a very good approximation when dealing with only one single frequency value, since the ESR is frequency dependent. Although a rule of thumb for evaluating the ESL value is proposed in [21], in Buck converters the model of Figure 4c can be used. This simplification can be inferred if (1), which describes the equivalent model represented in Figure 4b, is analyzed in the environment of a Buck converter.

$$\frac{dv_C(t)}{dt} = ESR \cdot \frac{di_C(t)}{dt} + ESL \cdot \frac{d^2 i_C(t)}{dt^2} + \frac{1}{C} \cdot i_C(t) \quad (1)$$

In (1), i_C and v_C represent, respectively, the current and voltage in the device (real capacitor).

From the analysis of Figure 3a, and 3b through Kirchhoff's law, it is possible to conclude that the current through the capacitor is almost linear. In fact, it is the result of the linear inductor current less the quasi-constant load current. Thus, its second derivative can be neglected in (1). In this way, (2) is obtained.

$$\frac{dv_C(t)}{dt} = ESR \cdot \frac{di_C(t)}{dt} + \frac{1}{C} \cdot i_C(t) \quad (2)$$

In DCM, when the inductor current is null, Figure 3c, the current through the capacitor is the same current flowing through the load, and so, it is approximately constant. Consequently, its first and second derivatives can be neglected in (1). Thus, (3) is obtained.

$$\frac{dv_C(t)}{dt} = \frac{1}{C} \cdot i_C(t) \quad (3)$$

In fact, the only effect of ESL on the capacitor voltage is only noticed in the boundaries between the states of Figure 3, when the derivative of i_L, and therefore of i_C present a large change. If necessary, ESL can be estimated by measuring the capacitor voltage step in these boundaries. In summary, it can be concluded that the ESL has almost no effect in the Buck converter output voltage waveform during the different states of Figure 3, and it can be neglected in the capacitor model as shown in Figure 4c during the just mentioned states.

In order to estimate the passive components in Buck converters, the inductor current and the capacitor voltage will be sampled simultaneously throughout the switching period, Figure 2. Regarding (2), sampling the capacitor current would be simpler for the method. However, the inductor current is usually sampled for control purposes and a current sensor in series with the filtering capacitor is normally a strong lay-out problem, since in large power applications the capacitor is directly screwed in the bus-bar. The sampled inductor current, whose shape is known, will determine the beginning and the end of every period. With the data of every period, average values for inductor current and the output voltage are computed. This way, (4) can be used to estimate the resistive load.

$$R_L = \frac{v_C^{avg}}{i_L^{avg}} \quad (4)$$

Once R_L is known, capacitor current can be computed as in (5), avoiding its sampling.

$$i_C(t) = i_L(t) - i_0(t) = i_L(t) - \frac{v_C(t)}{R_L} \quad (5)$$

III. A NOVEL TECHNIQUE FOR ONLINE ESTIMATION OF THE CAPACITANCE AND THE ESR

For estimating the capacitor parameters, the starting point is (2), which can be applied if the current and the voltage of the capacitor are known. The capacitance and the ESR must be calculated simultaneously according the following steps:

1.- The inductor current and the capacitor voltage are sampled simultaneously during several switching periods, obtaining $\left\langle \widehat{i_L} \right\rangle_j$ and $\left\langle \widehat{v_C} \right\rangle_j$. Analyzing these data it is possible to distinguish where the inductor current is increasing (Figure 3a), decreasing (Figure 3b) or being null (Figure 3c). Once the inductor current data have been divided in different sets (data related to states of Figure 3a, Fig 3b or Figure 3c.), only the data from two switching periods are selected for further use.

2.- It is well known that the inductor current is linear during all the three states. Therefore, it is possible to approximate each stretch of current by the equation of a straight line. On the other hand, to approximate the capacitor voltage accurately, a second degree polynomial is used for every state of the converter. These approximations are done by means of the Least Mean Squares (LMS) algorithm [11].

In all cases, to calculate the polynomial coefficients, the data sampled near the beginning and the end of each stretch are not used before applying LMS in order to eliminate switching noise.

3.- Once the current of two periods has been approximated by lines, it is easy to calculate the intersection of these lines. Thus, the maximum and minimum value of the current and the initial and final instant of one period are obtained. At this moment, the data from the sampled series are substituted by calculated data, $\langle i_L \rangle_j$ and $\langle v_C \rangle_j$. These new sets of data are free from switching noise and sampling error.

4.- In (6) the load is estimated according to (4), where 'n' is the number of sampled and recalculated data per period:

$$R_L = \frac{v_C^{avg}}{i_L^{avg}} = \frac{\frac{1}{n} \cdot \sum_{j=0}^{n-1} \langle v_C \rangle_j}{\frac{1}{n} \cdot \sum_{j=0}^{n-1} \langle i_L \rangle_j} = \frac{\sum_{j=0}^{n-1} \langle v_C \rangle_j}{\sum_{j=0}^{n-1} \langle i_L \rangle_j} \quad (6)$$

5.- Then, regarding (5), the value of the capacitor current for each sampling instant is obtained from (7) and a polynomial function for $i_C(t)$ can be obtained for every state of the converter.

$$\langle i_C \rangle_j = \langle i_L \rangle_j - \frac{\langle v_C \rangle_j}{R_L} \quad (7)$$

6.- One of the greatest advantages of the proposed method is that the derivatives of the waveforms are obtained with a surprising simplicity. Once the coefficients of the fitted polynomial functions are available, the derivatives are directly obtained through very simple derivation. Calculating the derivatives from simple polynomial functions is very useful from the point of view of implementing the online technique with simple hardware. It allows working with low number of samples per period, reducing the required sampling frequency and maintaining the accuracy of the results. This way, $\left\langle \frac{d\, i_C}{dt} \right\rangle_j$, $\left\langle \frac{d\, v_C}{dt} \right\rangle_j$ can be obtained for one period.

7.- Once an expression for the derivatives is also available, ESR and C are the only not known parameters of (2). They can be calculated by several means. If LMS algorithm is used, (8) and (9) are encountered. Both of them are easy to compute, contrarily to other methods involving more complex calculations [16-19].

$$ESR = \frac{\sum_{j=0}^{n-1} \left(\left\langle \frac{dv_C}{dt} \right\rangle_j \right) \cdot \sum_{j=0}^{n-1} \langle i_C \rangle_j^2 - \sum_{j=0}^{n-1} \left(\left\langle \frac{dv_C}{dt} \right\rangle_j \cdot \langle i_C \rangle_j \right) \cdot \sum_{j=0}^{n-1} \langle i_C \rangle_j}{\sum_{j=0}^{n-1} \left(\left\langle \frac{di_C}{dt} \right\rangle_j \right) \cdot \sum_{j=0}^{n-1} \langle i_C \rangle_j^2 - \sum_{j=0}^{n-1} \left(\left\langle \frac{di_C}{dt} \right\rangle_j \cdot \langle i_C \rangle_j \right) \cdot \sum_{j=0}^{n-1} \langle i_C \rangle_j} \quad (8)$$

$$C = \frac{R_L}{R_L + ESR} \frac{\sum_{j=0}^{n-1} \langle i_C \rangle_j^2 - \frac{1}{n} \cdot \left(\sum_{j=0}^{n-1} \langle i_C \rangle_j \right)^2}{\sum_{j=0}^{n-1} \left(\left\langle \frac{dv_C}{dt} \right\rangle_j \cdot \langle i_C \rangle_j \right) - \frac{1}{n} \cdot \sum_{j=0}^{n-1} \left\langle \frac{dv_C}{dt} \right\rangle_j \cdot \sum_{j=0}^{n-1} \langle i_C \rangle_j} \quad (9)$$

8.- It is also possible to obtain an estimation for the inductance of the buck converter throughout the use of (10). In the state of Figure 3b the current of the inductor is measured. If the voltage of the diode is measured the voltage of the inductor would be also known. Knowing the current and voltage of an inductor, its inductance can be also calculated using LMS.

$$L = \frac{\sum_{j=0}^{n-1} \left(\left\langle \frac{d\, i_L}{dt} \right\rangle_j \cdot \left(\langle v_C \rangle_j - \langle v_{diode} \rangle_j \right) \right)}{\sum_{j=0}^{n-1} \left(\left\langle \frac{d\, i_L}{dt} \right\rangle_j \right)^2} \quad (10)$$

The same behavior of the buck converter is observed in other DC/DC topologies such as the forward, push-pull, half bridge and full bridge converters. Therefore, the here introduced approach can also be applied to them. On the other hand, the boost converter operates differently and deserves its own mathematical approach as it will be described in the next section.

IV. THE BOOST CONVERTER

In the context of DC/DC conversion, the Boost converter shown in Figure 5 is also very important and widely used. For instance, it is possible to find it in high performance applications such as photovoltaic systems [22], or AC/DC converters with Power Factor Correction (PFC) [23]. Thus, it

is very important the development of diagnostic tools in order to keep its high performance.

For the Boost converter, depending on the operation mode two (CCM) or three (DCM) different discrete states are observed. In the case of CCM, only the discrete states of Figs. 6a and 6b occur. However, in DCM also the discrete state of Figure 6c is present.

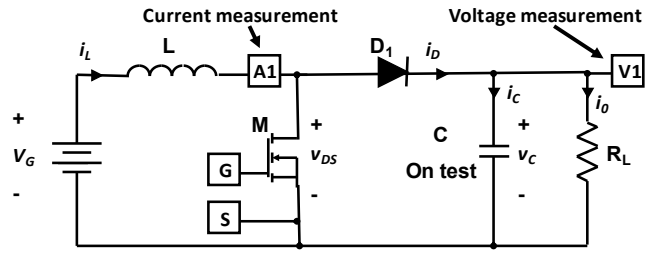

Fig. 5. DC/DC Boost converter connected to a resistive load and using and ideal capacitor.

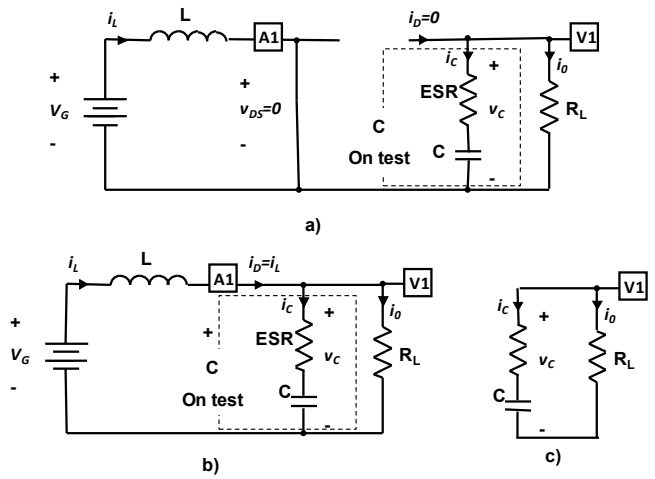

Fig. 6. Boost Converter: (a) conduction state, (b) non conduction state and (c) discontinuous state.

Considering the conduction state of Figure 6a, the following equations can be written:

$$\frac{di_L(t)}{dt} = \frac{V_G}{L} \tag{11}$$

$$\frac{dv_C(t)}{dt} = \frac{-1}{(ESR + R_L)\cdot C}\cdot v_C(t) \tag{12}$$

During the non conduction state (Figure 6b), the equations are now as follows:

$$\frac{di_L(t)}{dt} = \frac{(V_G - v_C(t))}{L} \tag{13}$$

$$\frac{dv_C(t)}{dt} = \frac{V_G \cdot ESR \cdot R_L}{(ESR + R_L)\cdot L} + \frac{R_L}{(ESR + R_L)\cdot C}\cdot i_L(t) + \left(\frac{-1}{(ESR + R_L)\cdot C} - \frac{ESR \cdot R_L}{(ESR + R_L)\cdot L}\right)\cdot v_C(t) \tag{14}$$

Finally, if the converter operates in discontinuous mode, Figure 6c, (12) is again valid.

In Figure 6 the capacitor has been modeled by its capacitance in series with its ESR, as shown in Figure 4c. This simplification can be inferred again because the current through the capacitor can be considered linear, being null its second derivative in (1), as in the case of Buck converters. In fact, during the conduction and the discontinuous states the current through the capacitor is the same that flows through the load, being also approximately constant. Consequently, its first and second derivatives can be neglected in (1), which can be simplified to (15). The same conclusion is true for the discontinuous state, Figure 6c.

$$\frac{dv_C(t)}{dt} = \frac{1}{C}\cdot i_C(t) \tag{15}$$

Then, from the analysis of Figure 6b through Kirchhoff's law, it is possible to conclude that during the non-conduction state, the current through the capacitor is almost linear. In fact, it is the result of the linear inductor current less the quasi-constant load current. In this way, (16) is obtained.

$$\frac{dv_C(t)}{dt} = ESR\cdot\frac{di_C(t)}{dt} + \frac{1}{C}\cdot i_C(t) \tag{16}$$

Coming back to (15), it can be deduced that the effect of ESR during the conduction period can be definitely neglected in the capacitor voltage derivative. This result is rather logic because the load is hiding the effect of the ESR, since they are connected in series and the later is small enough. Therefore, differently from the Buck converter, with the Boost topology it is possible to evaluate the capacitor parameters separately, each one in a different discrete state. It means that the capacitance can be evaluated during the conduction state of the switch, when the ESR effect is hidden by the load, and afterwards, knowing C, the ESR can be estimated during the non-conduction state of the switch.

Again, as done for the Buck converters:

1.- the inductor current and the capacitor voltage are sampled: $\langle \widehat{i}_L \rangle_j$ and $\langle \widehat{v}_C \rangle_j$.

2.- Now, from the shape of the current it is possible to identify the active switch gate signal by a very simple analysis, avoiding any extra sensor.

3.- The sampled current and voltage signals are fitted by a polynomial function of suitable order: second order for the voltage in Figure 6b conditions and first order otherwise.

4.- The sampled data are substituted by their fitted polynomial functions, $\langle i_L \rangle_j$ - $\langle v_C \rangle_j$

5.- The capacitor current is obtained. With this purpose, during the conduction state and the discontinuous state (17) is used, and for the non-conduction state (18) is used instead. In both cases i_0 represents the output current.

$$i_C(t) = -i_0(t) = -\frac{v_C(t)}{R_L} \tag{17}$$

$$i_C(t) = i_L(t) - i_0(t) = i_L(t) - \frac{v_C(t)}{R_L}. \tag{18}$$

In order to obtain an estimation of R_L and to compute (17) and (18), (19) and (20) must be previously used. In fact, it is well known that it is possible to obtain for each different operating mode (DCM or CCM), an average state model where the different discrete states are combined in one single system of differential equations representing the average behavior of the considered converter. From these models it is possible to obtain, under steady state condition and considering a resistive load, some relationships between the state-variables average values. For the case of the Boost

converter the following relationships are respectively found, for CCM and DCM operating modes:

$$R_L = \frac{v_C^{avg}}{i_L^{avg} \cdot D_{off}} \tag{19}$$

$$R_L = \frac{(D_{on} + D_{off}) \cdot v_C^{avg}}{i_L^{avg} \cdot D_{off}} \tag{20}$$

where D_{on}, called duty cycle, is linked to the period when the inductor is being charged (Figure 6a) and D_{off} is linked to the period when the inductor is being discharged (Figure 6b). In DCM, D_{off} lasts until the moment when there is no more current flowing through the inductor.

6.- Once the appropriate current and voltage derivatives are computed, LMS algorithm is used to obtain an estimation of C from (15). This estimation is used in (16) to compute ESR always through LMS.

This analysis can be straightforward extended to Buck-Boost and Flyback topologies. Also DC link capacitors can benefit from it, if the capacitor is discharged through a rheostat when switching off the converter [24]. In this situation its capacitance can be evaluated from (15). Moreover, as the capacitance is evaluated separately from ESR this method can be extended to film capacitors, where ESR is extremely low and difficult to measure even with accurate instruments.

V. REAL-TIME IMPLEMENTATION OF THE DIAGNOSTIC TECHNIQUE USING A DSP

This method is simple enough to be implemented in a low cost system based on a DSP. The current is acquired with a Hall Effect sensor and its level is adapted with one operational amplifier (OA) to the range of the DSP analogical inputs. The output voltage is treated as well by means of OAs to extract the ripple and amplify it to suitable levels. In both cases, the bandwidth of the OAs serves as low pass filter. The sampling of the waveforms is done by means of the internal A/D converter of a dsPIC from Microchip (dsPIC33F family). This device was selected due to its good compromise between performance and cost. Two internal sample and hold acquire both waveforms simultaneously, being converted to digital sequentially. For this configuration, the maximum sampling frequency per channel is 500 kHz. With this limit, the whole system has been tested up to a switching frequency of 20 kHz, meaning 25 samples per period, always providing a good performance.

As the inductor value is not needed for diagnostic purposes in electrolytic capacitors, in Buck converters the diode voltage is not sampled, but reasonably approximated by a constant. The value obtained with (10) is in this case only an approximation.

Once the signals have been acquired the capacitance and the ESR of the component are evaluated by the algorithm described before. The process can be repeated almost instantaneously for different switching cycles, having several measurements of C and ESR per second. The LCD display of the development system has been used to show the moving average of every 64 measurements. For an industrial product the dsPIC development board is not necessary, but only the dsPIC itself, dramatically reducing the size of Figure 7. In a final assemble, the resulting instrumentation, four OAs and a DSP, does not significantly affect the cost and the size of a large power converter.

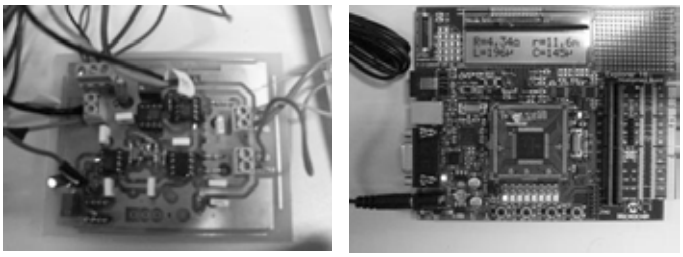

Fig. 7. Experimental prototype. Detail of the instrumentation and the DSP development board with measured data on the screen. The instrumentation and the DSP itself can be integrated in the power stage as small size additional hardware.

VI. EXPERIMENTAL RESULTS FOR A BUCK CONVERTER

Tables I-III show some experimental results from the embedded system of Figure 7 for two different capacitors and loads in a Buck converter. The results obtained are very stable and repetitive in good agreement with measurements performed by a high accuracy impedance analyzer (model Agilent 4294A), also given in the tables. As can be observed, they reproduce well the temperature influence in the capacitor parameters. In fact, lower duty cycle implies higher current ripple in the capacitor and therefore an increment of its temperature. This fact leads to a better conductivity of the electrolyte and hence lower ESR and larger capacitance.

TABLE I
Estimated Parameters Using a DSPic

Capacitor 1. Nominal Capacity 220µF – 63V. R load=2.33Ω			
Impedance analyzer estimation. ESR=92.2mΩ, C=192.2 µF			
Duty cycle	R load	ESR (mΩ)	C (µF)
0.3	2.30	81.7	195.4
0.4	2.37	85	193.1
0.5	2.37	92.5	192.2
0.6	2.38	95.4	189.8
0.7	2.38	97.4	189.7

TABLE II
Estimated Parameters Using a DSPic

Capacitor 2. Nominal Capacity 220µF – 35V. R load=2.33Ω			
Impedance analyzer estimation. ESR=111.4mΩ, C=188 µF			
Duty cycle	R load	ESR (mΩ)	C (µF)
0.3	2.26	100.2	204.7
0.4	2.34	105.5	199.4
0.5	2.35	109.6	198.4
0.6	2.36	112.2	196.3
0.7	2.37	114.7	197.3

TABLE III
Estimated Parameters Using a DSPic

Capacitor 2. Nominal Capacity 220µF – 35V. R load=4.73Ω			
Impedance analyzer estimation. ESR=111.4mΩ, C=188 µF			
Duty cycle	R load	ESR (mΩ)	C (µF)
0.3	4.59	100	207.9
0.4	4.73	104	200
0.5	4.75	110.1	198.4
0.6	4.76	114.4	198.1
0.7	4.71	116.4	197.3

Tables II and III have been conceived for the same capacitor under different loads. The measured current in the inductor is different. However, the current in the capacitor should be the same in both cases if the duty cycle is the same. So, ESR and C should match for the same duty cycle. The values of both tables are quite similar (error < 1.5%) and in very good agreement with the impedance analyzer estimation. As shown in Figure 1, at the capacitor end of life, a decrement of at least 20% in the capacitance value is expected. At the same time the ESR of the capacitor should increase to even ten times its initial value. Regarding the accuracy of these experimental results it is possible to affirm that this end of life could be foreseen in advance, and the replacement of the component can be alerted.

In Figure 8, it can be observed the difference among 320 different measurements of both parameters, C and ESR, as provided by the embedded system. Every single measurement and the moving average of the last 64 measurements are represented for each parameter. The average is considered as the final estimation given by the system, and it is an almost constant and stable value. This reliability is possible because the distribution of the single measurements is very narrow around the final value, as shown in Figure 9 for other measurements set. For all the measurements done, the deviation is so small that more than 90% of the real time estimations always differ of less than 3% from the final average value.

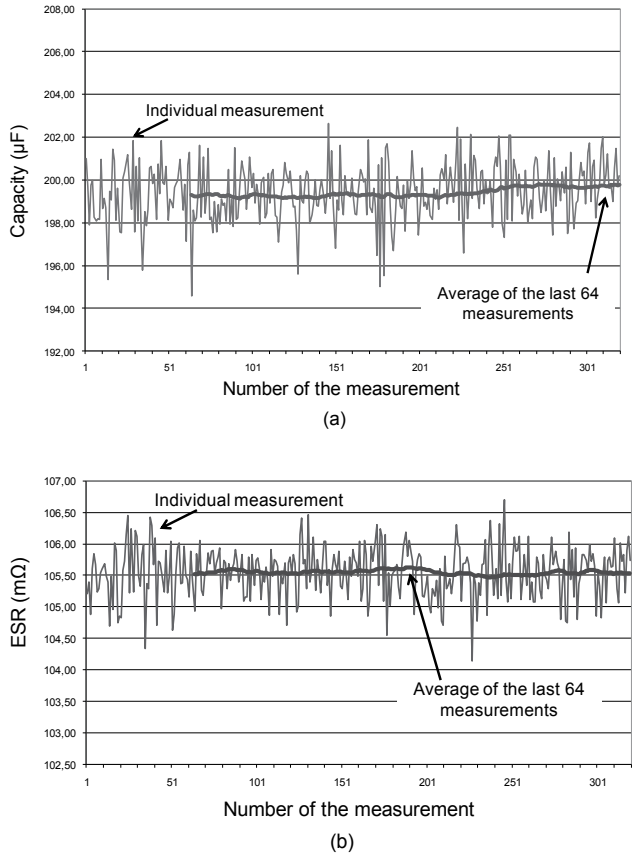

Fig. 8. (a) Capacitance and (b) ESR real time estimations for the conditions at Table II when the duty cycle in the converter is 0.4. The higher difference between any measurement and the moving average is below 3%.

VII. EXPERIMENTAL RESULTS FOR A BOOST CONVERTER

The method deduced for boost converters has also been experimentally tested. The diagnostic tool has been implemented in a DSP embedded system. Again the results obtained are very stable and repetitive. They reproduce well the temperature changes in the capacitor parameters, and are in good agreement with the impedance analyzer results as seen in Tables IV and V. The measurements with the impedance analyzer are done with no losses in the capacitor, meaning lower C due to temperature effects.

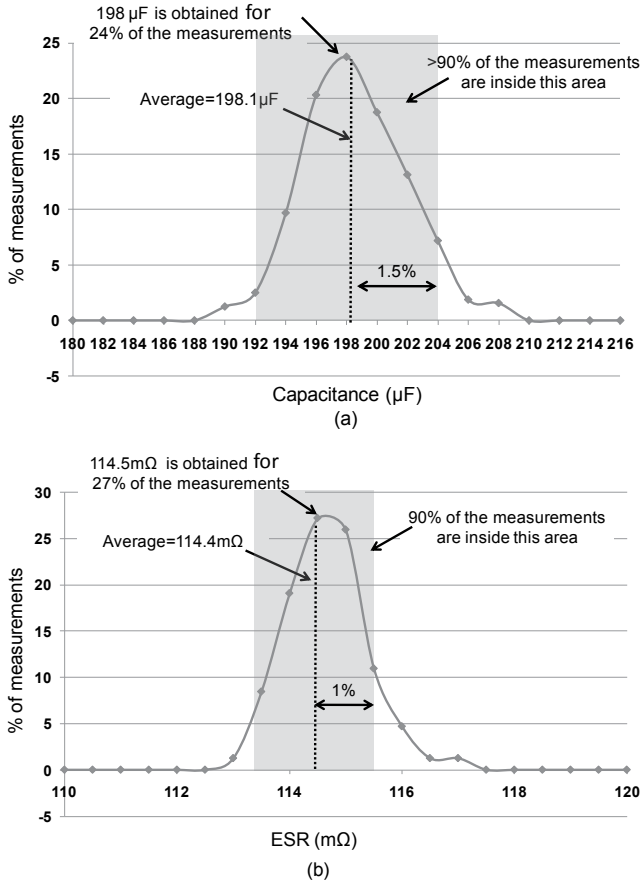

Fig. 9. (a) Capacitance and (b) ESR real time estimations for the conditions at Table III when the duty cycle in the converter is 0.6. More than 90% of the individual measurements differ less than 1.5% from the average value of them all.

The difference of every single measurement from the final (average) value is always very small: in more than 90% of the measurements, the difference between individual real time measurements and final average value is lower than 2%. A typical distribution of measurements is shown in Figure 10.

TABLE IV
Estimated Parameters Using a DSPic

Capacitor 1. Nominal Capacity 150µF – 35V		
Impedance analyzer estimation. ESR=119.9mΩ, C=137.6 µF, ESL=12.9nH		
Duty cycle	ESR (mΩ)	C (µF)
0.4	110	142
0.5	101	145
0.6	94	146

TABLE V
Estimated Parameters Using a DSPic

Capacitor 2. Nominal Capacity 470µF – 50V		
Impedance analyzer estimation. ESR=92mΩ, C=383.9 µF, ESL=31.5nH		
Duty cycle	ESR (mΩ)	C (µF)
0.4	98.4	394
0.5	92	402
0.6	88.4	405

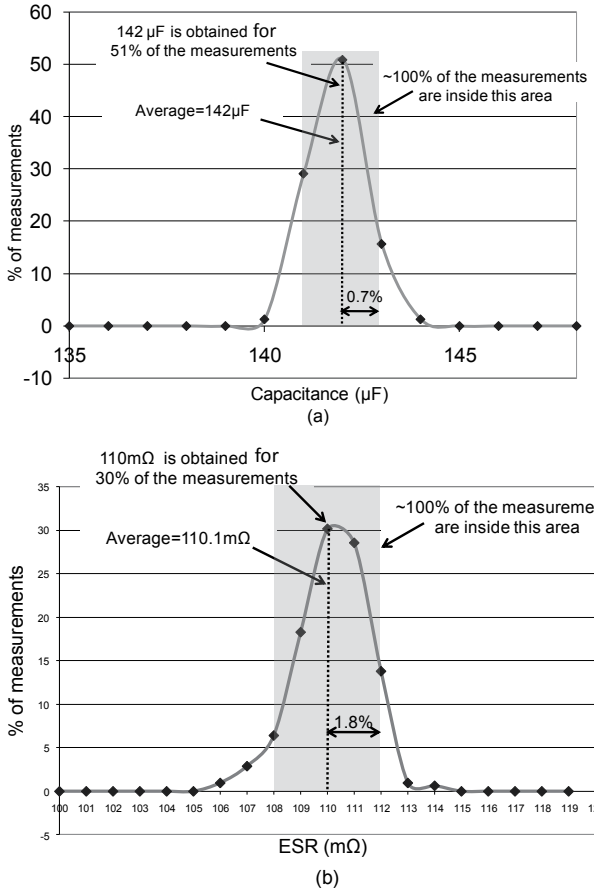

Fig. 10. (a) Capacitance and (b) ESR distribution of the real estimations for the 150 µF capacitor (D_{on}=0.4).

The same method has been also used to measure film capacitors. The device under test has a nominal capacitance value of 125 µF, and the value of its ESR provided by the manufacturer is 650 µΩ. When measured with an impedance analyzer Agilent 4294A the value obtained for its capacitance is 124.4 µF. However, it was impossible to measure accurately such a low ESR. Values below 5 mΩ have been obtained.

The capacitance and ESR measurements with the embedded system when working as filtering capacitor of a boost converter are shown in Figure 11. The capacitance measurement has been also very repetitive and stable, and the error is around 1% (Figure 11a). On the other hand the results for the ESR are quite similar to the ones obtained with an impedance analyzer.

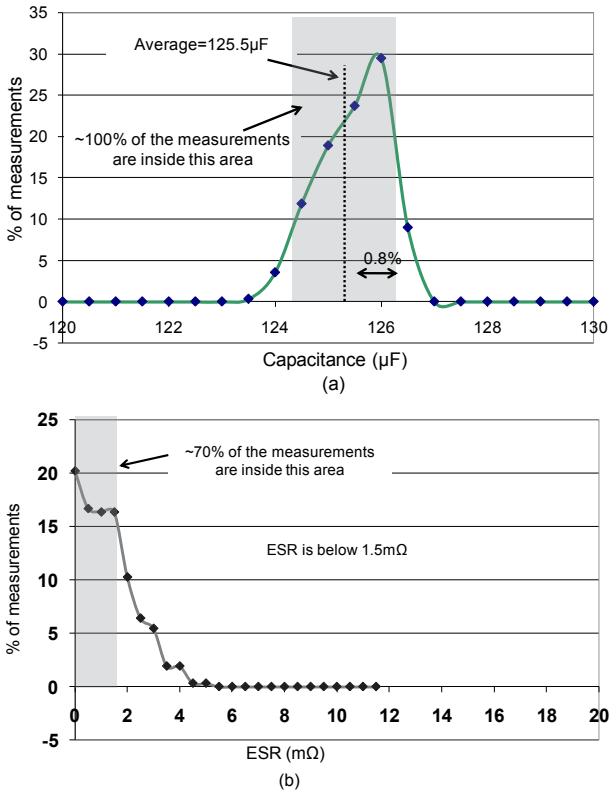

Fig. 11. (a) Capacitance and (b) ESR distribution of the real estimations for a film capacitor (125µF).

VIII. CONCLUSIONS

In this paper, a novel technique for monitoring the condition of electrolytic capacitors in power converters was presented. This proposed technique presents several advantages regarding other alternatives:

1.- Both parameters used in the diagnosis of electrolytic capacitors, ESR and capacitance, are estimated online, and even in real time, while the component is working in the power stage. Since the two parameters of the capacitor are evaluated, the reliability of the predictive maintenance system is enhanced, what is very interesting in high performance applications.

2.- For applying it, it is only necessary to know the inductor current and the capacitor voltage, being these two waveforms, in most of the cases, already sensed for control purposes. The technique does not use a current sensor in series with the capacitor. Such a current sensor would need space, i.e. additional wiring from the capacitor to the bus bar. As result, a parasitic inductance would be added in series with the capacitance due to the current sensor itself and the additional wiring. In a high power application, minimizing inductances in the power stage is a major concern.

3.- Due to the simplicity of the mathematical treatment the hardware required to run the algorithm is simple, inexpensive and compact. In this paper a low cost DSP is proposed to implement the software and obtain both ESR and capacitance.

4.- The only requirement for the hardware would be to sample the current and voltage at least 20 times per switching

period. With a switching frequency of 20 kHz a sampling frequency of 500 kHz per channel was used.

The reliability and the accuracy of the resulting embedded system are proved to be excellent. Although in this paper special emphasis was given to DC/DC converters, the proposed technique can be extended to any other configuration and also to DC link capacitors. It is especially indicated for those cases where it is not possible to place a current sensor in series with the capacitor. All these properties make the proposed technique a good solution to perform electrolytic or Metallized PolyPropylene Film (MPPF) capacitor predictive maintenance in high power converters.

NOMENCLATURE

C - Capacitance of the capacitor.
ESR - Equivalent Series Resistance of the capacitor.
ESL - Equivalent Series Inductance of the capacitor.
R_L - Load resistance.
i_C - Capacitor current.
v_C - Capacitor voltage.
i_L - Inductor current.
i_0 - Load current.
v_C^{avg} - Average value of the capacitor voltage.
i_L^{avg} - Average value of the inductance current.
$\langle \hat{i}_L \rangle_j$ - j-th sampled value of the inductor current.
$\langle \hat{v}_C \rangle_j$ - j-th sampled value of the capacitor voltage.
$\langle i_L \rangle_j$ - Estimated j-th value for the inductor current when fitted by a polynomial approach.
$\langle v_C \rangle_j$ - Estimated j-th value for the capacitor voltage when fitted by a polynomial approach.
$\langle i_C \rangle_j$ - Estimated j-th value of the capacitor current when fitted by a polynomial approach.
$\left\langle \frac{d\, i_C}{dt} \right\rangle_j$ - Estimated j-th value of the derivative of the capacitor current when fitted by a polynomial approach.
$\left\langle \frac{d\, v_C}{dt} \right\rangle_j$ - Estimated j-th value of the derivative of the capacitor voltage when fitted by a polynomial approach.
$\left\langle \frac{d\, i_L}{dt} \right\rangle_j$ - Estimated j-th value of the derivative of the inductor current when fitted by a polynomial approach.
$\langle v_{diode} \rangle_j$ - j-th sampled value of the diode voltage.
D_{ON} - Duty cycle. Fraction of the period with the transistor switched on.
D_{off} - Fraction of the period with the transistor switched off and current in the inductor.
n - Number of times that the inductor current and the capacitor voltage are sampled per period.

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