STRUCTURES OF SINGLE-STAGE AND HIGH POWER FACTOR ELECTRONIC BALLASTS INTEGRATING THE BOOST AND BALLAST INDUCTORS

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***Abstract* – This paper presents a new family of high power factor for electronic ballasts applied to fluorescent lamps. From the proposed structures, two topologies are presented without the ballast inductor, because the boost inductor, in addition to performing power factor correction, also has the function of limiting and stabilizing the lamp current, besides making it to start. The main characteristics of these topologies are the reduction in the production costs owing to fewer components, the low harmonic distortion in the input current, the lower current in the switches, and the lower DC bus voltage. To verify the proposed design methodology and to provide the condition of unity power factor and stabilization of the lamp current, the experimental results of one prototype is presented.**

***Keywords* - Electronic ballast, Fluorescent lamps, High power factor, Charge pump.**

I. INTRODUCTION

Recently, the issue of quality in the electrical energy delivered by electricity distribution systems is gaining attention, mainly owing to energy standards requirements that regulate the electro-electronic equipments. Several of such equipments employ an electronic converter that transforms the energy from AC power supply to different shapes and levels [1]. The majority of converters, for mere economic reasons, spawn distortions to the AC grid voltage waveform, because current waveform is not sinusoidal. In low-power applications, as in the case of lighting systems, the use of new techniques that perform power-factor correction with the objective of minimizing harmonic content while maintaining a near-unity power factor is very attractive [2]–[4]. This is even more important if the cost is kept low.

The use of electronic ballasts operating at high frequencies is clearly attractive owing to several advantages, such as lower energy consumption, higher lighting efficiency (lm/W), reduced magnetic elements, and absence of audible noise and stroboscopic effect [4].

With the objective of reducing implementation costs, usually single-stage topologies are used, i.e., the inverter and PFC stages of the electronic ballast operate in an integrated design [5]–[16].

In fact, one of the most efficient and widely employed techniques is known as Charge Pump, which achieves AC–DC conversion and power-factor correction in a single stage [9]. This work presents a new family of electronic ballasts that are based on this concept. The proposed structures represent a highly viable solution to a great portion of the electric energy market share, which holds around 20% of the total energy consumed by artificial lighting power supplies [17].

II. TOPOLOGY EVOLUTION

The family of electronic ballasts presented in [10] is based on the Voltage Source-Charge Pump Power Factor Correction (VS-CPPFC) concept [9], which, although having a reduced number of components, still exhibits low efficiency and high DC bus voltage as disadvantages, limiting its use in low-power applications, mainly in compact fluorescent lamps. With the aim of achieving an improved efficiency as well as reduced DC bus voltage, the topologies proposed in this paper exhibit the characteristic of current source output, i.e., Continuous Input Current - Charge Pump Power Factor Correction (CIC-CPPFC) [11].

Figure 1(a) shows the proposed CIC circuit presented in [12] and [11]. It can be observed that besides the input boost inductor L_{in}, an LC filter is needed to realize the power-factor correction. In the topology presented in [13] and [7], illustrated in Figure 1(b), the DC bus diode D_{y} is withdrawn. As a consequence, capacitor C_{P} is connected in parallel to one of the rectifier bridge diodes that must be fast, because they produce the "dither" effect [18]–[19]. To turn the topology into a symmetric one, two capacitors C_{P1} and C_{P2} have been used. Such symmetry results in a better energy distribution between the capacitors of the circuit, allowing a lower DC bus voltage and enhancing the power factor by the reduction in the amplitudes of the high-frequency components. Figure 1(c) shows the topology of a CIC electronic ballast published in [14], where, through some modifications, the structures shown in this paper are derived.

In Figure 2(a), a structure where the capacitors C_{f1} and C_{f2}, besides working as input filters and also working as resonant tank circuit capacitor C_{d}, is proposed. The removal of boost inductors L_{in1} and L_{in2} obligates a filter inductor L_{f} (L_{f1}+L_{f2}) to be added, as shown in Figure 2(b). The L_{in1} and

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L_{in2} inductors of Figure 2(a) do not need to be coupled. By employing the dual boost inductors, it is possible to move out the ballast inductor L_B, resulting in the circuit of Figure 2(c). In this case, inductors L_{in1} and L_{in2} operate with several different functions, such as input filter along with capacitors C_{f1} and C_{f2}, current limiter (ballast), and lamp starter.

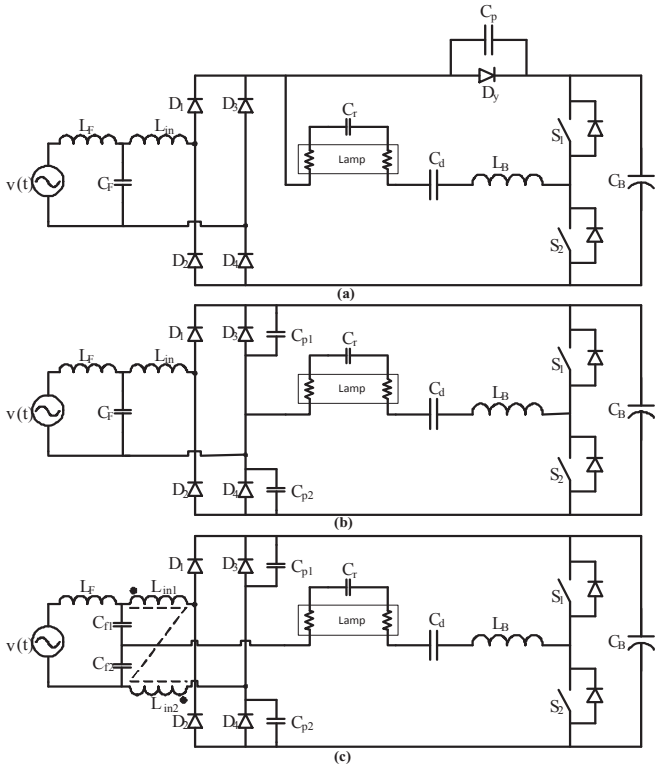


Fig. 1. (a) Topology based on Moisin's (1997) work [12]; (b) Topology presented by Pereira (2004) [13]; (c) Topology presented by Nascimento (2005) [14].

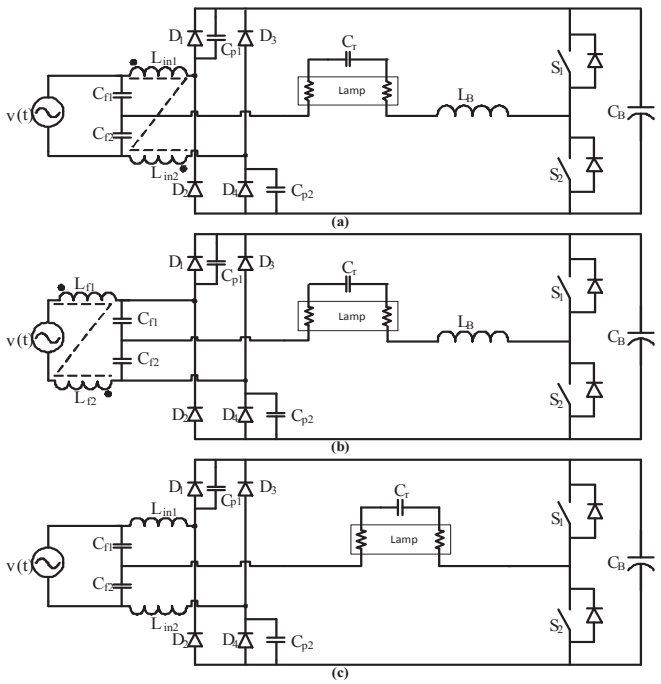


Fig. 2. Proposed topologies 1: (a) without capacitor C_d and without input filter inductor L_f; (b) without capacitor C_d and without boost inductors L_{in1} and L_{in2}; (c) without capacitor C_d and without ballast inductor L_B.

From the proposed topologies, mathematical analysis and experimental results of structure in Figure 2(c) can be presented, because it is a structure that integrates the resonant tank with the PFC stage, as inductors L_{in1} and L_{in2}, together with capacitors C_{f1}, C_{f2}, and C_r, perform the role of limiting the lamp starting current as well as power-factor correction of the electronic ballast.

It can be observed that the topologies proposed in Figure 2 can feed one or more lamps, because they have connection conditions at the midpoint between the capacitors C_{f1} and C_{f2}. However, with the midpoint division, one can obtain another set of topologies, as shown in Figure 3. In this case, the operation of these structures is constrained to the use of two lamps.

Figure 3(a) shows the circuit without capacitors C_{f1} and C_{f2} and ballast inductors L_{B1} and L_{B2}. After the direct connection of the charge-pump capacitors, C_{p1} and C_{p2}, between the power supply $v(t)$ and the rectifier bridge, it is possible to couple inductors L_{in1} and L_{in2}, as stated in Figure 3(b). By removing L_{in1} and L_{in2}, one can obtain the topology shown in Figure 3(c). In this case, a filter inductor must be used, which does not need to be coupled.

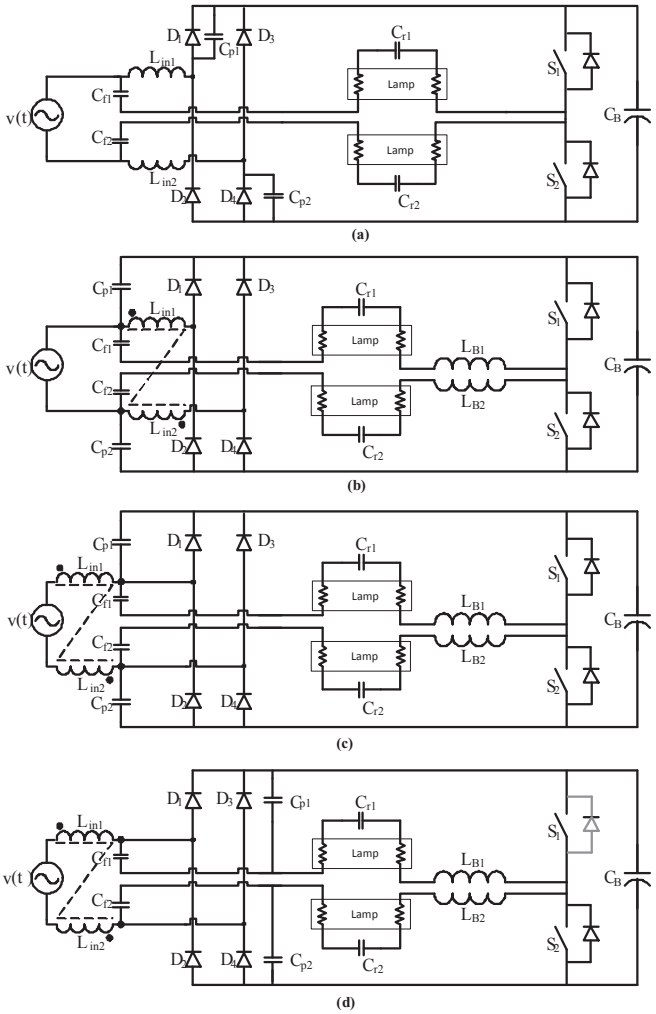


Fig. 3. Proposed topologies 2: (a) without capacitors C_{d1} and C_{d2}, without LC input filter, and without ballast inductors L_{B1} and L_{B2}; (b) without LC filter and with boost inductors L_{in1} and L_{in2} coupled; (c) without boost inductors L_{in1} and L_{in2} and without input filter capacitors C_f; (d) Topology variation from Fig. 3(c).

All the circuits presented in Figs. 2 and 3 exhibit very similar performance characteristics. The main advantages are the high efficiency and low crest factor in the lamp and high input power factor. Every proposed structure can be applied with output power up to 250W. However, by having a fairly small number of components, they are much viable in the use of compact fluorescent lamps with power less than 40 W.

III. STEADY-STATE ANALYSIS

As the way in which the circuit operates in the positive and negative semicycles are the same, and owing to the circuit symmetry in a switching period at high frequency, only half of the entire set of steps in a switching cycle of the positive semicycle is presented.

During the description of the steps of operation and the mathematical model, the following simplifications were considered for the circuit analysis:

The ripple in the bus DC voltage V_B (DC-link C_B) will be disregarded;

The voltage over the power supply $(v(t))$ will be considered constant during a switching period, since the switching frequency is much higher than the mains frequency;

The input current will be considered constant during the whole switching period;

The resonant circuits currents will be considered as ideal current sources;

All the components will be considered ideal.

Stage 1 – $(t_{B0} \sim t_{B1})$: In the previous step, diodes D_1 and D_4 were conducting together with t_1. At t_0, the current across L_{in2} reverses its direction causing the flow of current through capacitor C_{p1}.

Stage 1 initiates exactly when the current across C_B reaches zero, driving D_4 to off-state naturally. From this point ahead, a charge variation in C_{p1} starts, resulting in a voltage reduction in its terminals. As the voltage across the capacitors C_{f1} and C_{f2} are constant during the switching period, the voltages across L_{in1} and L_{in2} change according to voltage over the capacitor C_{p1}, causing these elements to resonate. This step ends when S_1 is turned off and S_2 is turned on.

Stage 2 – $(t_1 \sim t_2)$: At t_1, S_2 is turned on. As currents across inductors L_{in1} and L_{in2} does not vary immediately, diode D_{T2} starts conduction of the load current together with capacitor C_B, which exhibits an instantaneous increase in current. The current across L_{in2} and C_{p1} reverts its direction again, rising the voltage across the C_{p1} terminals.

This step ends when the current across the load reaches zero and the voltage at C_{p1} reaches its clamping value V_B, driving D_4 that goes into conduction.

Stage 3 – $(t_2 \sim t_3)$: At t_2, the current across the load exchange direction and diode D_4 is driven to on-state. In this step, voltages in C_{p1} and C_{p2} are clamped, equal to V_B, and the currents across diodes D_1 and D_4 fall and rise, respectively, according to charge variation at C_B. This step ends when the current across C_B reaches zero and D_1 stops to conduct naturally.

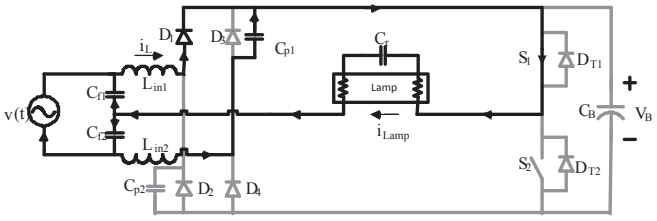


Fig. 4. Operating stage 1 $(t_0–t_1)$.

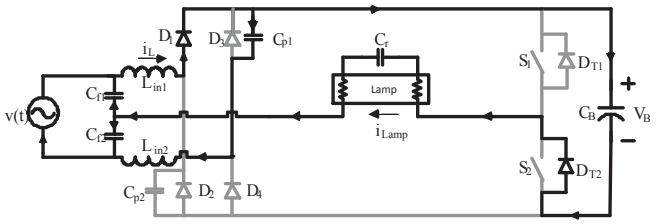


Fig. 5. Operating stage 2 $(t_1–t_2)$.

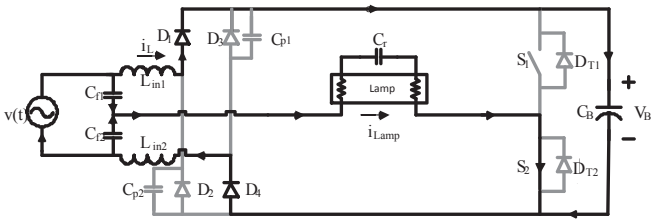


Fig. 6. Operating stage 3 (t_2–t_3).

The theoretical waveforms in steady-state of a switching period from the steps previously described are presented in Figure 7.

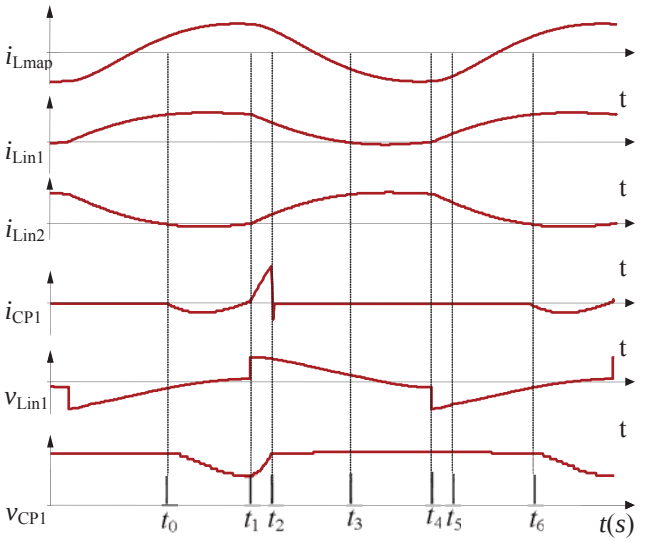


Fig. 7. The theoretical waveforms in steady-state of a switching period.

IV. DESIGN CONSIDERATIONS

The mathematical analysis is carried out through observation of operating steps, which represents the electronic ballast principles of operation. From the mathematical analysis, it is possible to define the main parameters of the presented electronic ballast. It is evident that there is no need to analyze all the steps, because some are repetitive, and therefore, does not influence the calculated

results. Thus, only steps from t_0 to t_3 will be discussed. In this interval, the charge of the capacitor C_{p1} varies, allowing definition of equations in these steps to determine the values of the inductors L_{in1} and L_{in2}, along with the values of capacitors C_{p1} and C_{p2}. As the charge variation in the capacitor C_{p1} is identical to that in C_{p2}, it is needless to reproduce the analysis for the time interval where such variation occurs. Therefore, equations that define C_{p1} and C_{p2} are the same, similar to those that define L_{in1} and L_{in2}.

A. Considerations:

$$v(t) = V_P \sin(\omega t) \tag{1}$$

$$i_{Lamp}(t) = I_{PLamp} \sin(\omega_s t + \theta) \tag{2}$$

$$L_{in1} = L_{in2} = \frac{L}{2} \tag{3}$$

$$C_{p1} = C_{p2} = C \tag{4}$$

$$i_L(t) = i_{Lin1}(t) \tag{5}$$

B. Interval t_0-t_2:

$$i_L(t) = I_{Lamp} \sin(\theta)\cos(\omega_0 t) + + \left(\frac{|v(t)|-V_B}{Z_0}\right)\sin(\omega_0 t) + K \tag{6}$$

Where V_B is the capacitor C_B voltage, I_{Lamp} is defined as

$$I_{Lamp} = \left(1 - \frac{CL}{2}{\omega_s}^2\right) I_{PLamp} \tag{7}$$

and

$$\omega_0 = \frac{1}{\sqrt{CL}}, \quad C = \frac{1}{Z_0 \omega_0} \quad e \quad Z_0 = \sqrt{\frac{L}{C}}$$

with

$$\omega_s = 2\pi f_s \text{ and } T_s = \frac{1}{f_s}$$

Where f_s is the switching frequency of the inverter stage, and

$$K = \frac{{\omega_0}^2}{{\omega_0}^2 - {\omega_s}^2} I_{Lamp}[\sin(\omega_s t + \theta) - \sin(\theta)\cos(\omega_0 t)] - - \frac{{\omega_0}^2}{{\omega_0}^2 - {\omega_s}^2} I_{Lamp}\left[\frac{\omega_s}{\omega_0}\cos(\theta)\sin(\omega_0 t)\right] \tag{8}$$

C. Interval t_2-t_3:

$$i_L(t) = \frac{|v(t)|-V_B}{L}(t - t_2) + i_L(t_2) \tag{9}$$

1. Average $i_L(t)$ current is

$$i_{Lmed} = \frac{1}{T_s}\int_{t_0}^{t_2} i_L(t)dt + \frac{1}{T_s}\int_{t_2}^{t_3} i_L(t)dt \tag{10}$$

Considering that

$$\alpha = \frac{\omega_0}{\omega_s}; \quad t = \frac{\varphi}{\omega_t}; \quad \rightarrow \quad dt = \frac{d\varphi}{\omega_t}; \quad \omega_s T_s = 2\pi \tag{11}$$

Aproximating

$$t_2 = \frac{T_s}{3}, \quad t_3 = \frac{T_s}{2} \quad e \quad i_L(t_2) = I_P = 2\frac{P_{out}}{V_P}$$

where P_{out} is the average power lamp, yelds

$$I_{Lamp} = \frac{\pi(\alpha^2+1)}{\alpha^2}\left[V_B\left(\frac{1}{72Lf_s} + \frac{1-\cos(\alpha\pi)}{2\pi\alpha Z_0}\right) - - \frac{P_{out}}{3V_P} - \left(\frac{1}{2\pi}\frac{1}{\alpha^2-1} I_{Lamp}\right)(1 - \cos(\alpha\pi))\right] \tag{12}$$

$$V_B = \frac{\left[\frac{1}{\pi\alpha^2-1} I_{Lamp} + \left(\frac{1}{2\pi\alpha^2-1} I_{Lamp}\right)(1-\cos(\alpha\pi)) + \frac{P_{out}}{3V_P}\right]}{\frac{T_s}{72L} + \frac{1-\cos(\alpha\pi)}{2\pi\alpha Z_0}} \tag{13}$$

2. Design considerations:

$$P_{in}(t) = |v(t)|.\, i_g(t) \tag{14}$$

$$P_{in}(t) = |v(t)|^2\left[\frac{T_s}{72L} + \frac{1-\cos(\alpha\pi)}{2\pi\alpha Z_0}\right] \tag{15}$$

Considering that average power output is

$$P_{out} = \eta P_{in} \tag{16}$$

where η is the efficiency and P_{in} is the average power input and

$$\omega_0 = \frac{1}{\sqrt{CL}} = \alpha\omega_s \tag{17}$$

yelds

$$C = \left(\frac{2P_{out}}{\eta {V_P}^2 f_s} - \frac{1}{72L{f_s}^2}\right)\frac{1}{1-\cos(\alpha\pi)} \tag{18}$$

and

$$L = \frac{\eta {V_P}^2}{8P_{out}f_s}\left[\frac{1-\cos(\alpha\pi)}{\pi^2\alpha^2} + \frac{1}{18}\right] \tag{19}$$

Figure 8 shows a surface that describes the value of C as a function of f_s and P_{out}. It is remarkable that the values of C are inversely proportional to f_s and directly proportional to P_{out}.

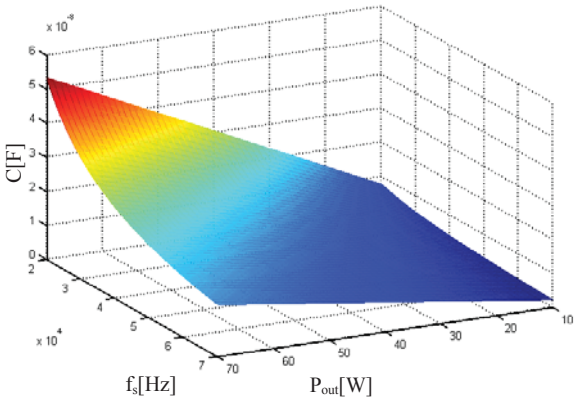


Fig. 8. Variation of C_P as a function of lamp power P_{out} and switching frequency f_s.

The surface shown in Figure 9 demonstrates that as the switching frequency and lamp power increase, the boost inductor L_{in} tends to decrease. These data are important in applications where more compact structures are necessary, as in the case of fluorescent lamps.

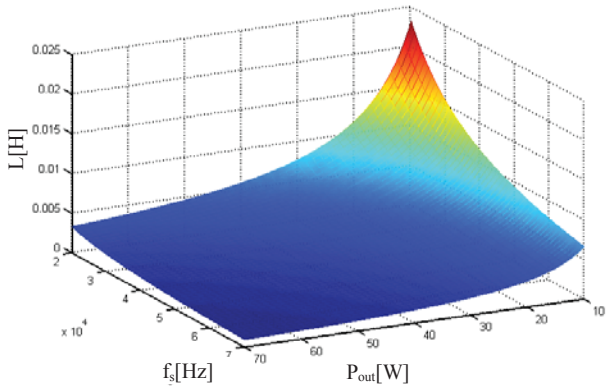


Fig. 9. Variation of L_{in} as a function of lamp power P_{out} and switching frequency f_s.

V. EXPERIMENTAL RESULTS

To achieve the desired experimental results, one prototype using a self-oscillating drive was implemented to verify the design methodology applied to the electronic ballast proposed in Figure 2(c), where a 26W PL-type lamp was used. Figure 10 presents the implemented prototype

Although not all standards require power-factor correction, this work aims to demonstrate the technical viability of the structure under low-power applications, when compared with other electronic ballast structures having power-factor correction.

The parameters used in the calculation of the circuit elements are: switching frequency of 50 kHz, peak input voltage of 311V sinusoidal, efficiency of 90%, and α=0.6 [13].

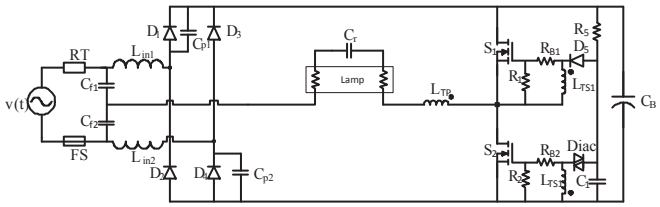


Fig. 10. Diagram of the implemented prototype for 26 W Lamp.

According to the derived equations in the mathematical analysis, the values for the electronic ballast prototype can be obtained. Table I present the implemented design parameters.

TABLE I
Implemented design parameters

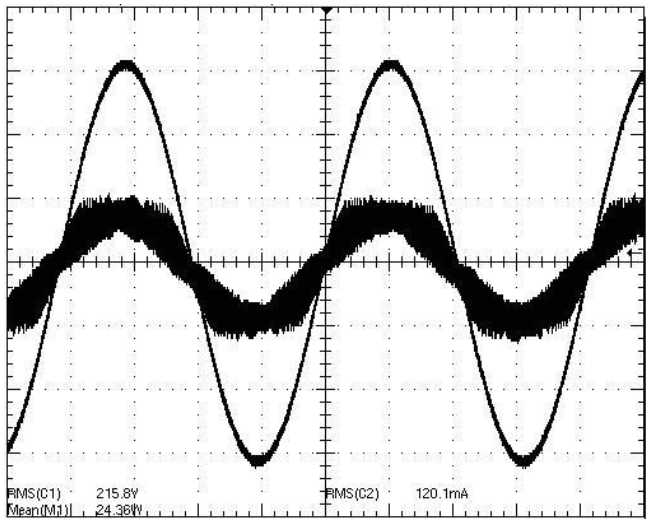
Parameters	Value
L_{in1}=L_{in2}	2mH
C_{p1}=C_{p2}	6.8nF
C_r	5.4nF
C_{f1}=C_{f2}	330nF
R_{B1}=R_{B2}	33Ω
R_1=R_2	1KΩ
C_B	33μF/450V
D_1=D_2= D_3=D_4	1N4937
D_5	1N4936
S_1=S_2	IRF840
R_5	470kΩ

The experimental results obtained are presented in the TABLE II.

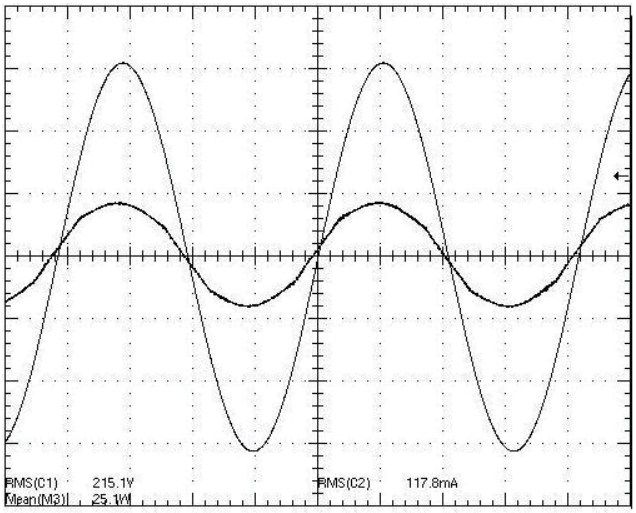
TABLE II
Experimental results obtained

Parameters	Value
P_{in}	25.1W
P_{out}	22.67W
V_B	448V (maximum voltage)
H	90.3%
THD	6.1%
Power Factor	0.996
Crest Factor	1.52

The AC input voltage and current, which tends to be sinusoidal, are presented in Figure 11(a). Remarkably, the electronic ballast complies with the established limits in the standard. To completely eliminate the high-frequency harmonics and the Electromagnetic Interference (EMI) problems, a small filter inductor is used in the electronic ballast input. The AC input voltage and current using an input L_f filter are presented in Figure 11(b). The line-harmonic components (with Total Harmonic Distortion - THD = 6,1%,) , in accordance to the limits established by standard IEC 61000-3-2 for Class C lighting applications, are presented in Figure 12.



(a)



(b)

Fig. 11. (a) Supply voltage and current (t: 4 ms/div; v: 100 V/div; i: 200 mA/div). (b) Supply voltage and current with input inductor L_f filter (L_f=200μH) (t: 4ms/div; v: 100V/div; i: 200mA/div).

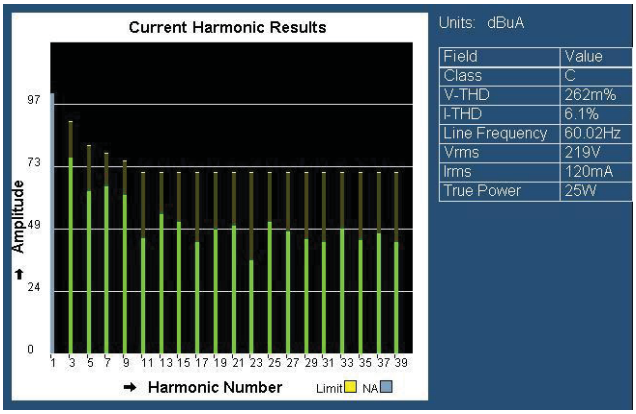


Fig. 12. Supply current harmonics, according to IEC61000-3-2 Class C.

The crest factor measured over the lamp is 1.525, which represents a satisfactory condition, taking into account the limit of 1.7 established in the standard ANSI C82.11, as can be observed in Figure 13. Through Figure12 (True Power) and Figure 13 it can observed that the obtained efficiency is 90%. Figure 14 presents the voltage, current and power of the lamp in high frequency. It can be observed which the waveforms tend to be sinusoidal. Figure 15 presents the lamp startup and it can observe that is of instantaneous type. As the structure has a self-oscillating drive and is devoid of integrated circuits, the application of programmed preheating becomes a complex task, because one of the main targets of this structure is the reduction in production costs. This was possible owing to the smooth on-state switching of the transistors, as shown in Figure 16.

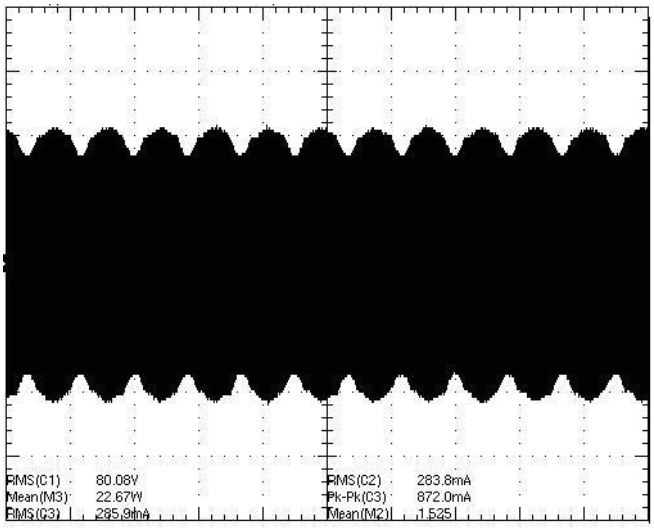


Fig. 13. Current across the lamp with crest factor equal to 1.525 (t: 10 ms/div; i: 200 mA/div).

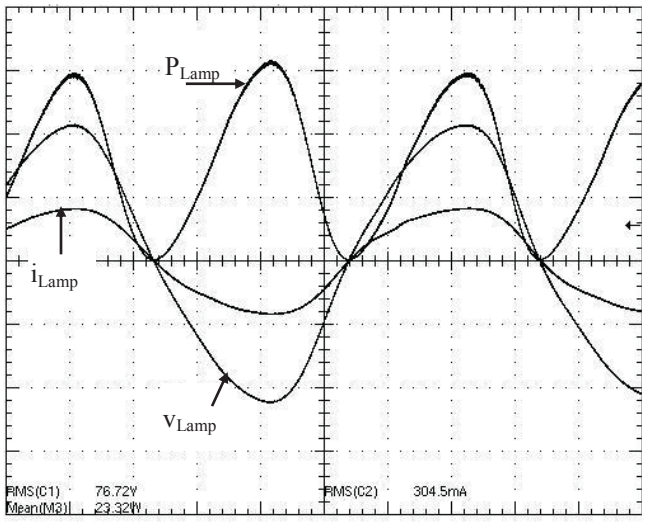


Fig. 14. Voltage, current, and power on the lamp (t: 4 µs/div; v: 50 V/div; i: 500 mA/div; P: 15 W/div).

VI. CONCLUSION

A new family of electronic ballasts for fluorescent lamps has been presented. Using concepts known as the charge pump concept, new structures were obtained, where there is no necessity to use the ballast inductor to limit and stabilize the lamp current, because the boost inductor works a dual role, performing these functions and making power-factor correction.

The withdrawal of the ballast inductor provides the reduction in the number of components, and consequently, weight, volume, and cost. The main features of the CIC electronic ballasts were preserved, such as the high power factor, but a significant improvement in efficiency and crest factor could be observed. The experimental results of the implemented structure show that the electronic ballast has high possibilities of market deployment of compact fluorescent lamps with power-factor correction, because it complies with the IEC 61000-3-2 Class C standard, keeping the limit of the crest factor. In addition, it was also verified that there is no restriction in the use of a self-oscillating drive.

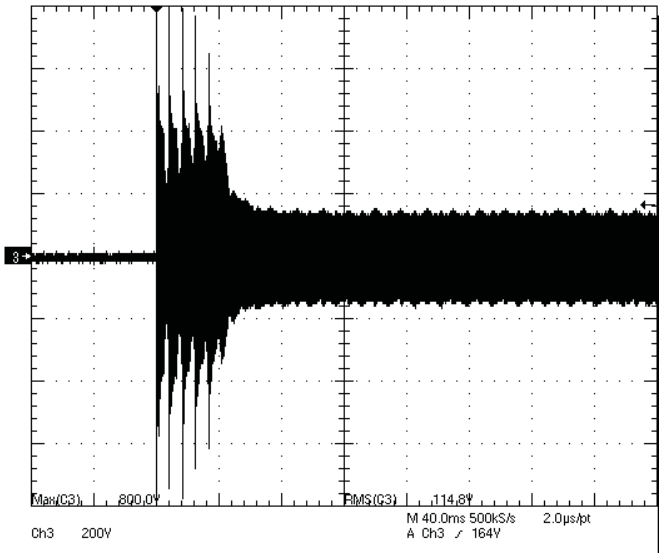


Fig. 15. Startup voltage on the lamp (t: 40 ms/div; v: 200 V/div).

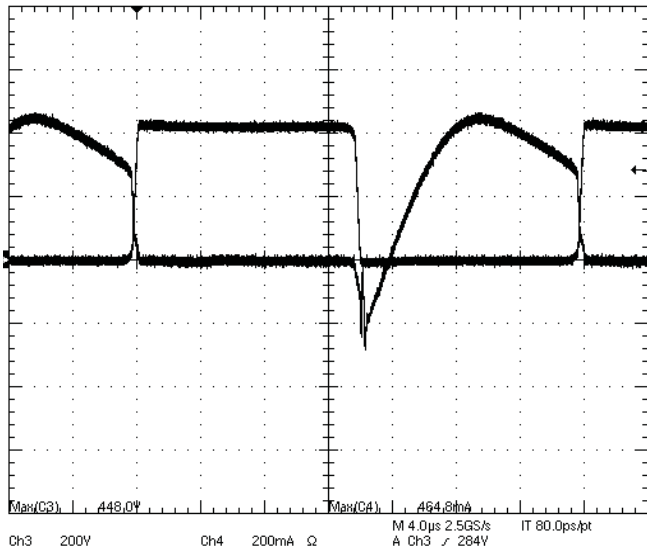


Fig. 16. Voltage and current on the switch during switching (t: 4 µs/div; v: 200 V/div; i: 200 mA/div).

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